Chapter 12

Standard Graphic Symbols

12.1 RECTANGULAR-SHAPE SYMBOLS

Digital components such as gates, decoders, multiplexers, and registers are available commercially in integrated circuits and are classified as SSI or MSI circuits. Standard graphic symbols have been developed for these and other components so that the user can recognize each function from the unique graphic symbol assigned to it. This standard, known as ANSI/IEEE Std. 91-1984, has been approved by industry, government, and professional organizations and is consistent with international standards.

The standard uses a rectangular-shape outline to represent each particular logic function. Within the outline, there is a general qualifying symbol denoting the logical operation performed by the unit. For example, the general qualifying symbol for a multiplexer is MUX. The size of the outline is arbitrary and can be either a square or a rectangular shape with an arbitrary length–width ratio. Input lines are placed on the left and output lines are placed on the right. If the direction of signal flow is reversed, it must be indicated by arrows.

The rectangular-shape graphic symbols for SSI gates are shown in Fig. 12.1. The qualifying symbol for the AND gate is the ampersand (&). The OR gate has the qualifying symbol that designates greater than or equal to 1, indicating that at least one input must be active for the output to be active. The symbol for the buffer gate is 1, showing that only one input is present. The exclusive-OR symbol designates the fact that only one input must be active for the output to be active. The inclusion of the logic negation small circle in the output converts the gates to their complement values. Although the rectangular-shape symbols for the gates are recommended, the standard also recognizes the distinctive-shape symbols for the gates shown in Fig. 2.5.

An example of an MSI standard graphic symbol is the four-bit parallel adder shown in Fig. 12.2. The qualifying symbol for an adder is the Greek letter Σ. The preferred letters for the arithmetic operands are P and Q. The bit-grouping symbols in the two types of inputs and

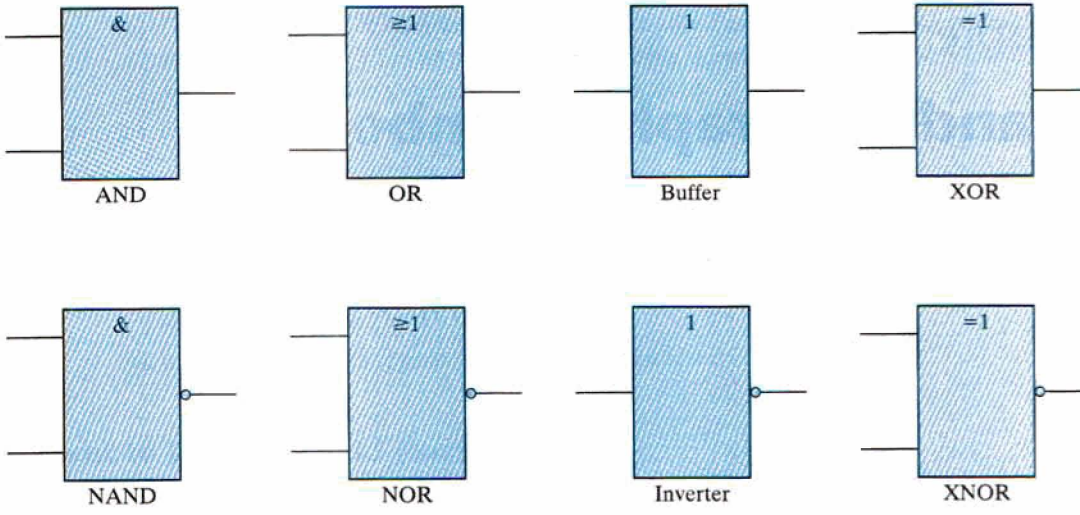


FIGURE 12.1
Rectangular-shape graphic symbols for gates

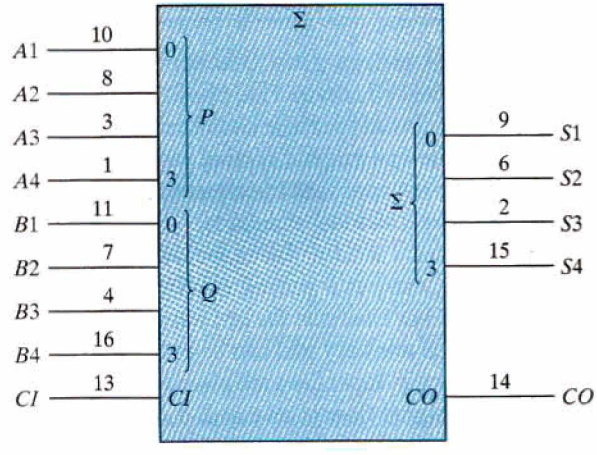


FIGURE 12.2
Standard graphic symbol for a four-bit parallel adder, IC type 7483

the sum output are the decimal equivalents of the weights of the bits to the power of 2. Thus, the input labeled 3 corresponds to the value of $2^3 = 8$. The input carry is designated by *CI* and the output carry by *CO*. When the digital component represented by the outline is also a commercial integrated circuit, it is customary to write the IC pin number along each input and output. Thus, IC type 7483 is a four-bit adder with look-ahead carry. It is enclosed in a package with 16 pins. The pin numbers for the nine inputs and five outputs are shown in Fig. 12.2. The other two pins are for the power supply.

Before introducing the graphic symbols of other components, it is necessary to review some terminology. As mentioned in Section 2.8, a positive-logic system defines the more positive of two signal levels (designated by H) as logic 1 and the more negative signal level (designated by L) as logic 0. Negative logic assumes the opposite assignment. A third alternative is to employ a mixed-logic convention, where the signals are considered entirely in terms of their H and L values. At any point in the circuit, the user is allowed to define the logic polarity by assigning logic 1 to either the H or L signal. The mixed-logic notation uses a small right-angle-triangle graphic symbol to designate a negative-logic polarity at any input or output terminal. (See Fig. 2.10(f).)

Integrated-circuit manufacturers specify the operation of integrated circuits in terms of H and L signals. When an input or output is considered in terms of positive logic, it is defined as *active high*. When it is considered in terms of negative logic, it is defined as *active low*. Active-low inputs or outputs are recognized by the presence of the small-triangle polarity-indicator symbol. When positive logic is used exclusively throughout the entire system, the small-triangle polarity symbol is equivalent to the small circle that designates negation. In this book, we have assumed positive logic throughout and employed the small circle when drawing logic diagrams. When an input or output line does not include the small circle, we define it to be active if it is logic 1. An input or output that includes the small-circle symbol is considered active if it is in the logic-0 state. However, we will use the small-triangle polarity symbol to indicate active-low assignment in all drawings that represent standard diagrams. This will conform with integrated-circuit data books, where the polarity symbol is usually employed. Note that the bottom four gates in Fig. 12.1 could have been drawn with a small triangle in the output lines instead of a small circle.

Another example of a graphic symbol for an MSI circuit is shown in Fig. 12.3. This is a 2-to-4-line decoder representing one-half of IC type 74155. Inputs are on the left and outputs on the right. The identifying symbol X/Y indicates that the circuit converts from code X to code Y. Data inputs A and B are assigned binary weights 1 and 2 equivalent to 2^0 and 2^1, respectively. The outputs are assigned numbers from 0 to 3, corresponding to outputs D_0 through D_3, respectively. The decoder has one active-low input E_1 and one active-high input E_2. These two inputs go through an internal AND gate to enable the decoder. The output of the AND gate is labeled EN (enable) and is activated when E_1 is at a low-level state and E_2 at a high-level state.

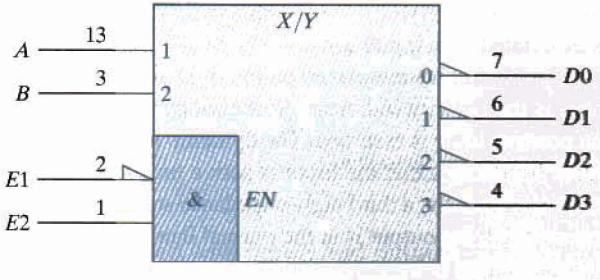


FIGURE 12.3
Standard graphic symbol for a 2-to-4-line decoder (one-half of IC type 74155)

12.2 QUALIFYING SYMBOLS

The IEEE standard graphic symbols for logic functions provide a list of qualifying symbols to be used in conjunction with the outline. A qualifying symbol is added to the basic outline to designate the overall logic characteristics of the element or the physical characteristics of an input or output. Table 12.1 lists some of the general qualifying symbols specified in the standard. A general qualifying symbol defines the basic function performed by the device represented in the diagram. It is placed near the top center position of the rectangular-shape outline. The general qualifying symbols for the gates, decoder, and adder were shown in previous diagrams. The other symbols are self-explanatory and will be used later in diagrams representing the corresponding digital elements.

Table 12.1
General Qualifying Symbols

Symbol	Description
&	AND gate or function
≥1	OR gate or function
1	Buffer gate or inverter
=1	Exclusive-OR gate or function
2k	Even function or even parity element
2k + 1	Odd function or odd parity element
X/Y	Coder, decoder, or code converter
MUX	Multiplexer
DMUX	Demultiplexer
Σ	Adder
Π	Multiplier
COMP	Magnitude comparator
ALU	Arithmetic logic unit
SRG	Shift register
CTR	Counter
RCTR	Ripple counter
ROM	Read-only memory
RAM	Random-access memory

Some of the qualifying symbols associated with inputs and outputs are shown in Fig. 12.4. Symbols associated with inputs are placed on the left side of the column labeled *symbol*. Symbols associated with outputs are placed on the right side of the column. The active-low input or output symbol is the polarity indicator. As mentioned previously, it is equivalent to the logic negation when positive logic is assumed. The dynamic input is associated with the clock input in flip-flop circuits. It indicates that the input is active on a transition from a low-to-high-level signal. The three-state output has a third high-impedance state, which has no logic significance. When the circuit is enabled, the output is in the normal 0 or 1 logic state, but when the circuit is disabled, the three-state output is in a high-impedance state. This state is equivalent to an open circuit.

The open-collector output has one state that exhibits a high-impedance condition. An externally connected resistor is sometimes required in order to produce the proper logic level.

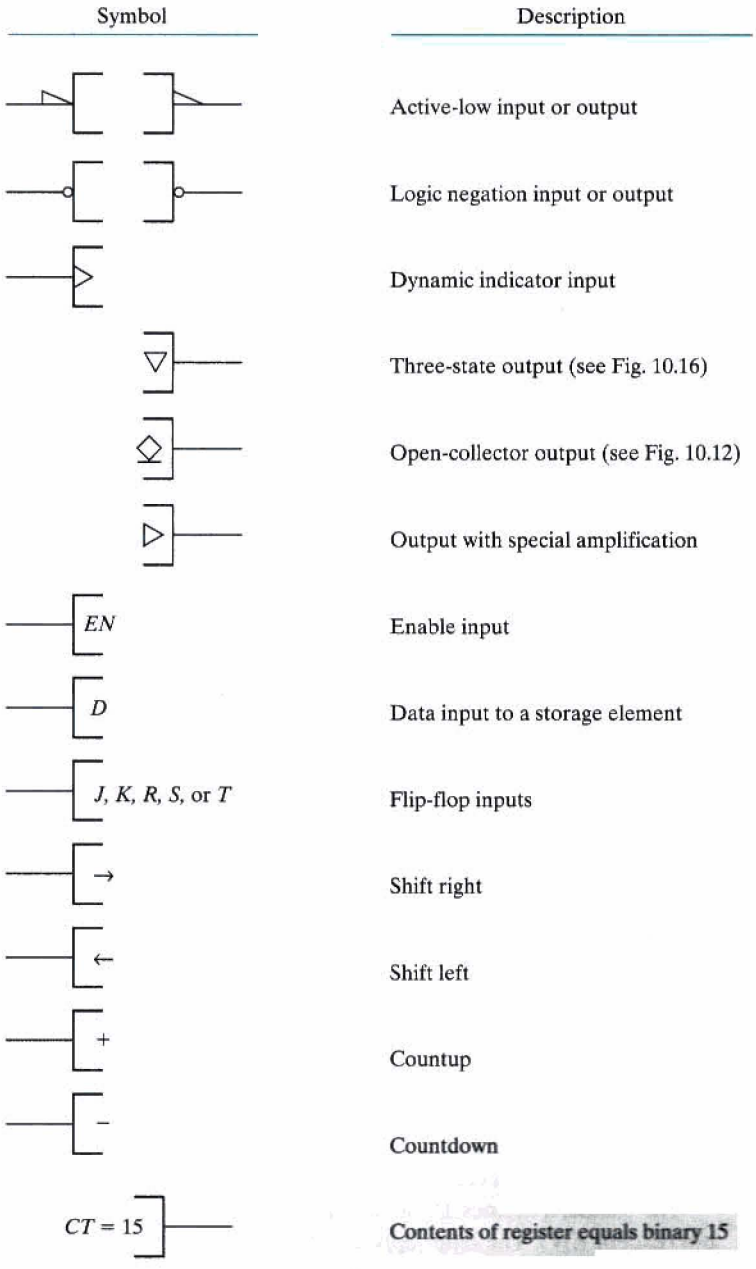


FIGURE 12.4
Qualifying symbols associated with inputs and outputs

The diamond-shape symbol may have a bar on top (for high type) or on the bottom (for low type). The high or low type specifies the logic level when the output is not in the high-impedance state. For example, TTL-type integrated circuits have special outputs called open-collector outputs. These outputs are recognized by a diamond-shape symbol with a bar under it. This indicates that the output can be either in a high-impedance state or in a low-level state. When used as part of a distribution function, two or more open-collector NAND gates when connected to a common resistor perform a positive-logic AND function or a negative-logic OR function.

The output with special amplification is used in gates that provide special driving capabilities. Such gates are employed in components such as clock drivers or bus-oriented transmitters. The *EN* symbol designates an enable input. It has the effect of enabling all outputs when it is active. When the input marked with *EN* is inactive, all outputs are disabled. The symbols for flip-flop inputs have the usual meaning. The *D* input is also associated with other storage elements such as memory input.

The symbols for shift right and shift left are arrows pointing to the right or the left, respectively. The symbols for count-up and count-down counters are the plus and minus symbols, respectively. An output designated by $CT = 15$ will be active when the contents of the register reach the binary count of 15. When nonstandard information is shown inside the outline, it is enclosed in square brackets [like this].

12.3 DEPENDENCY NOTATION

The most important aspect of the standard logic symbols is the dependency notation. Dependency notation is used to provide the means of denoting the relationship between different inputs or outputs without actually showing all the elements and interconnections between them. We will first demonstrate the dependency notation with an example of the AND dependency and then define all the other symbols associated with this notation.

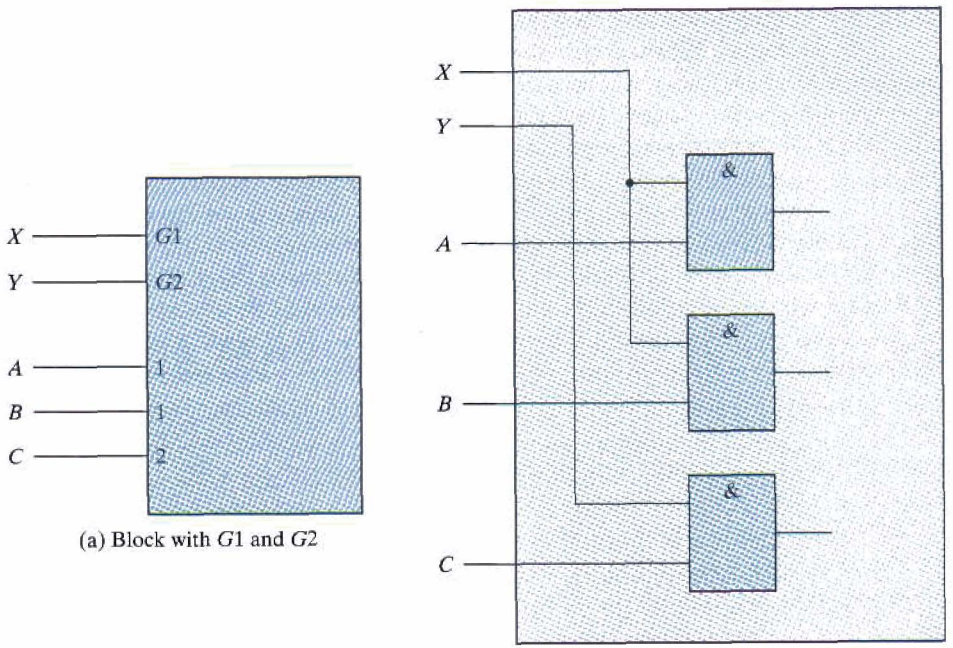
The AND dependency is represented with the letter *G* followed by a number. Any input or output in a diagram that is labeled with the number associated with *G* is considered to be ANDed with it. For example, if one input in the diagram has the label *G* 1 and another input is labeled with the number 1, then the two inputs labeled *G* 1 and 1 are considered to be ANDed together internally.

An example of AND dependency is shown in Fig. 12.5. In (a), we have a portion of a graphic symbol with two AND dependency labels, *G* 1 and *G* 2. There are two inputs labeled with the number 1 and one input labeled with the number 2. The equivalent interpretation is shown in part (b) of the figure. Input *X* associated with *G* 1 is considered to be ANDed with inputs *A* and *B*, which are labeled with a 1. Similarly, input *Y* is ANDed with input *C* to conform with the dependency between *G* 2 and 2.

The standard defines 10 other dependencies. Each dependency is denoted by a letter symbol (except *EN*). The letter appears at the input or output and is followed by a number. Each input or output affected by that dependency is labeled with that same number. The 11 dependencies and their corresponding letter designation are as follows:

G Denotes an AND (gate) relationship

V Denotes an OR relationship



(a) Block with *G*1 and *G*2

(b) Equivalent interpretation

FIGURE 12.5
Example of G (AND) dependency

N	Denotes a negate (exclusive-OR) relationship
EN	Specifies an enable action
C	Identifies a control dependency
S	Specifies a setting action
R	Specifies a resetting action
M	Identifies a mode dependency
A	Identifies an address dependency
Z	Indicates an internal interconnection
X	Indicates a controlled transmission

The *V* and *N* dependencies are used to denote the Boolean relationships of OR and exclusive-OR similar to the *G* that denotes the Boolean AND. The *EN* dependency is similar to the qualifying symbol *EN* except that a number follows it (for example, *EN*2). Only the outputs marked with that number are disabled when the input associated with *EN* is active.

The control dependency *C* is used to identify a clock input in a sequential element and to indicate which input is controlled by it. The set *S* and reset *R* dependencies are used to specify internal logic states of an *SR* flip-flop. The *C*, *S*, and *R* dependencies are explained in Section 12.5

in conjunction with the flip-flop circuit. The mode M dependency is used to identify inputs that select the mode of operation of the unit. The mode dependency is presented in Section 12.6 in conjunction with registers and counters. The address A dependency is used to identify the address input of a memory. It is introduced in Section 12.8 in conjunction with the memory unit.

The Z dependency is used to indicate interconnections inside the unit. It signifies the existence of internal logic connections between inputs, outputs, internal inputs, and internal outputs, in any combination. The X dependency is used to indicate the controlled transmission path in a CMOS transmission gate.

12.4 SYMBOLS FOR COMBINATIONAL ELEMENTS

The examples in this section and the rest of this chapter illustrate the use of the standard in representing various digital components with graphic symbols. The examples demonstrate actual commercial integrated circuits with the pin numbers included in the inputs and outputs. Most of the ICs presented in this chapter are included with the suggested experiments outlined in Chapter 11.

The graphic symbols for the adder and decoder were shown in Section 12.2. IC type 74155 can be connected as a 3 × 8 decoder, as shown in Fig. 12.6. (The truth table of this decoder is shown in Fig. 11.7.) There are two C and two G inputs in the IC. Each pair must be connected together as shown in the diagram. The enable input is active when in the low-level state. The outputs are all active low. The inputs are assigned binary weights 1, 2, and 4, equivalent to 2^0, 2^1, and 2^2, respectively. The outputs are assigned numbers from 0 to 7. The sum of the weights of the inputs determines the output that is active. Thus, if the two input lines with weights 1 and 4 are activated, the total weight is 1 + 4 = 5 and output 5 is activated. Of course, the EN input must be activated for any output to be active.

The decoder is a special case of a more general component referred to as a *coder*. A coder is a device that receives an input binary code on a number of inputs and produces a different binary code on a number of outputs. Instead of using the qualifying symbol X/Y, the coder can be specified by

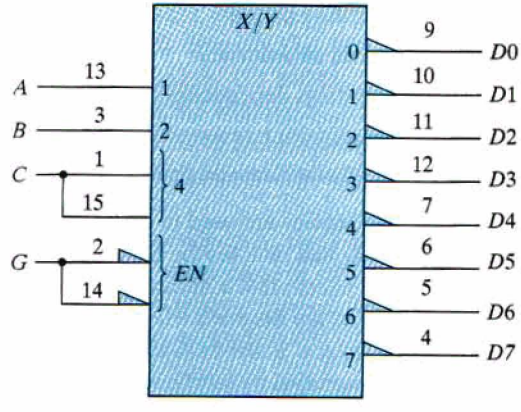


FIGURE 12.6
IC type 74155 connected as a 3 × 8 decoder

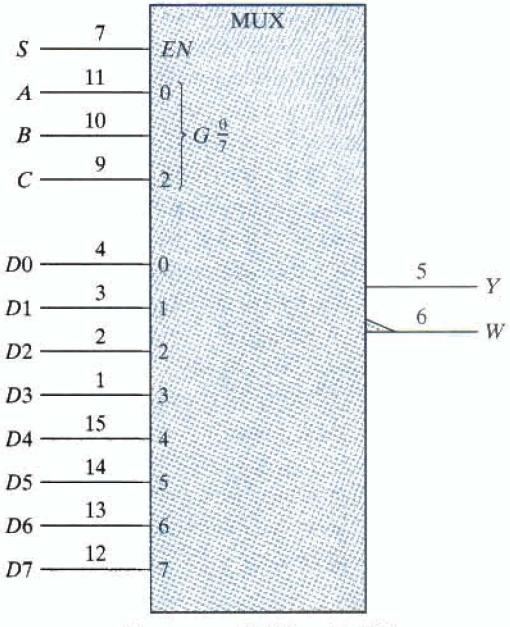
the code name. For example, the 3-to-8-line decoder of Fig. 12.6 can be symbolized with the name *BIN/OCT* since the circuit converts a 3-bit binary number into 8 octal values, 0 through 7.

Before showing the graphic symbol for the multiplexer, it is necessary to show a variation of the AND dependency. The AND dependency is sometimes represented by a shorthand notation like $G\frac{0}{7}$. This symbol stands for eight AND dependency symbols from 0 to 7 as follows:

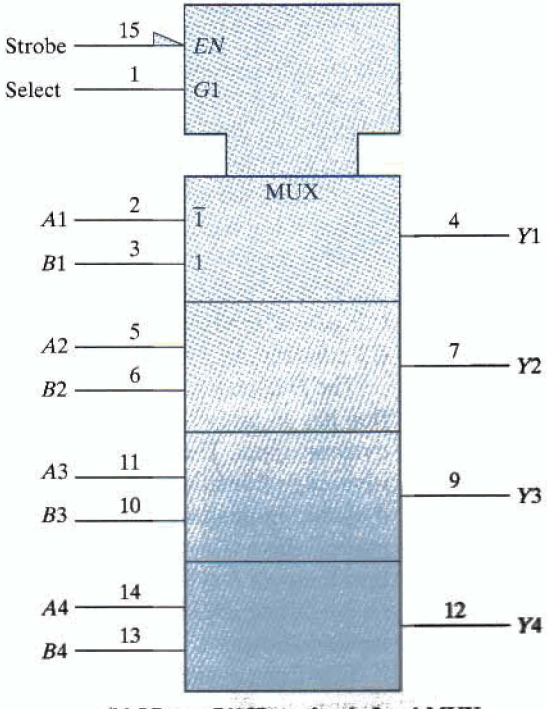
$$G0, G1, G2, G3, G4, G5, G6, G7$$

At any given time, only one out of the eight AND gates can be active. The active AND gate is determined from the inputs associated with the G symbol. These inputs are marked with weights equal to the powers of 2. For the eight AND gates just listed, the weights are 0, 1, and 2, corresponding to the numbers 2^0, 2^1, and 2^2, respectively. The AND gate that is active at any given time is determined from the sum of the weights of the active inputs. Thus, if inputs 0 and 2 are active, then the AND gate that is active has the number $2^0 + 2^2 = 5$. This makes $G5$ active and the other seven AND gates inactive.

The standard graphic symbol for a 8 × 1 multiplexer is shown in Fig. 12.7(a). The qualifying symbol MUX identifies the device as a multiplexer. The symbols inside the block are part of the standard notation, but the symbols marked outside are user-defined symbols. The function table of the 741551 IC can be found in Fig. 11.9. The AND dependency is marked with $G\frac{0}{7}$ and is associated with the inputs enclosed in brackets. These inputs have weights of 0, 1,



(a) IC type 74151 8 × 1 MUX



(b) IC type 74157 quadruple 2 × 1 MUX

FIGURE 12.7
Graphic symbols for multiplexers

and 2. They are actually what we have called the selection inputs. The eight data inputs are marked with numbers from 0 to 7. The net weight of the active inputs associated with the G symbol specifies the number in the data input that is active. For example, if selection inputs $CBA = 110$, then inputs 1 and 2 associated with G are active. This gives a numerical value for the AND dependency of $2^2 + 2^1 = 6$, which makes $G6$ active. Since $G6$ is ANDed with data input number 6, it makes this input active. Thus, the output will be equal to data input D_6 provided that the enable input is active.

Fig.12.7(b) represents the quadruple 2 × 1 multiplexer IC type 74157 whose function table is listed in Fig. 11.17. The enable and selection inputs are common to all four multiplexers. This is indicated in the standard notation by the indented box at the top of the diagram, which represents a *common control block.* The inputs to a common control block control all lower sections of the diagram. The common enable input EN is active when in the low-level state. The AND dependency, $G1$, determines which input is active in each multiplexer section. When $G1 = 0$, the A inputs marked with $\bar{1}$ are active. When $G1 = 1$, the B inputs marked with 1 are active. The active inputs are applied to the corresponding outputs if EN is active. Note that the input symbols $\bar{1}$ and 1 are marked in the upper section only instead of repeating them in each section.

12.5 SYMBOLS FOR FLIP-FLOPS

The standard graphic symbols for different types of flip-flops are shown in Fig. 12.8. A flip-flop is represented by a rectangular-shaped block with inputs on the left and outputs on the right. One output designates the normal state of the flip-flop and the other output with a small-circle negation symbol (or polarity indicator) designates the complement output. The graphic symbols distinguish between three types of flip-flops: the D latch, whose internal construction is shown in Fig. 6.5; the master–slave flip-flop, shown in Fig. 6.9; and the edge-triggered flip-flop, introduced in Fig. 6.12. The graphic symbol for the D latch or D flip-flop has inputs D and C indicated inside the block. The graphic symbol for the JK flip-flop has inputs J, K, and C inside. The notation $C1$, $1D$, $1J$, and $1K$ are examples of control dependency. The input in $C1$ controls input $1D$ in a D flip-flop and inputs $1J$ and $1K$ in a JK flip-flop.

The D latch has no other symbols besides the $1D$ and $C1$ inputs. The edge-triggered flip-flop has an arrowhead-shaped symbol in front of the control dependency $C1$ to designate a dynamic input. The dynamic indicator symbol denotes that the flip-flop responds to the positive-edge transition of the input clock pulses. A small circle outside the block along the dynamic indicator designates a negative-edge transition for triggering the flip-flop. The master–slave is considered to be a pulse-triggered flip-flop and is indicated as such with an upside-down L symbol in front of the outputs. This is to show that the output signal changes on the falling edge of the pulse. Note that the master–slave flip-flop is drawn without the dynamic indicator.

Flip-flops available in integrated-circuit packages provide special inputs for setting and resetting the flip-flop asynchronously. These inputs are usually called direct set and direct reset. They affect the output on the negative level of the signal without the need of a clock. The graphic symbol of a master–slave JK flip-flop with direct set and reset is shown in Fig. 12.9(a).

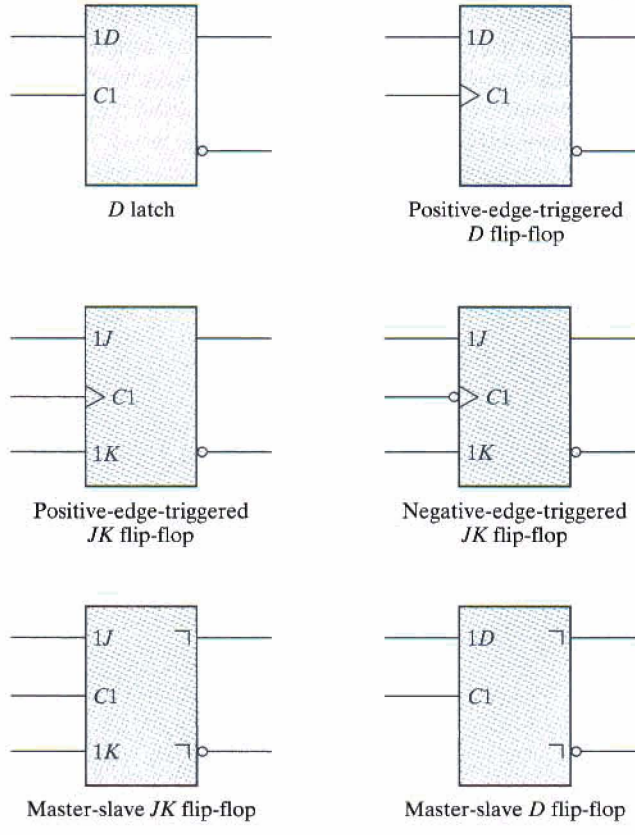


FIGURE 12.8
Standard graphic symbols for flip-flops

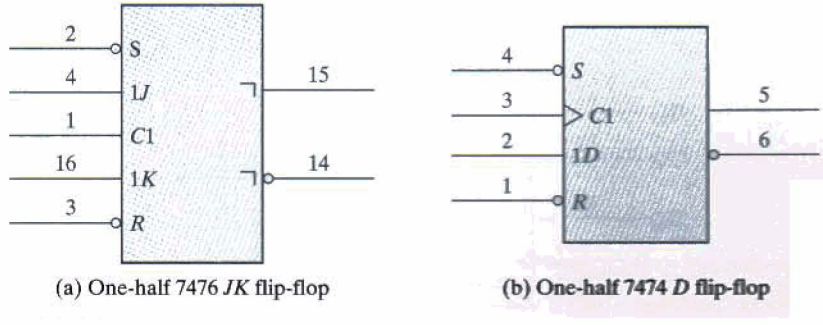


FIGURE 12.9
IC flip-flops with direct set and reset

The notations $C1$, $1J$, and $1K$ represent control dependency, showing that the clock input at $C1$ controls inputs $1J$ and $1K$. S and R have no 1 in front of the letters and, therefore, they are not controlled by the clock at $C1$. The S and R inputs have a small circle along the input lines to indicate that they are active when in the logic-0 level. The function table for the 7476 flip-flop is shown in Fig. 11.12.

The graphic symbol for a positive-edge-triggered D flip-flop with direct set and reset is shown in Fig. 12.9(b). The positive-edge transition of the clock at input $C1$ controls input $1D$. The S and R inputs are independent of the clock. This is IC type 7474, whose function table is listed in Fig. 11.13.

12.6 SYMBOLS FOR REGISTERS

The standard graphic symbol for a register is equivalent to the symbol used for a group of flip-flops with a common clock input. Fig. 12.10 shows the standard graphic symbol of IC type 74175, consisting of four D flip-flops with common clock and clear inputs. The clock input $C1$ and the clear input R appear in the common control block. The inputs to the common control block are connected to each of the elements in the lower sections of the diagram. The notation $C1$ is the control dependency that controls all the $1D$ inputs. Thus, each flip-flop is triggered

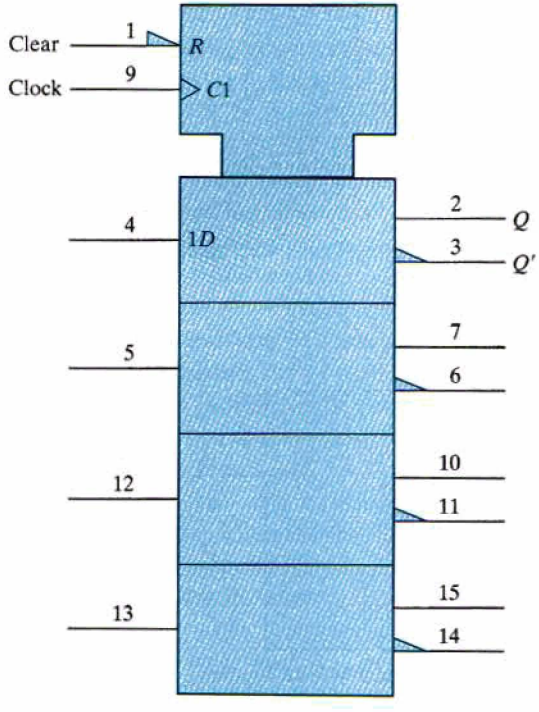


FIGURE 12.10
Graphic symbol for a four-bit register, IC type 74175

by the common clock input. The dynamic input symbol associated with $C1$ indicates that the flip-flops are triggered on the positive edge of the input clock. The common R input resets all flip-flops when its input is at a low-level state. The $1D$ symbol is placed only once in the upper section instead of repeating it in each section. The complement outputs of the flip-flops in this diagram are marked with the polarity symbol rather than the negation symbol.

The standard graphic symbol for a shift register with parallel load is shown in Fig. 12.11. This is IC type 74195, whose function table can be found in Fig. 11.16. The qualifying symbol for a shift register is SRG followed by a number that designates the number of stages. Thus, $SRG4$ denotes a four-bit shift register. The common control block has two mode dependencies, $M1$ and $M2$, for the shift and load operations, respectively. Note that the IC has a single input labeled SH/LD (shift/load), which is split into two lines to show the two modes. $M1$ is active when the SH/LD input is high and $M2$ is active when the SH/LD input is low. $M2$ is recognized as active low from the polarity indicator along its input line. Note the convention in this symbology: We must recognize that a single input actually exists in pin 9, but it is split into two parts in order to assign to it the two modes, $M1$ and $M2$. The control dependency $C3$ is for the clock input. The dynamic symbol along the $C3$ input indicates that the flip-flops trigger on the positive edge of the clock. The symbol $/1 \rightarrow$ following $C3$ indicates that the register shifts to the right or in the downward direction when mode $M1$ is active.

The four sections below the common control block represent the four flip-flops. Flip-flop QA has three inputs: Two are associated with the serial (shift) operation and one with the

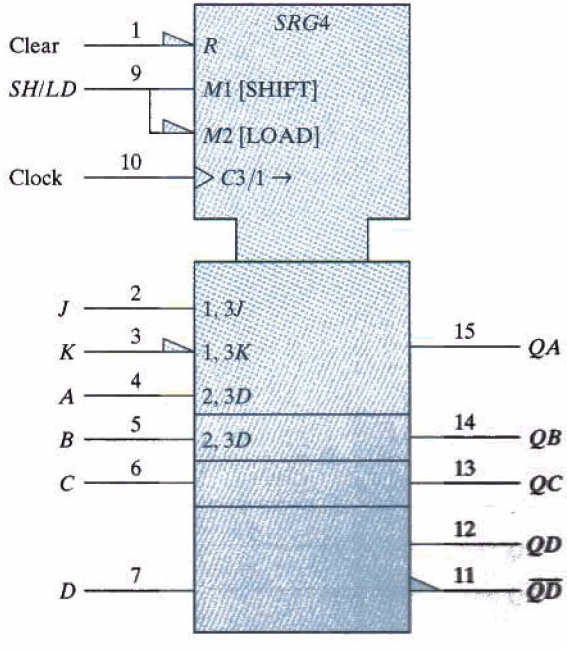


FIGURE 12.11
Graphic symbol for a shift register with parallel load, IC type 74195

parallel (load) operation. The serial input label 1, 3*J* indicates that the *J* input of flip-flop *QA* is active when *M* 1 (shift) is active and *C* 3 goes through a positive clock transition. The other serial input with label 1, 3*K* has a polarity symbol in its input line corresponding to the complement of input *K* in a *JK* flip-flop. The third input of *QA* and the inputs of the other flip-flops are for the parallel input data. Each input is denoted by the label 2, 3*D*. The 2 is for *M* 2 (load), and 3 is for the clock *C* 3. If the input in pin number 9 is in the low level, *M* 1 is active, and a positive transition of the clock at *C* 3 causes a parallel transfer from the four inputs, *A* through *D*, into the four flip-flops, *QA* through *QD*. Note that the parallel input is labeled only in the first and second sections. It is assumed to be in the other two sections below.

Figure 12.12 shows the graphic symbol for the bidirectional shift register with parallel load, IC type 74194. The function table for this IC is listed in Fig. 11.19. The common control block shows an *R* input for resetting all flip-flops to 0 asynchronously. The mode select has two inputs and the mode dependency *M* may take binary values from 0 to 3. This is indicated by the symbol $M\frac{0}{3}$, which stands for *M* 0, *M* 1, *M* 2, *M* 3, and is similar to the notation for the *G* dependency in multiplexers. The symbol associated with the clock is

$$C4/1 \rightarrow \quad /2 \leftarrow$$

C 4 is the control dependency for the clock. The $/1 \rightarrow$ symbol indicates that the register shifts right (down in this case) when the mode is $M1\,(S_1S_0 = 01)$. The $/2 \leftarrow$ symbol indicates that the register shifts left (up in this case) when the mode is $M_2\,(S_1S_0 = 10)$. The right and left directions are obtained when the page is turned 90 degrees counterclockwise.

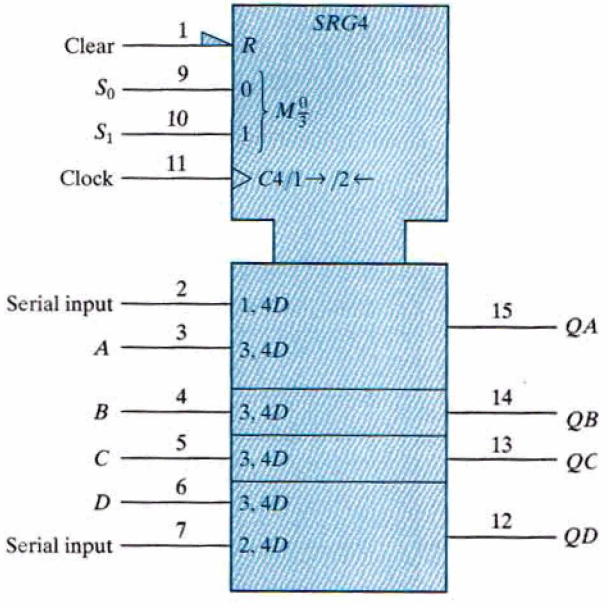


FIGURE 12.12
Graphic symbol for a bidirectional shift register with parallel load, IC type 74194

The sections below the common control block represent the four flip-flops. The first flip-flop has a serial input for shift right, denoted by 1, 4 *D* (mode *M* 1, clock *C* 4, input *D*). The last flip-flop has a serial input for shift left, denoted by 2, 4 *D* (mode *M* 2, clock *C* 4, input *D*). All four flip-flops have a parallel input denoted by the label 3, 4 *D* (mode *M* 3, clock *C* 4, input *D*). Thus, *M* 3 $(S_1S_0 = 11)$ is for parallel load. The remaining mode *M* 0 $(S_1S_0 = 00)$ has no effect on the outputs because it is not included in the input labels.

12.7 SYMBOLS FOR COUNTERS

The standard graphic symbol of a binary ripple counter is shown in Fig. 12.13. The qualifying symbol for a ripple counter is *RCTR*. The designation *DIV* 2 stands for the divide-by-2 circuit that is obtained from the single flip-flop *QA*. The *DIV* 8 designation is for the divide-by-8 counter obtained from the other three flip-flops. The diagram represents IC type 7493, whose internal circuit diagram is shown in Fig. 11.2. The common control block has an internal AND gate, with inputs *R* 1 and *R* 2. When both of these inputs are equal to 1, the content of the counter goes to zero. This is indicated by the symbol *CT* = 0. Since the count input does not go to the clock inputs of all flip-flops, it has no *C* 1 label and, instead, the symbol + is used to indicate a count-up operation. The dynamic symbol next to the + together with the polarity symbol along the input line signify that the count is affected with a negative-edge transition of the input signal. The bit grouping from 0 to 2 in the output represents values for the weights to the power of 2. Thus, 0 represents the value of $2^0 = 1$ and 2 represents the value $2^2 = 4$.

The standard graphic symbol for the four-bit counter with parallel load, IC type 74161, is shown in Fig. 12.14. The qualifying symbol for a synchronous counter is *CTR* followed by the symbol *DIV* 16 (divide by 16), which gives the cycle length of the counter. There is a single

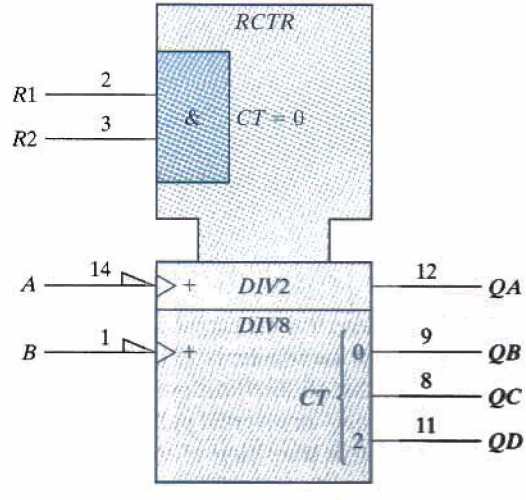


FIGURE 12.13
Graphic symbol for ripple counter, IC type 7493

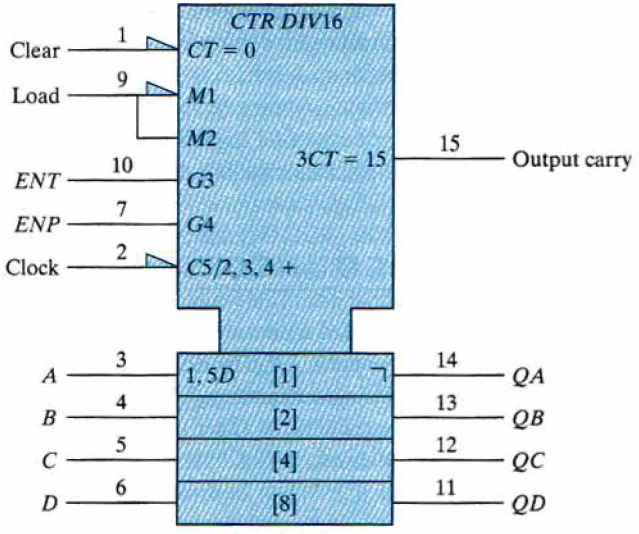


FIGURE 12.14
Graphic Symbol for 4-Bit Binary Counter with Parallel Load, IC Type 74161

load input at pin 9 that is split into the two modes, $M1$ and $M2$. $M1$ is active when the load input at pin 9 is low and $M2$ is active when the load input at pin 9 is high. $M1$ is recognized as active low from the polarity indicator along its input line. The count-enable inputs use the G dependencies. $G3$ is associated with the T input and $G4$ with the P input of the count enable. The label associated with the clock is

$$C5/2, 3, 4 \ +$$

This means that the circuit counts up (the + symbol) when $M2$, $G3$, and $G4$ are active (load = 1, ENT = 1, and ENP = 1) and the clock in $C5$ goes through a positive transition. This condition is specified in the function table of the 74161 listed in Fig. 11.15. The parallel inputs have the label 1, 5 D, meaning that the D inputs are active when $M1$ is active (load = 0) and the clock goes through a positive transition. The output carry is designated by the label

$$3CT = 15$$

This is interpreted to mean that the output carry is active (equal to 1) if $G3$ is active ($ENT = 1$) and the content (CT) of the counter is 15 (binary 1111). Note that the outputs have an inverted L symbol, indicating that all the flip-flops are of the master–slave type. The polarity symbol in the $C5$ input designates an inverted pulse for the input clock. This means that the master is triggered on the negative transition of the clock pulse and the slave changes state on the positive transition. Thus, the output changes on the positive transition of the clock pulse. It should be noted that IC type 74LS161 (low-power Schottky version) has positive-edge-triggered flip-flops.

12.8 SYMBOL FOR RAM

The standard graphic symbol for the random-access memory (RAM) 74189 is shown in Fig. 12.15. The numbers 16 × 4 that follow the qualifying symbol RAM designate the number of words and the number of bits per word. The common control block is shown with four address lines and two control inputs. Each bit of the word is shown in a separate section with an input and output data line. The address dependency *A* is used to identify the address inputs of the memory. Data inputs and outputs affected by the address are labeled with the letter *A*. The bit grouping from 0 through 3 provides the binary address that ranges from *A* 0 through *A* 15. The inverted triangle signifies three-state outputs. The polarity symbol specifies the inversion of the outputs.

The operation of the memory is specified by means of the dependency notation. The RAM graphic symbol uses four dependencies: *A* (address), *G* (AND), *EN* (enable), and *C* (control). Input *G* 1 is to be considered ANDed with 1*EN* and 1*C* 2 because *G* 1 has a 1 after the letter *G* and the other two have a 1 in their label. The *EN* dependency is used to identify an enable input that controls the data outputs. The dependency *C* 2 controls the inputs as indicated by the 2*D* label. Thus, for a write operation, we have the *G* 1 and 1*C* 2 dependency ($CS = 0$), the *C* 2 and 2*D* dependency ($WE = 0$), and the *A* dependency, which specifies the binary address in the four address inputs. For a read operation, we have the *G* 1 and 1*EN* dependencies ($CS = 0, WE = 1$) and the *A* dependency for the outputs. The interpretation of these dependencies results in the operation of the memory as listed in the function table of Fig. 11.18.

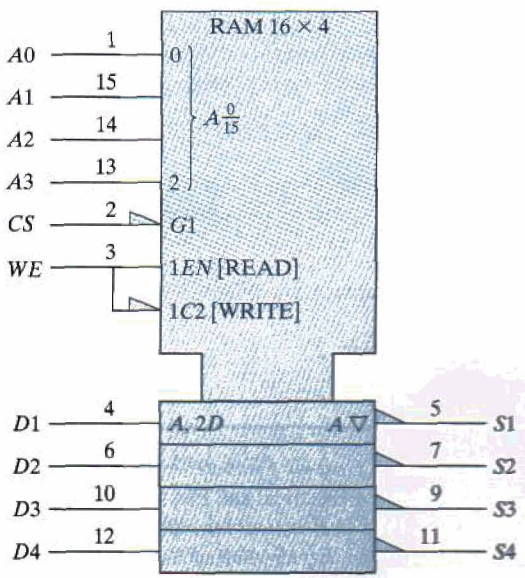


FIGURE 12.15
Graphic symbol for 16 × 4 RAM, IC type 74189

PROBLEMS

12.1 Figure 11.1 shows various small-scale integration circuits with pin assignment. Using this information, draw the rectangular-shaped graphic symbols for the 7400, 7404, and 7486 ICs.

12.2 Define the following in your own words:

(a) Positive and negative logic.
(b) Active high and active low.
(c) Polarity indicator.
(d) Dynamic indicator.
(e) Dependency notation.

12.3 Show an example of a graphic symbol that has the three Boolean dependencies—G, V, and N. Draw the equivalent interpretation.

12.4 Draw the graphic symbol of a BCD-to-decimal decoder. This is similar to a decoder with 4 inputs and 10 outputs.

12.5 Draw the graphic symbol for a binary-to-octal decoder with three enable inputs, $E1$, $E2$, and $E3$. The circuit is enabled if $E1 = 1$, $E2 = 0$, and $E3 = 0$ (assuming positive logic).

12.6 Draw the graphic symbol of dual 4-to-1-line multiplexers with common selection inputs and a separate enable input for each multiplexer.

12.7 Draw the graphic symbol for the following flip-flops:

(a) Negative-edge-triggered D flip-flop.
(b) Master–slave RS flip-flop.
(c) Positive-edge-triggered T flip-flop.

12.8 Explain the function of the common control block when used with the standard graphic symbols.

12.9 Draw the graphic symbol of a four-bit register with parallel load using the label $M1$ for the load input and $C2$ for the clock.

12.10 Explain all the symbols used in the standard graphic diagram of Fig. 12.12.

12.11 Draw the graphic symbol of an up–down synchronous binary counter with mode input (for up or down) and count-enable input with G dependency. Show the output carries for the up count and the down count.

12.12 Draw the graphic symbol of a 256 × 1 RAM. Include the symbol for three-state outputs.

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