Altium Designer

Module 12: Design Rules

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Module Seq = 12

12.1 Design rules and design rule checking

In Altium Designer, design rules are used to define the requirements of your design. These rules cover every aspect of the design – from routing widths, clearances, plane connection styles, routing via styles, and so on. Rules can be monitored as you work and you can also run a batch test at any time and produce a DRC report.

Altium Designer design rules are not attributes of the objects; they are defined independently of the objects. Each rule has a scope that defines which objects it must target.

Rules are applied in a hierarchical fashion, for example, there is a clearance rule for the entire board, then perhaps a clearance rule for a class of nets, then perhaps another for one of the pads in a class. Using the rule priority and the scope, the PCB Editor can determine which rule applies to each object in the design.

This section describes how design rules are defined and how to check for design rule violations.

12.1.1 Adding design rules

Design rules are defined in the *PCB Rules and Constraints Editor* dialog that is displayed by selecting **Design » Rules**.

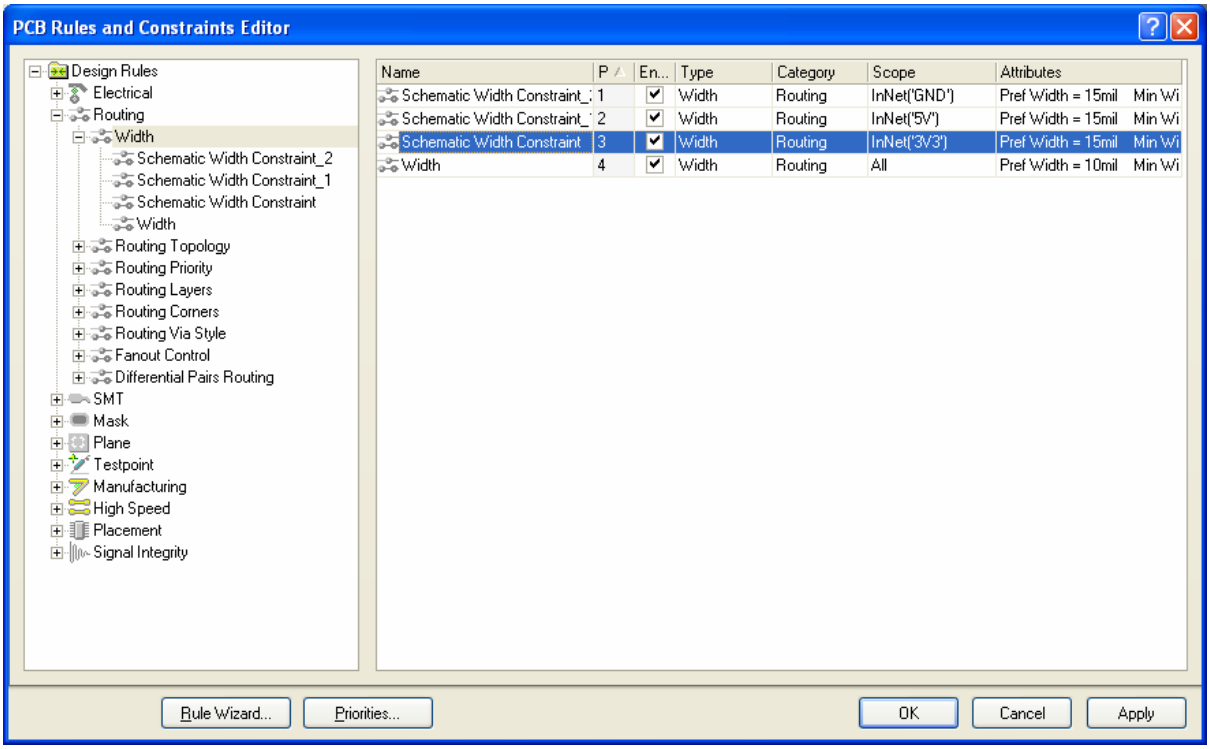

Figure 1. PCB Rules and Constraints Editor dialog.

To set up a design rule:

1. Click on the ⊞ to expand the required rule category in the tree on the left.
2. Click on the ⊞ next to the rule kind to display the rules of that kind that have been defined. Notice how in Figure 1 the tree is expanded to show the four Width rules.
3. Click on a specific rule to display the properties of that rule.
4. Right-click on a rule kind to add a new rule of that kind.

- You can use the PCB Rules and Violations panel to see the objects targeted by a rule.
- Alternatively, right-click on an object in the workspace and select **Applicable Unary Rules** or **Applicable Binary Rules** to work out what rules are being applied to an object(s).

Figure 2. Unary rules dialog showing what's applied to a component

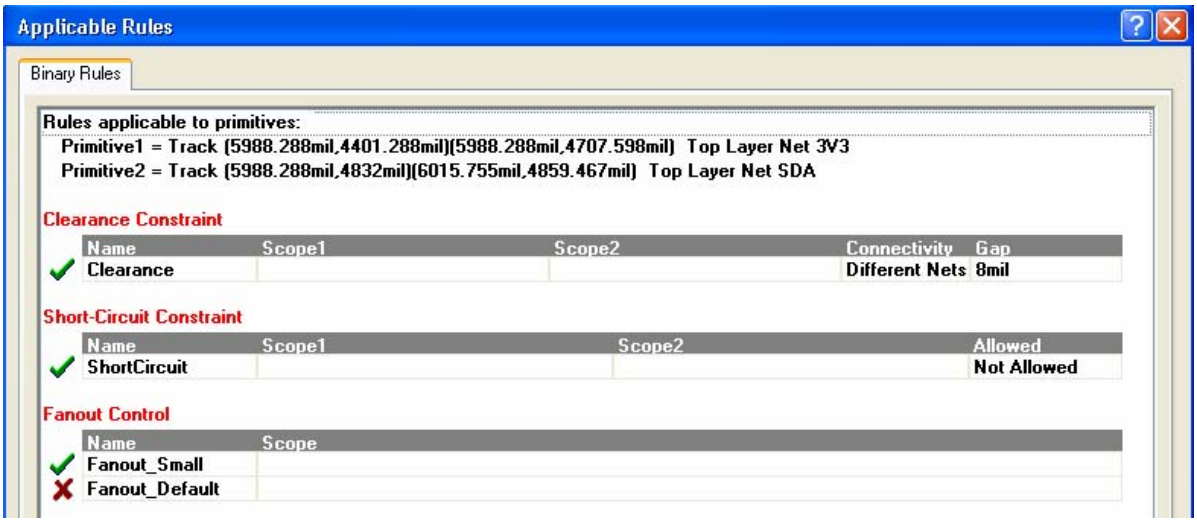

Figure 3. Binary rules dialog showing what's applied between two nets

12.1.2 Design rules concepts

To effectively apply the design rules, the concepts of rule type, object set, query and priority need to be understood.

12.1.2.1 Rule type

There are two types of design rules – unary and binary.

Unary design rules

These apply to one object, or each object in a set of objects. For example, Width Constraint.

Binary design rules

These apply between any object in the first set to any object in the second set. Binary rules have two object set sections that must be configured. An example of a binary rule is the Clearance rule – it defines the clearance required between any copper object in the first set and any copper object in the second set, as identified by the two rule queries.

12.1.2.2 Object set

This refers to the group of objects that the rule applies to. The scope of the object set is determined by the rule Query.

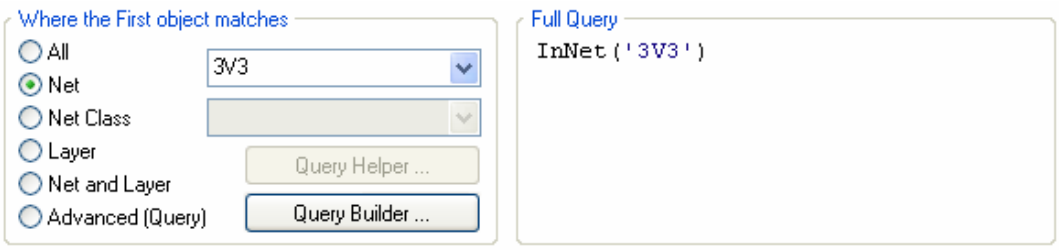

Figure 4. The scope of the rule defines the objects it targets. This rule targets the 3V3 net.

12.1.2.3 Rule Query

The Query is a description of the objects that this rule applies to. The Query can be typed in directly, it can be constructed automatically using the controls on the left of the Full Query edit field, or it can be constructed using the Query Builder.

For more information on queries, refer to the article, *An Insiders Guide to the Query Language.*

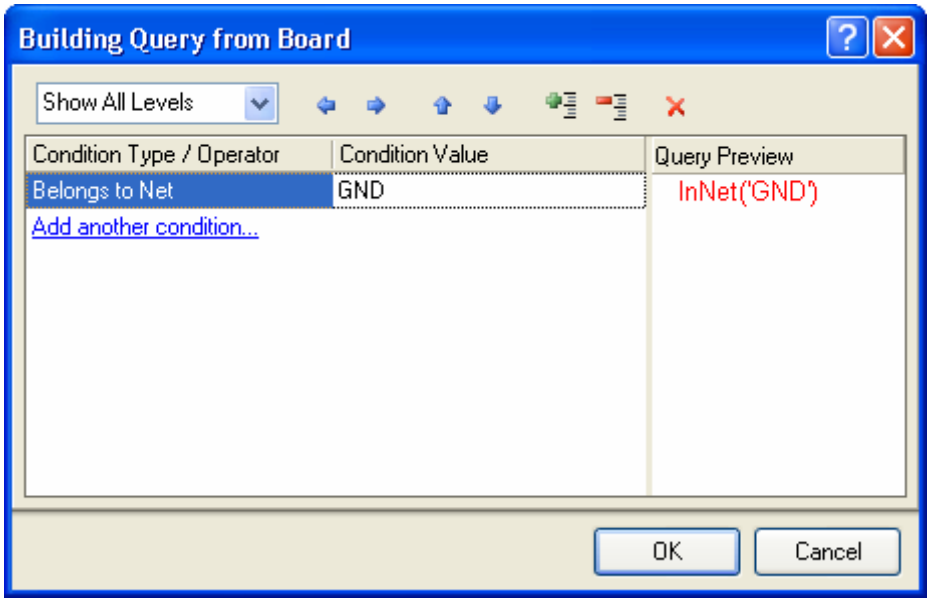

Figure 5. Use the Query Builder to construct the rule query.

12.1.2.4 Query errors

If you are typing the query in and you make a mistake, for example, you leave off a bracket, a message will appear warning that there are errors when you attempt to close the Rules dialog. It is important to resolve these errors, as if you do not, the on-line DRC can become very slow. Rules that have a query error have their name displayed in red in the tree on the left of the dialog.

12.1.2.5 Setting the rule priority

The priority, or order that the rules are tested to determine the applicable rule, is user-defined. When a new rule is added it is automatically set to the highest priority for rules of that kind. It is essential that the priority is set appropriately for them to be applied correctly. To get to the Priorities dialog, click on the **Priorities** Button. Before pressing this button you need to set the area of design rules you wish to alter, like for example clearance rules, width rules to only display rules of this type.

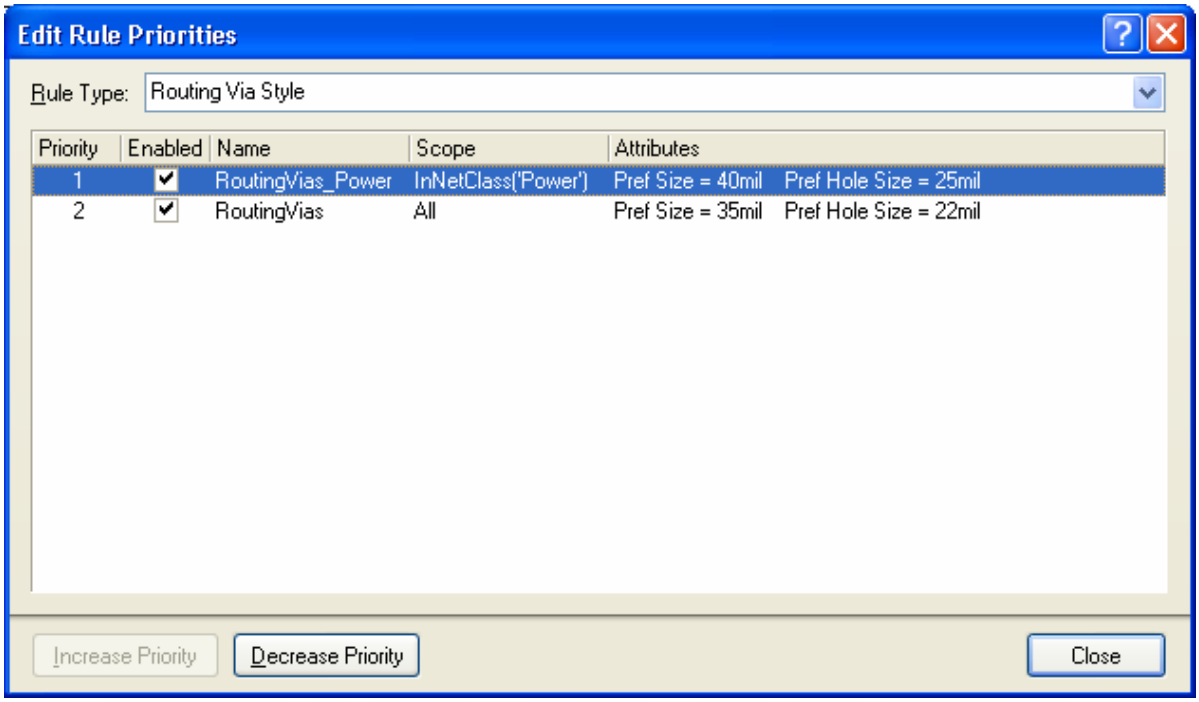

Figure 6 After adding a rule, make sure that the priority is appropriate

In Figure 6 a routing via style rule for the NetClass Power exists. Note that it has a rule priority of 1 (the highest priority). If it had a priority lower than the RoutingVias rule, which has a scope of All, it would never be applied.

12.1.3 How rules are checked

Design rules are checked by the Design Rule Checker (DRC) either online as you work, or as a batch process (with an optional report). The batch mode can be run at any time, and it is good design practice to run it as a final verification check when the board is completed.

12.1.3.1 Online DRC

If the Online DRC option is turned on, all DRC violations are marked as you create them. This is especially helpful when manually routing to immediately highlight clearance, width and parallel segment violations.

Checking the **Online DRC** check box in the **General** page of the *Preferences* dialog (**Tools » Preferences**) turns on the Online DRC.

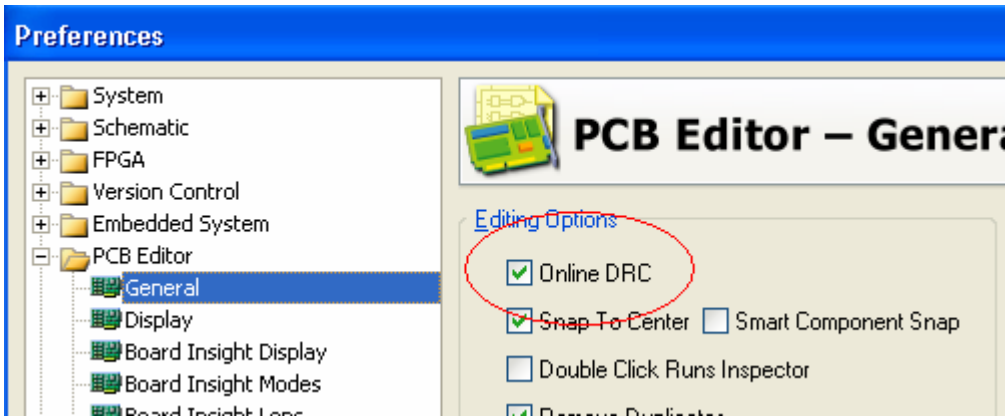

Figure 7. Online DRC tick box in the preferences

Each rule is then individually enabled for online and/or batch checking in the **Rules to Check** page of the *Design Rule Checker* dialog, as shown in Figure 8 (select **Tools » Design Rule Check** from the menus). Enable the online checkbox for each rule that you want to have automatically monitored as you work.

DRC errors display in the color chosen in the **Board Layers and Colors** tab of the *View Configurations* dialog, when the **Show** checkbox is enabled. Also DRC markers can be set via **Tools » Preferences » DRC Violations Display**. From here there are new styles and display options to be set to show an icon based view of a DRC violation.

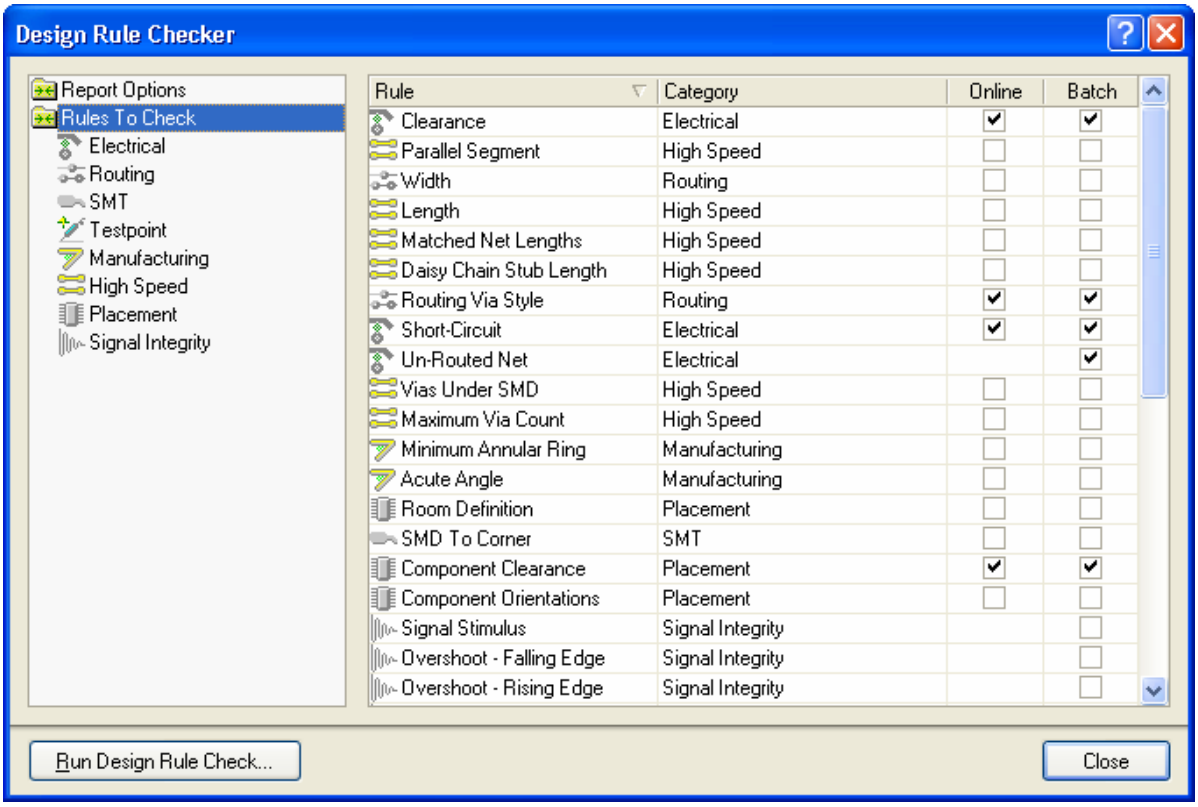

Figure 8. Configure when each rule is to be checked in the Design Rule Checker dialog.

12.1.4 Where rules apply

12.1.4.1 Routing rules

Rule Class	Manual Route	Auto Route	Online DRC	Batch DRC	Other
Clearance Constraint	Y	Y	Y	Y	Place Polygon
Routing Corners	Y				Specctra DSN export
Routing Layers		Y			
Routing Priority		Y			
Routing Topology		Y			
Routing Via Style	Y	Y			
SMD Neckdown Constraint		Y	Y	Y	
SMD To Corner Constraint			Y	Y	
SMD To Plane Constraint			Y	Y	
Width Constraint	Y	Y	Y	Y	Physical connected copper

Table 1. Routing rules

12.1.4.2 Manufacturing rules

Rule Class	Auto Route	Online DRC	Batch DRC	Output Generation	Other
Acute Angle Constraint		Y	Y		
Hole Size Constraint		Y	Y		
Layer Pairs		Y	Y		Manual route
Minimum Annular Ring		Y	Y		
Paste Mask Exp				Y	
Polygon Connect Style					Place Polygon
Power Plane Clearance	Y			Y	Internal Planes
Power Plane Connect Style	Y			Y	Internal Planes
Solder Mask Exp				Y	
Testpoint Style	Y	Y	Y	Y	Find Testpoint
Testpoint Usage	Y	Y	Y	Y	Find Testpoint
Hole to Hole clearance		Y	Y		
Minimum Solder Mask Silver		Y	Y		
Silkscreen Over Component Pads		Y	Y		
Net Antennae		Y	Y		
Silk to Silk Clearance		Y	Y		

Table 2. Manufacturing Rules

12.1.4.3 High Speed rules

Rule Class	Auto Route	Online DRC	Batch DRC	Output Generation	Other
Daisy Chain Stub Length		Y	Y		
Length Constraint		Y	Y		
Matched Length Nets		Y	Y		Interactive length tuning tool
Differential Pairs		Y	Y		Interactive Differential pair length tuning tool
Maximum Via Count		Y	Y		
Parallel Segment		Y	Y		
Vias Under SMD		Y	Y		

Table 3. High Speed Rules

12.1.4.4 Placement rules

Rule Class	Auto Route	Online DRC	Batch DRC	Output Generation	Other
Component Clearance Constraint		Y	Y		Cluster Auto Placer
Component Orientation					Cluster Auto Placer
Nets To Ignore					Cluster Auto Placer
Permitted Layers					Cluster Auto Placer
Room Definition		Y	Y		Arrange within room

Table 4. Placement Rules

12.1.4.5 Signal Integrity rules

All Signal Integrity rules apply only to Signal Integrity Analysis and Batch DRC.

12.1.4.6 Other design rules

Rule Class	Auto Route	Online DRC	Batch DRC	Output Generation	Other
Short Circuit Constraint		Y	Y		
Unconnected pin Constraint		Y			
Unrouted Net Constraint		Y	Y		

Table 5. Other Design Rules

12.1.5 From-tos

The PCB Editor allows commands to operate on a particular pin-to-pin connection in a net, in a different manner to the rest of the net. A specific pin-to-pin connection is defined as a *from-to* Commands will operate on a from-to if a design rule for that from-to has been defined.

From-tos are created using the From-To Editor. Select **From-To Editor** in the PCB panel to display this editor.

The top region of the panel lists all nets in the design. Click on a net to list that nets nodes in the Nodes on Net region of the panel. When you click on any two nodes in the net (use CTRL+Click to multi-select), the **Add From To** button will be enabled. When this is clicked, the new from-to will appear in the From-Tos on Net section of the panel.

The **Generate** button allows you to create from-tos for a complete net in the pattern of the selected topology.

12.1.6 Exercise – Setting up the design rules

This exercise looks at setting up the required design rules.

1. Using the Temperature sensor project PCB document, confirm that the basic (The ALL rule) clearance constraint design rule is set to 8mils.
2. Add a clearance constraint to keep polygons at least 15mils from other copper objects. To do this:
   - add a second clearance constraint rule
   - for the First Object Matches query, type in the query **`InPolygon`**
   - leave the Second Object Matches query as **`All`**
   - set the minimum clearance to 15mils
   - set the rule name to `Clearance_Polygon`.
3. Confirm that basic (The ALL rule) Board scope width constraint is set to 8 mils (all three settings).
4. For the three power nets on the schematic included parameter set objects that defined the width rule required for these nets. Confirm that a width constraint has been created for each of these nets with a width of 15 mils.
5. Edit the Routing Via Style design rule, setting the via diameter to 35 and the hole size to 22 (all three settings).
6. Save the board.

12.1.7 Design Rule Checking

- The Design Rules Checking (DRC) functions are provided to check that your design conforms to the design rules.
- There are both Online and Batch DRC functions.
- A design should only be submitted for manufacturing when all DRC violations have been resolved.
- DRC violations can be located using its own PCB Rules and Violations panel.

12.1.7.1 Design Rules Check report

The DRC report is often referred to as the Batch DRC. This performs design rules checks based on the options selected and marks any violations found. Selecting the **Tools » Design Rule Check** menu command runs the DRC. This displays the *Design Rule Checker* dialog shown in Figure 9.

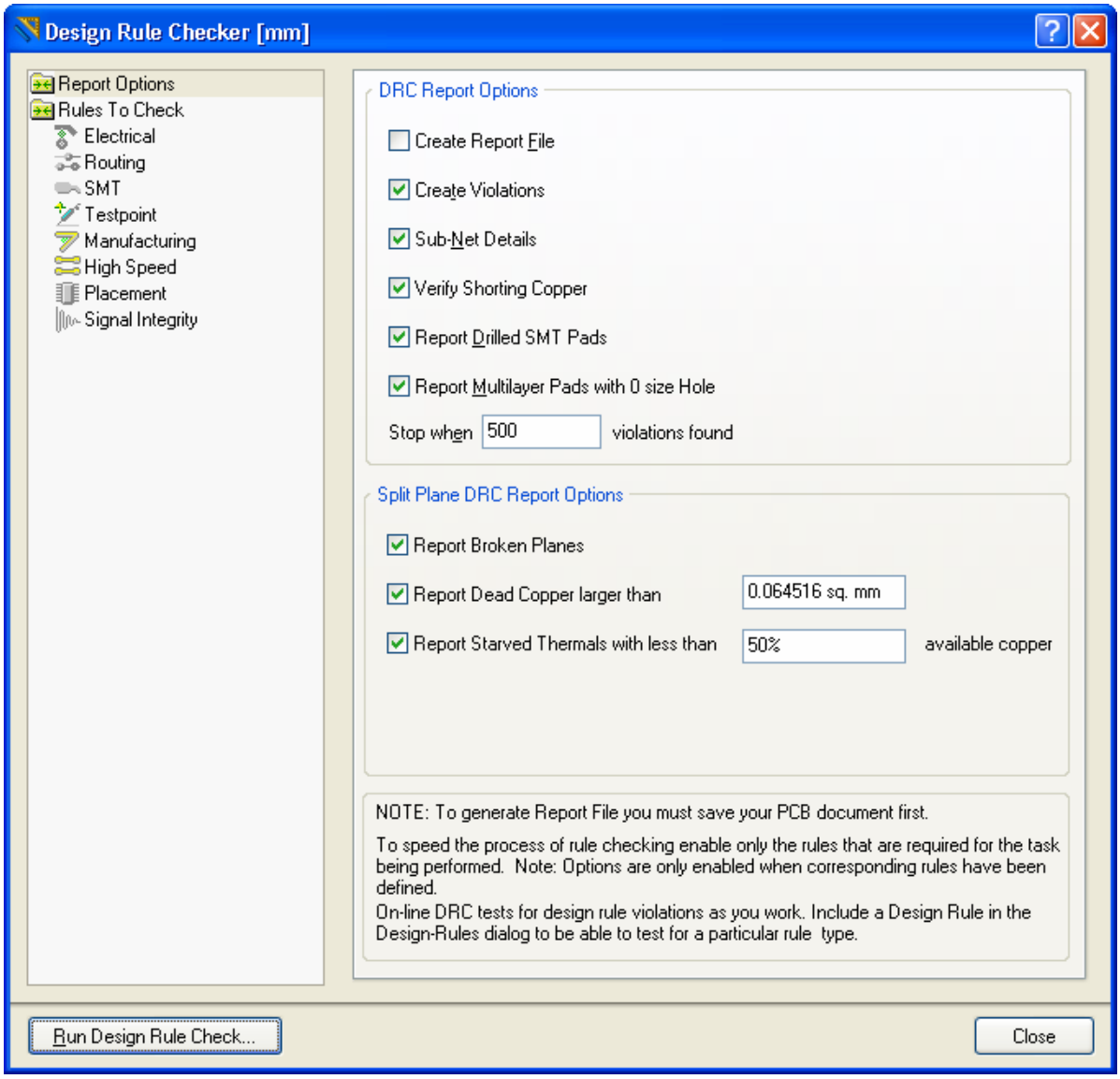

Figure 9. Report Options in the Design Rules Checker dialog

The Rules to Check sections of this dialog enables you to select which design rules the DRC will check for violations. Click on the **Run Design Rule Check** button to start a DRC check on the

PCB. A report (.DRC) is generated and displays in the Text Editor if the Create Report File option is enabled.

12.1.7.2 Locating design rule violations

The following features are provided to locate and interpret DRC violations:

- PCB Rules and Violations panel. Select [All Rules] in the Rule Class section of the panel to list all violations. Click once on a violation to display it (and mask all other objects). Double-click to open the *Violations Details* dialog.
- The Message panel. This panel lists all violations detected in the design. Double-clicking on most message types will jump you to the violation (but will not mask like using the panel).
- The DRC report. This report is generated if the **Create Report File** option is enabled in the *Design Rule Checker* dialog.
- The right-click Violations menu entry. Right-click on a violation and select Violation to display information about the violations on that object, select a violation entry to open the *Violation Details* dialog.
- **Shift + V** shortcut while hovering the mouse over the top of a violation.

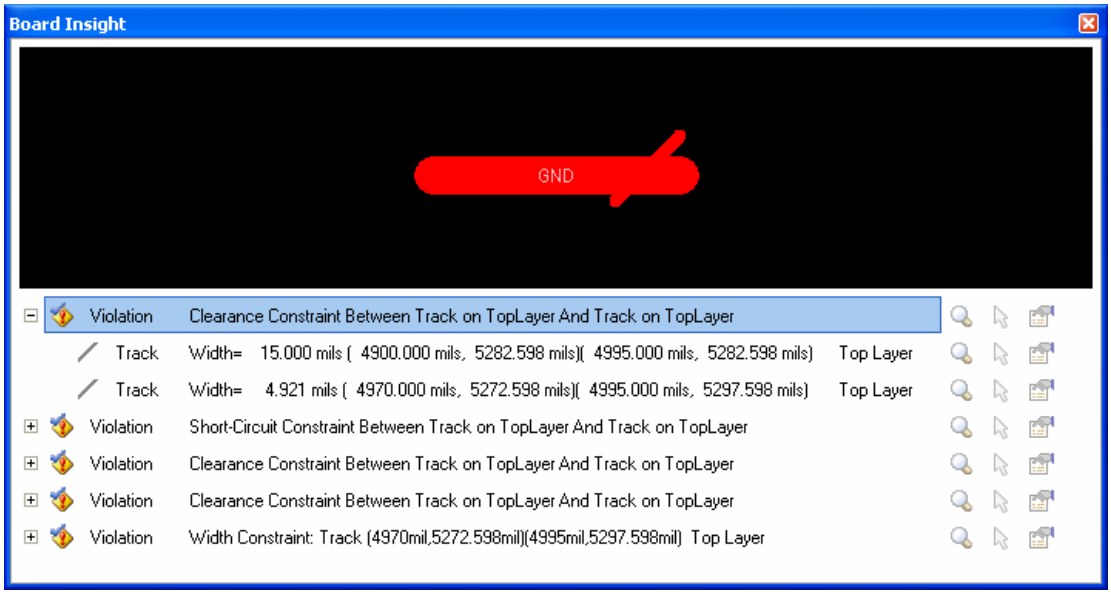

Figure 10. Using shift + v to display violation in board insight

12.1.8 Exercise – Running a DRC

In this exercise, you will run a Design Rule Check (DRC) to check for PCB design violations.

1. Run a DRC and review the violations in the PCB Rules and Violations Panel. There should be at least three violations as the pads in J200, the power connector, have holes that are larger than the maximum permitted by the default hole size constraint rule.
2. Change the rules to suit the requirements of the connector. A suggestion for an effective rule in this case would be to use a rule that targets the footprint name. The query to use in this case would be, **HasFootprint('PWR2.5')**
3. Create a new rule for Hole size in the manufacturing section and set to the query in step 2. Make sure the priorities are setup correctly after creating this rule. Also make sure there are two rules at this stage. One should be set to All scope.
4. Note that the Unrouted Net design rule is used to check for nets that have not been completely routed, if your board is not routed yet you should disable checking of this rule in the *Design Rule Checker* dialog.

5. On top of above the is also some manufacturing rules checked that at this stage are causing errors that we'll fix later on. These include the silk to silk clearance, silk over component pads and min solder mask sliver
6. To make sure the rule added in step two is working correctly right click on the offending pad found in step 1 and select **Applicable Unary Rules**. It should be using the new rule for the offending pads and the original rule for any other pads.
7. Save the board.

> **Note:** Make sure that all used layers are on when you are trying to resolve design rule violations. Keep in mind that with the default settings, the DRC stops after detecting 500 errors (configured in the *Design Rule Checker* dialog).