

Chapter 9

Towards Integrated Power Electronics

9.1. The integration

9.1.1. Introduction

Power electronics is a branch of electronics which uses semiconductor devices for making systems to transform the form, size and/or frequency of waves that carry electrical energy. These operations are carried out with powers far greater than those encountered in linear electronics. For reasons of efficiency, but also because they cannot safely remove a large fraction of the flowing power, these semiconductor devices work between two states, either with a current of the magnitude of the nominal current and a very low voltage at the terminals, or with a voltage close to the nominal voltage but with a current as low as possible. Furthermore, to achieve the necessary conversions, these components must move from one state to another during little dissipative transitions. All these constraints lead to a switching operation in which the role of the semiconductor components can be like that of an operating switch between two states: opened or closed. Thus, the important characteristics of these devices are blocking voltage (a few volts to a few thousand volts), the passing current (a few amps to a few hundred amps), the voltage drop during on-state operation and switching times which set the losses of conduction and commutation.

Since the first devices, improving performances of power components is achieved in general by:

- increased voltage and current ratings of devices;
- optimizing performances during the commutation;
- improved security areas;
- greater simplicity of command.

These improvements are the consequences of technological progress in the field of microelectronics, development of new structures and specific studies carried out in the field.

Although the performances to optimize for power components are different from those of integrated circuits, the explosion of microelectronics had a significant impact on the development of power components. In terms of power components, the first trend was mainly an increase in the ratio $V.A/mm^2$, while for integrated circuits, progress corresponds to an improvement in the ratio of the number of transistors/ mm^2 . Over the past twenty years, the microelectronics industry has developed significantly with major research effort towards reducing dimensions. Although evolution has taken place in different directions, a transfer of technological progress and means of production was made from the field of integrated circuits to the power components, as shown in Figure 9.1.

In terms of structures, a large number of power components are developed from devices used for the first time in the field of signal processing. 15 years elapsed between the first introduction by the FAIRCHILD Company in 1954 of a bipolar transistor with silicon planar technology and the arrival of the first transistor adapted for use in power. The penetration of MOS transistors in the field of power took place within the same time span as the development of the first VMOS power transistor in 1976. The first realization of a silicon-based MOS transistor was conducted in 1960. This time span saw the adaptation of electrical devices for the application of power requirements. This introduction of MOS technology in the field of power devices is the decisive step that marked a break in the evolution of power components in terms of both performances and structures. The reduction in size of VDMOS structures for low and medium voltage led to a significant reduction of resistance during the on - state operation. For the first time, reducing the size of a power component led to an improvement in its performances, thereby joining the mode of development of integrated circuits. This reduction in size has been made possible by improved manufacturing technology processes from microelectronics, such as double diffusion based on the creation of polycrystalline silicon grids. These devices have benefited from research progress in the field of microelectronics, and sometimes production lines used for older generations of integrated circuits. These works on MOS power components then allowed the rapid development of IGBT, which now constitutes the major axis of power components, and the study of new grid MOS devices such as

MCT, BRT, EST, etc. This has naturally led to the development of power integrated circuits.

These integrated power circuits are an extension of the integration of logic circuits by adding an element of power to signal processing circuits. As in any development in power semiconductor devices, the first achievements were applications with low voltage and low current.

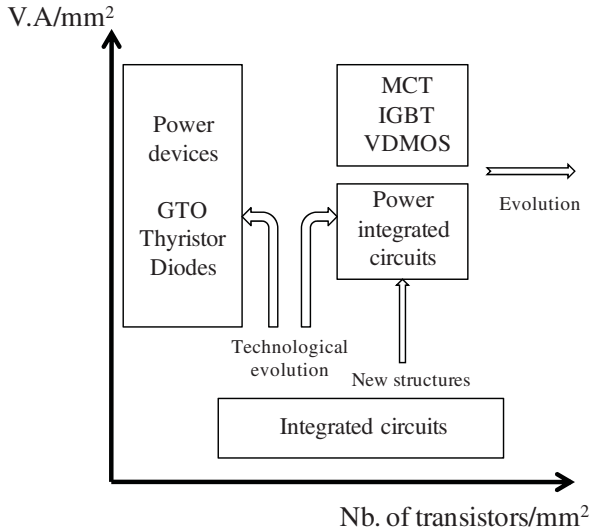


Figure 9.1. *Impact of technological advances in microelectronics on power components*

Currently, only a portion of applications in the domain of very low power (automotive electronics) use integrated power circuits. However, the majority of applications on the power grid can also enjoy the benefits of integration. We will present as a first step the main methods of monolithic integration, and we will then outline the best suited strategies for integration of new functions for the power electronics of the future.

9.1.2. *The different types of monolithic integration*

The strategy for integrating power functions can be handled in two ways: either by promoting the functionality compared to power elements, by promoting the optimization of the power part [CHA 95a, SAN 99a]. The “Smart Power” and HVIC (high voltage integrated circuit) devices are more relevant to the first approach and

are made from technologies of integrated circuits (CMOS or BiCMOS). The devices based on the functional integration of the second approach are based on power component technologies.

9.1.2.1. *Power integrated circuits*

Technological advances in the field of microelectronics have made it possible to integrate into a single chip, power components and logic and analog circuits to serve as command, diagnosis and protection. Thus, the first power integrated circuits for low voltage applications emerged in 1985, fifteen years after the initial integration of signal components.

These power integrated circuits were developed under two names, “Smart Power” circuits and HVIC circuits [RUM 85]. The difference between the two families is essentially linked to the power element and to the ranges of current and voltage addressed:

- for “Smart Power”, the power component alone is generally vertical (VDMOS);
- for HVIC, power components are lateral and very often of MOS type (LDMOS).

HVIC are multi-output circuits able to support up to a few hundred volts but presenting very low current densities inherent to the lateral components used. In contrast, “Smart Power” components, more efficient in terms of current densities, and may pass currents of several amps.

The study of insulation techniques between the low voltage area and the power elements was one of the most important challenges of this family of components (Figure 9.2). The self-insulation, the junction insulation and the dielectric insulation are the main solutions used today. However, the dielectric insulation is still costly and, despite its effectiveness, it is still reserved for applications requiring a very strong insulation.

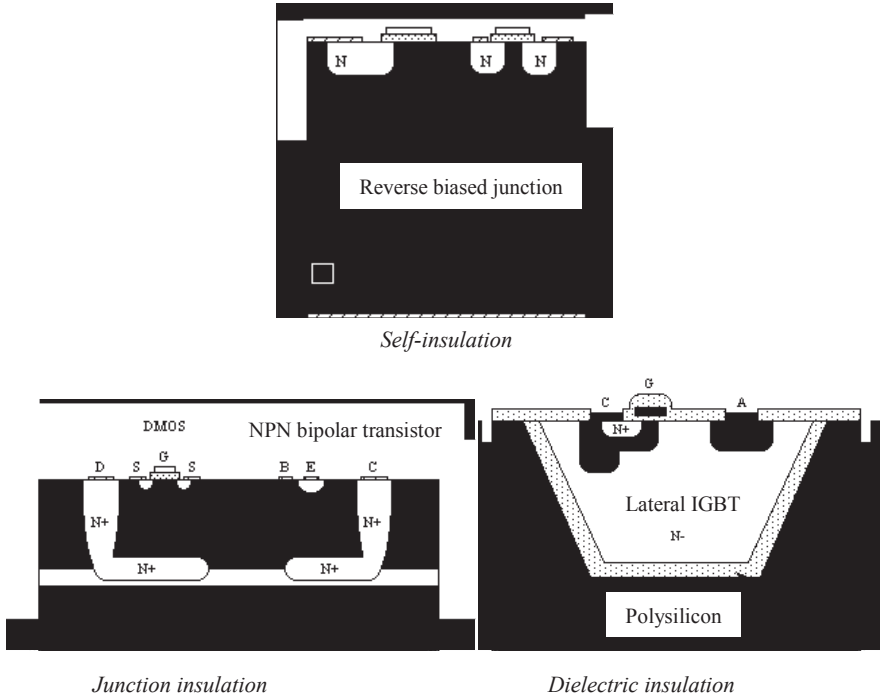


Figure 9.2. Insulation techniques for vertical and lateral power components

The first generations of power integrated devices *Smart Power* were carried out with a technology which does not allow very large densities of integration (Figure 9.3). The new generations of “Smart Power” components, Smartmos 5 (Motorola), BCD5 (ST-Microelectronics), SIPMOS (Siemens) are designed from VLSI technologies which must be able to allow for the design of power components able of support voltages in the order of 100 V, using insulation techniques developed in recent years (by junction insulation, dielectric insulation).

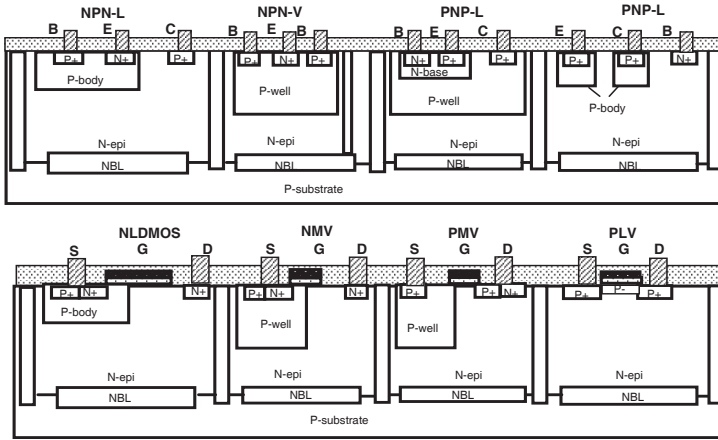


Figure 9.3. Structures and standard elements on Smart Power Technology

These technologies make it possible to integrate complex digital circuits (DSP) and micro-controllers. While in the first Smart Power circuits the surface of the power component was often greater than that of the integrated circuit, the trend is reversed in the new power integrated circuits, which are characterized by the integration of new functionalities. This trend is accompanied by a reduction of design rules and advanced technologies. Figure 9.4 shows a block diagram of this type of circuit that can be described as “new Smart Power”. It is divided into three parts: the interface circuits, control circuits and signal processing, and the power element. In terms of interface circuits, the trend is to replace the bipolar circuits with BICMOS circuits, for more desirable performances. The signal processing circuit functions correspond to CMOS with low power consumption and high density of integration. The power devices are generally based on DMOS technologies to achieve lateral structures (LDMOS), or vertical structures (VDMOS). In view of increasing functionality, memory can also be integrated. The BCD technologies (Bipolar, CMOS and DMOS) allow considerable flexibility in order to achieve the different types of above mentioned circuits.

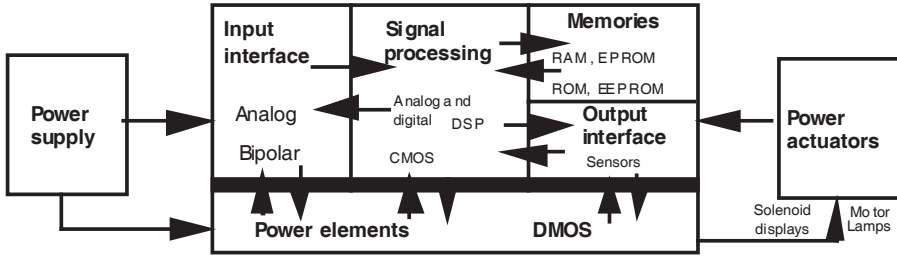


Figure 9.4. Block diagram of a Smart Power circuit

The main areas of application of these power integrated circuits are portable equipments telecommunications and automotive electronics. The development of these circuits is mainly supported by automotive applications such as ignition, injection, ABS, lighting, command of small motors (lift windows, air conditioning). The optional level of integration, the range of power and hence the power component are then functions of the proposed application.

The technologies developed for integrated logic and analog circuits with low voltages were utilized a few years after power integrated circuits (Figure 9.5). This different development is linked, on the one hand, to the important work in the field of integrated circuits supported by an important market, and on the other hand by the complexity of integrated circuit manufacture for larger power, where insulation and voltage strength aspects must be accounted for. Today, this gap is reduced to only one generation, while lengths of MOS transistors channels reach $0.6\ \mu\text{m}$ for power integrated circuits, against $0.35\ \mu\text{m}$ or $0.18\ \mu\text{m}$ for VLSI (*very large scale integration*) electronics. This development can allow an estimation of trend for the future of integrated power circuits. This evolution towards an increased degree of integration leads to integrated systems on a single chip in the field of low power.

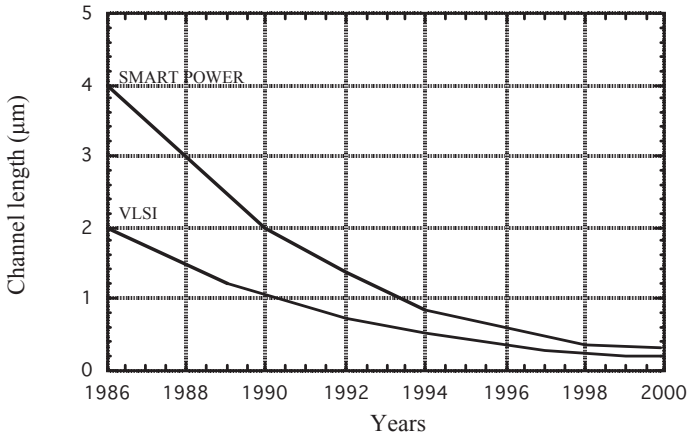


Figure 9.5. Comparison between the evolutions of “Smart Power” and VLSI technologies

9.1.2.2. Functional integration

The concept of functional integration in power electronics has emerged from the operating principle of the first power devices, such as thyristors and especially triacs [BOU 02, BOU 04, GEN 64a, GEN 64b, PEZ 97a] (see Figure 9.6). In this mode of monolithic integration, the function is made by surface interconnections but also by many electrical interactions between different semi-conductive areas which must be carefully designed and sized.

Without reaching the complexity of functions obtained with “Smart Power” components, devices made by functional integration can obtain specific features for applications of control and protection by combining several basic elements [CHA 95b, SAN 97, SAN 99b, MAR 00]. This mode of integration, based on the vertical power components ability to withstand voltages of several hundred volts, and transit currents of several amps, is better suited to the development of new functions for power applications of medium power connected on electrical energy distribution networks. At the moment, functional integration is evolving both in terms of designing new functions of monolithic power and on developing new technological solutions.

STMicroelectronics, for example, uses this concept of functional integration in the development of new power functions, under the name ASD™ (application specific discrete). The ASD™ is an approach responding quickly to the specifications imposed by a customer [PEZ 95a].

9.1.2.2.1. The AC Switch™ structure

The extension of functional integration enables the development of new command and switch protection functions [PEZ 95b, PEZ 96, PEZ 97b, PEZ 97c], with advantages over discrete components (volume reduction and performances). Figure 9.6 represents an AC Switch™ structure developed by STMicroelectronics in Tours. This structure is well suited for grid applications.

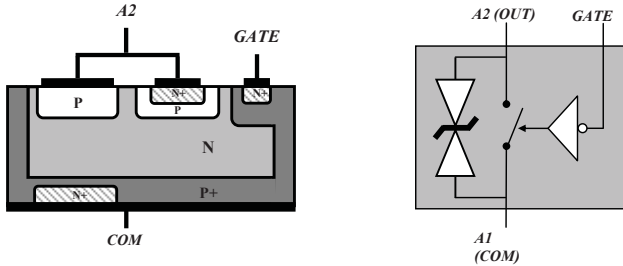


Figure 9.6. Cross-section view of an ACS structure and electric symbol (patented structure)

Unlike the triac, two thyristors with anode trigger are managed by a single command. This command, on top of the chip, is referenced in relation to the underside of the chip. This allows a decoupling of the two thyristors (improves dV/dt strength) and facilitates the use and mounting of chips onto a single base (such as a radiator).

The technology used is a planar technology with better reliability and lower manufacturing cost. Moreover, the use of suburb P+ areas ensures the robustness of the device in avalanche, and avoids the use of a varistor.

However, the operation under negative command confines the use of the AC Switch to two quadrants (Q2 and Q3 of triac). One of the main strengths of this structure is the design of its trigger which is isolated from the power part by the junction. The reaction of the trigger on the command circuit (called “kick back”) becomes low enough to allow the direct command of the trigger by a microcontroller circuit.

9.1.2.2.2. AC Switch™ structures with a predetermined trigger [PEZ 95A] over a half period

The following power structure has a monolithic form in which we find an AC Switch™ with a predetermined trigger, on a half period, which remains automatically conductive on the next period. This device has a sensitive trigger, does

not require a strong boot current, and presents a good immunity against parasitic triggering in terms of dI/dt and dV/dt .

This AC Switch™ consists of a series mounting of two blocks. Each includes a thyristor and an antiparallel diode (Figure 9.7). The first block includes a thyristor with a trigger output. The second block includes a thyristor and a vertical diode in the same substrate. The electrical interaction between these two structures is very strong so that the charges stored during the blocking of the diode are used for triggering the second thyristor (Figure 9.8).

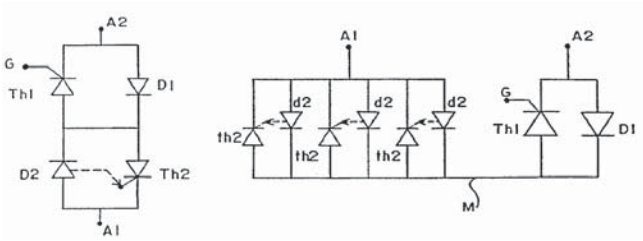


Figure 9.7. Electric schematic and operating principle

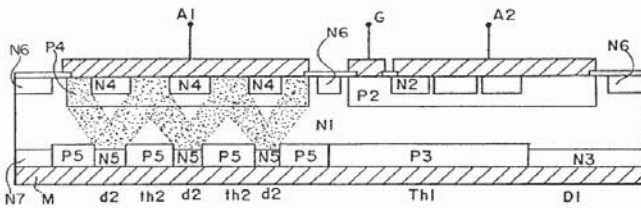


Figure 9.8. Cross-section view of the AC switch device with a predetermined trigger

This power device includes a conventional thyristor ($TH1$) with a trigger electrode (G), and a diode ($D1$) mounted in antiparallel. This diode $D1$ is mounted in series with a second thyristor ($TH2$), which is mounted with a second antiparallel diode $D2$. The structure now has two main electrodes, $A1$ and $A2$ and a command electrode G . Thus, if the electrode $A1$ is polarized positively compared to the electrode $A2$, the current passes between $A1$ and $A2$ through the diode $D2$ and thyristor $TH1$ after applying an order on the thyristor $TH1$. Then the thyristor $TH2$ automatically becomes a conductor during the half period following the conduction phase of the diode $D2$.

The operating principle (see Figure 9.7) and the cross-section view of the structure (see Figure 9.8) highlight the strong electrical interaction between the different structures. This interaction is being used to develop a new feature, which illustrates the potential to create new functions, offered by the mode of functional integration.

9.2. Examples and development of functional integration

Functional integration is not confined to the bipolar structures and multi-layer interactions in silicon. It also applies strongly to other technologies and more particularly to the MOS technology. This gives new lines of components making better use of silicon. The best known state of the art is certainly IGBT. However, many variants have emerged through a process of functional integration. In this part we describe, by example, the functional integration process of a MOS-thyristor function. We then discuss specific functions. The dual thyristor example will be developed to show how, through a process of functional integration, a specific component can be fully established.

9.2.1. *The MOS thyristor structures*

The use of MOS technology for power devices offers a degree of freedom in designing the additional functions of integrated power because they can combine the advantages of both MOS transistors and electrical interactions in the volume. The MOS structures have a high input impedance (considerably simplifying command circuits). However, in standard configurations of vertical MOS structures adapted to power applications, the compromise between on-state resistance and voltage strength limits their use in the range of medium and low powers. To take advantage of this voltage command, research has been undertaken to combine MOS and bipolar structures for “high voltage” applications. The IGBT (insulated gate bipolar transistor) (see Chapter 2), based on this type of association, has undergone an important industrial growth in recent years. The device meets the advantage of a voltage command (via a grid of MOS transistor) and a low on-state resistance linked to the modulation of conductivity inherent to the injection of carriers by the anode structures in the low N- doped region. This approach was then extended to MOS-thyristor associations that are the integration foundation of new power switches.

9.2.1.1. *Ordering the closure of MOS thyristor structures*

In the case of devices such as classical thyristors with a large N-type base, the closure order is carried out through a N-channel MOS transistor that is connected between the cathode and the N base of the PNP structure [BAL 79, JAE 87]. Most of

these devices (known as MOS thyristors or MOS gated thyristors) presented in recent years in the literature are derived from power VDMOS transistors, in which the N^+ drain region is replaced by a P-type region strongly doped to obtain a vertical structure of four thyristor type layers, equipped with an isolated control (Figure 9.9). On this semi-conductive architecture, we can identify a PNP transistor coupled with a NPN transistor, as in a conventional thyristor, and a resistance under short circuit R_{CC} corresponding to the resistance of the P region under the N^+ cathode. In this configuration, the P-type substrate of the MOS transistor is connected to its source region (the thyristor cathode) through this resistance R_{CC} (see Figure 9.9).

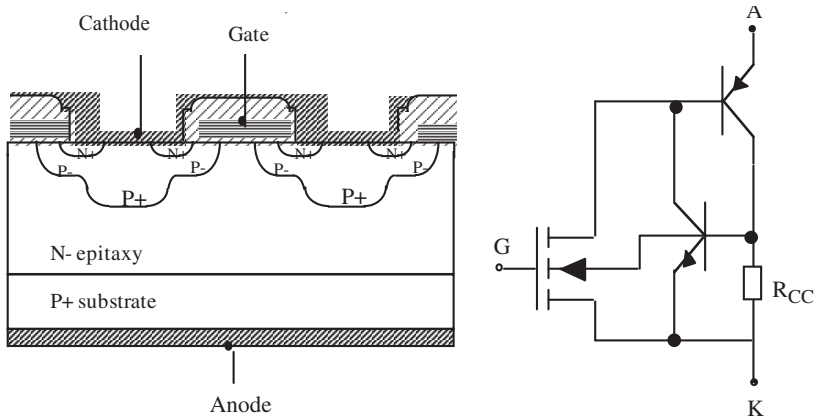


Figure 9.9. Cross-section view and equivalent circuit of the thyristor MOS

Most of the components that were developed derive from VDMOS power transistors or IGBT, and are multi-cellular type. But the concept can be applied to single components designed from thyristor structures, in which the trigger region is replaced by a MOS grid [DAR 86, SAN 90].

9.2.1.2. Orders at the opening of MOS thyristor structures

Several approaches have been proposed to achieve the opening of a thyristor through a MOS transistor. The latter may be placed:

- in series between the semi-conductive region of the cathode and the cathode contact in order to be able to interrupt the current flow;
- between the N- base region of PNP transistor and the N region of the NPN transistor collector to remove the coupling between the two transistors; or

– in parallel with short circuit resistance between the cathode and the base for value variation, thus changing the level of maintenance current in the thyristor.

9.2.1.2.1. MOS transistor placed in series between the semi-conductive cathode region and cathode contact

In the first option (see Figure 9.10), the EST (emitter switched thyristor) [BAL 90], the cathode region (called cathode floating) of the thyristor structure is linked to an outside contact by a MOS transistor, which plays the role of a short circuit. The passage of current between the anode and the external cathode contact occurs only when the MOS transistor is on; the process of opening happens when we block this transistor.

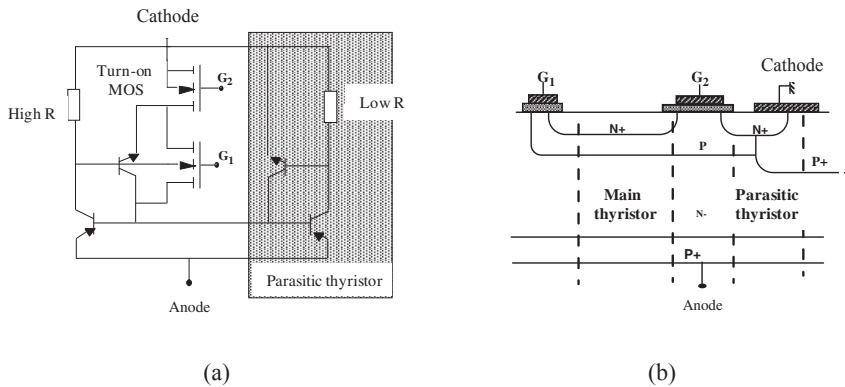


Figure 9.10. An EST device: a) equivalent electrical schematic; and b) a cross-section view

The configuration of this structure places a MOS transistor in series with the thyristor. This contributes to increasing the on-state voltage drop of the device. Indeed, this additional voltage drop becomes a handicap when the current range of the structure is increased. This integration solution leads to the presence of a parasitic vertical thyristor located between the anode and the cathode contact. The device control by the MOS transistor is lost when the thyristor begins to take effect. The closure order is ensured by a MOS transistor placed in an identical pattern to that of the MOS thyristor described in the preceding section.

The solution of setting a MOS in series with a thyristor has also been proposed under the name FIBS (five layers bimos switch) [LIL 92]. This involves a five-layer structure and the integration of several MOS transistors within a single cell (see Figure 9.11). The structure is controlled by 3 integrated MOS transistors, one for the closure and two for the opening. At the opening, the first transistor (MOS A)

connects the cathode of the device to the emitter region of the thyristor. This transistor is therefore placed in series with the thyristor as in the EST structures. To achieve the opening process, we must block the MOS transistor A. From this point on, the device may be likened to a five-layer structure with two junctions to ensure blocking: the main junction (base P base N-) can withstand high voltages, while the other junction made of N- area and P⁺ short circuit cannot support them. At this level, the MOS transistor B can eliminate the breakdown problem if it is passing at the time of deadlock. This MOS section also enables the movement of holes from the anode, via the P⁺ short circuit of cathode.

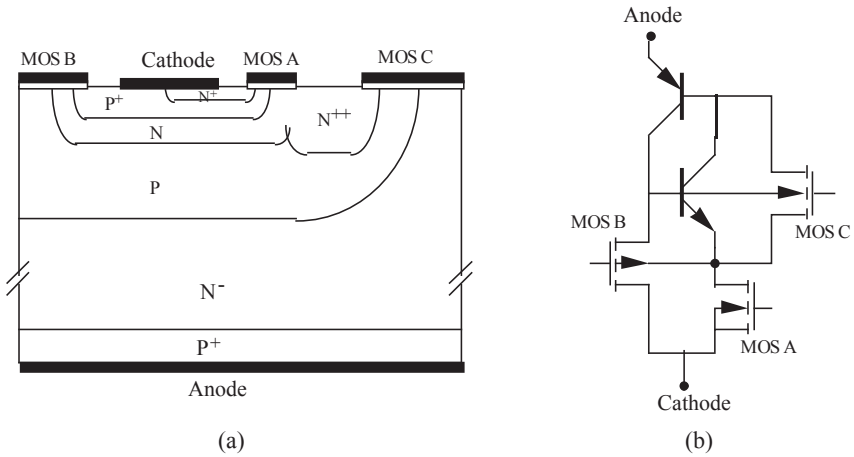


Figure 9.11. FIBS device: (a) cross-section view; and (b) equivalent electrical schematic

In another solution called DMT (depletion mode thyristor) [BAL 88], the MOS transistor is placed in series between the base of the PNP transistor and the NPN transistor collector (see Figure 9.12). Applying a negative voltage on the grid induces a depopulated layer in the region A, located under the base of the NPN and between the grids. The distance between these grids is optimized so that this region is entirely depopulated for grid voltages of 10 volts. Once this area is depopulated, the grid polarization produces a potential barrier, i.e. electrons, thus eliminating the coupling between bipolar PNP and NPN sections. The opening process is that of a PNP bipolar transistor with an open base. Thus, for these devices, the evolution of current during this period of openness presents a “tail current”, corresponding to the evacuation by recombination of charges stored in the base.

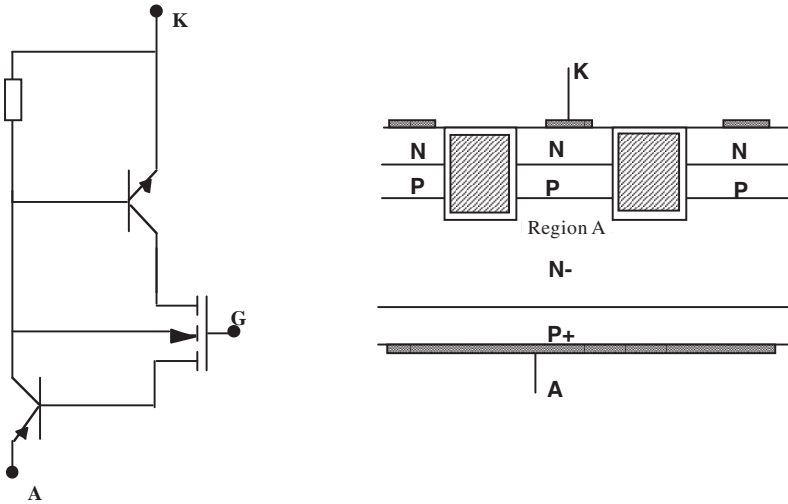


Figure 9.12. *Equivalent electrical schematic and cross-section view of a DMT structure*

9.2.1.2.2. Transistors placed in parallel with short circuit cathode base resistance

Regarding the latter solution, two different approaches using MOS transistors should be distinguished for integration: one is to directly link the two semi-conductive cathode regions and the P base region of the NPN transistor; the other is to connect them via an intermediate semi-conductive region.

Indeed, on the cross-section view of the device shown in Figure 9.13, we note the presence of an additional P^+ region outside of the thyristor section, and linked to the cathode. Applying a negative voltage on the MOS grid induces the formation of a channel on the surface of the N^- region, which connects the P base to the intermediate P^+ region. This helps to reduce the value of the short circuit cathode-base resistance, and will momentarily increase the constant current value of the thyristor section. Opening occurs as soon as this value is higher than its flowed current. This arrangement proposed by BALIGA is known as the BRT (base resistance thyristor) [NAD 91].

It is possible to directly link the P base and the cathode through a MOS transistor acting as an ordered short circuit, thus reducing the value of short circuit resistance between the cathode and base (see Figure 9.14). This decline in resistance increases the value of the constant current, i.e. the nominal current, and allows the device to open for currents less than this maintenance current. This mode of openness is used in devices known as MCT [ART 93, BAU 91, TEM 86].

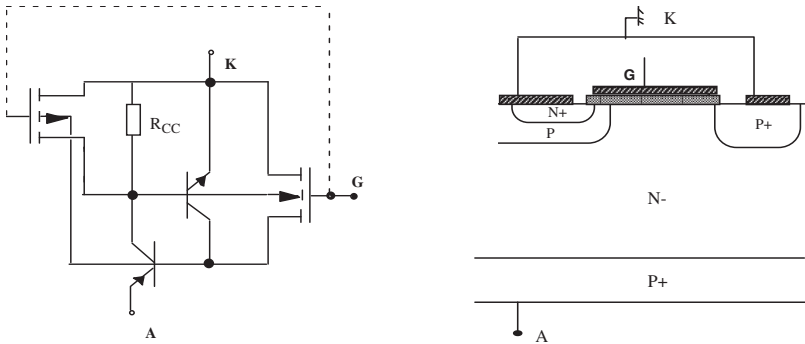


Figure 9.13. *Equivalent electrical schematic and cross-section view of a BRT structure*

The effectiveness of opening these devices is directly linked to the performance of the MOS structures. It is convenient to make small cells in order to get the highest Z/L ratio (width divided by the length of the MOS channel), thus leading to a lowest possible on-state resistance and to an effective emitter-base short circuit. The constraints imposed for these MOS structures, in terms of optimizing the Z/L ratio, are similar to those encountered in the low-voltage VDMOS devices, and as for the latter, the optimization of electrical characteristics are made through deeper integration.

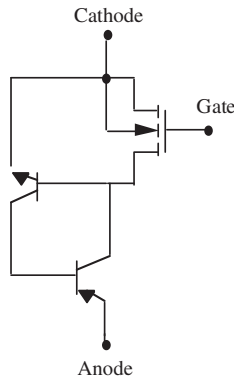


Figure 9.14. *Equivalent circuit of an opening command by emitter-base short circuit*

In the case of the DGMOT structure (dual gate mos thyristor), a lateral MOS structure in a P box allows for short circuiting of the P base with the N^+ emitter (see Figure 9.15). At this level, opening occurs when the maintenance current becomes

greater than the nominal current. Note the adopted technology is similar to that of IGBT because we have a vertical structure with four layers.

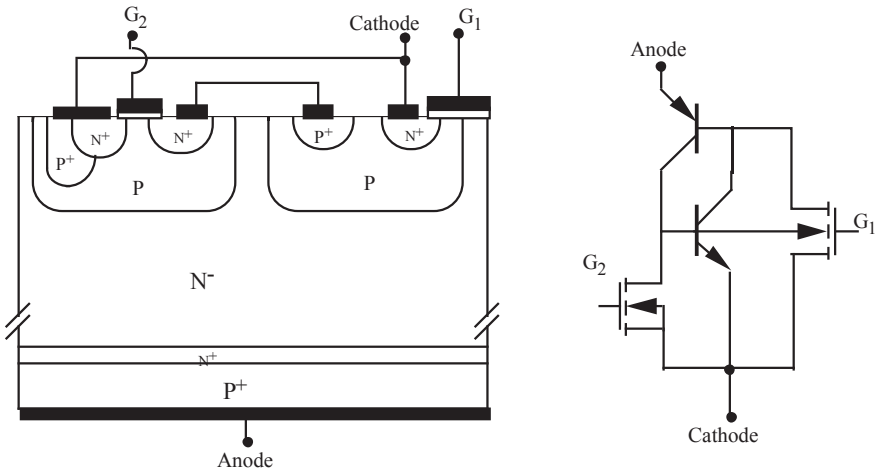


Figure 9.15. Cross-section view and electrical equivalent diagram of a DGMOT device

In the case of five layers structures, one should distinguish two types of devices: the NMCT [ART 93] and the PMCT. The principles for closing and opening are the same but the type of MOS transistors used for opening and closing is reversed because the successive layers of the thyristor structure are also reversed. The N or P qualification refers to the type of the thyristors lowest doped base thyristor. In the case of a N base, the integration mode imposes an N-channel MOS transistor for setting conduction and a P-channel for the opening (see Figure 9.16); while in the case of a PMCT with a P base, we have a P-channel MOS for setting conduction and a N-channel for the opening.

As the relationship between the mobility of electrons and holes is clearly favorable to electrons, the PMCT solution displays an improved performance at the opening from that of its counterpart NMCT. However, the real difficulty of manufacturing P-type low-doped substrates in a reproducible way, and the difficulty of growing thicker layers (thicker than 150 μm) by epitaxy, put the PMCT devices out of competition for immediate applications where the voltage required is greater than or equal to 1,200 volts.

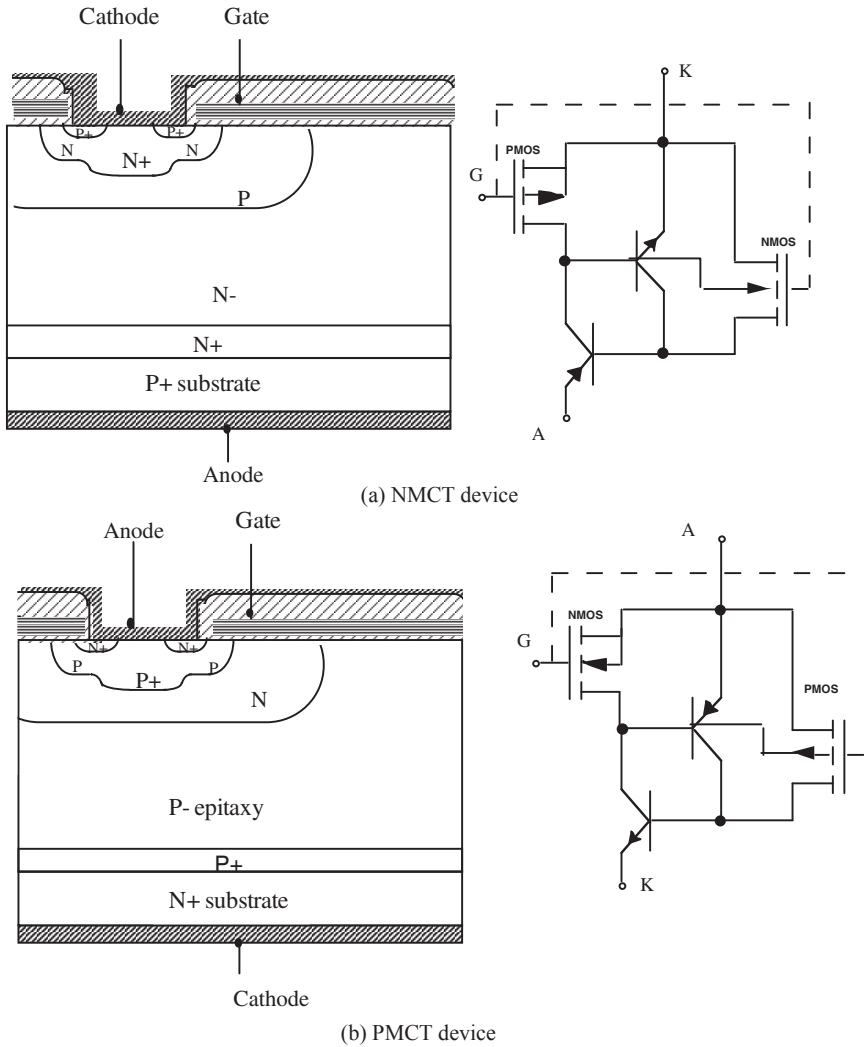


Figure 9.16. Cross-section view and equivalent circuit of (a) a NMCT structure and (b) a PMCT structure

9.2.2. Evolution towards the integration of specific functions

Currently, the concept of functional integration can be used to obtain, on the one hand, original ways of switching which are not exploited in the usual components; and on the other hand, ways to perform new functions including in a monolithic

device where the power components are together with protection elements, amplification and validation of the command. This must ultimately lead to improved performances, better adaptation to requirements (manufacturing can be made for a given application), and greater simplicity of design equipment. Firstly we will present the integration strategy adopted for the dual thyristor function; and secondly the integration of a switch-breaker function. These examples will enable us to highlight the generic nature of this mode of integration before outlining the possible developments for the integration of power functions.

9.2.2.1. *The dual thyristor*

The static switches involved in the conversion must possess static characteristics directly related to the reversibility of the energy conversion. It is possible to consider four different types of switches:

- non-reversible (e.g. the bipolar transistor, the diode);
- only reverse voltage (e.g. the thyristor);
- only reverse current (e.g. the dual-thyristor, the MOSFET); and
- reversible voltage and current (e.g. triac).

The dynamic characteristics of components – their way of switching and therefore way of command – must be linked both to the structure of the converter and its strategy of control. These components must either have orders for blocking or triggering, or present spontaneous commutations.

So far, only diodes, transistors, thyristors, and triacs devices have been monolithic. However, it is possible to obtain new integrated switches such as dual thyristors based on the method of functional integration.

The properties of the dual thyristor can be established from those of the thyristor in applying the rules of duality [FOC 78]. Indeed, as the thyristor is blocked during the passage of zero current (or, more accurately, below the keeping current value) the dual thyristor switches on with the passage of the zero voltage (by increasing values). The blocking is obtained by order if the switch is flowed by a positive current, as a thyristor is turned on by the order if a positive voltage is applied on its terminals. All properties of thyristor and dual thyristor are summarized in Figure 9.17 [CHE 88]. If the thyristor function is available as a monolithic device for a long time, dual thyristor function is achieved by combining the basic power components (bipolar transistor, MOST, IGBT, and diode) with a logic command (see Figure 9.18). The integration of these discrete solutions into silicon offers even less benefit as it does not exclude the major handicap of these circuits, namely the need for bulky, costly and potential EMC disturbance vector auxiliary power supplies. In the following sections, we will show that the functional integration

[BRE 98a] is able to achieve global function beyond the constraints described above.

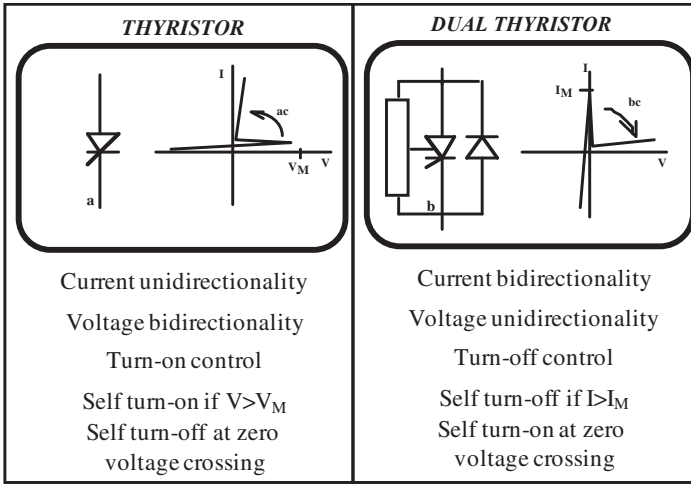


Figure 9.17. Symbols, characteristics and comparative properties of the thyristor and dual thyristor

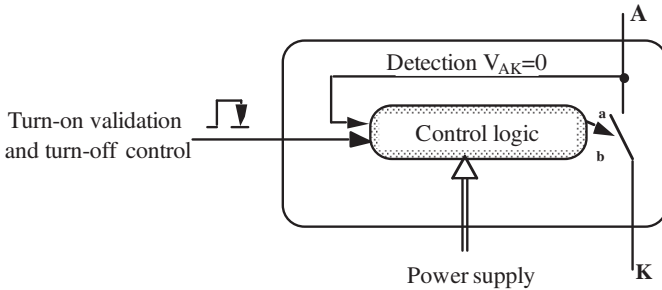


Figure 9.18. Discrete solution making the dual thyristor function

The dual thyristor function is a three segment switch, reversible in current. In the family of power semiconductor, the thyristor is the only one to present, under positive bias, a bi-stable blocked-conductive behavior, and to remain started after the abolition of the command order. The basic power device ensuring the “dual thyristor” consists of a thyristor structure. The static characteristic can be obtained by a thyristor structure associated with a diode placed in antiparallel. In terms of

dynamic characteristics, this function must exhibit a spontaneous switch-on at zero voltage and a switch-off ordered by a pulse. Thus, the full functionality can be obtained by completing the thyristor-diode association of two adapted cells for self switch-on and switch-off made with two MOS.

Thus, the heart of the function is constituted by a thyristor with self switch-on and switch-off ability. Figure 9.19 shows the equivalent electrical circuit of the power component for this function and the associated status table. At the closing, the thyristor switches on spontaneously when the anode voltage becomes positive through the current supplied by the MOS transistor with preformed M_1 channel, whose drain current feeds the base of the PNP section and acts as a triggering current for the thyristor. The switch-off is then made by applying a positive voltage to the transistor M_2 grid, to bypass the emitter base junction of the NPN transistor, as is the case in MCT structures. If we analyze the electrical diagram of this function, it is clear that the MOS transistor with preformed channel M_1 must include a N-channel since it is in parallel with the NPN transistor. As M_2 can be either N-channel or P-channel, we can consider two very different structure types for the monolithic integration of the switch function: a four layer structure (where M_2 is a N channel), and a five layer structure (where M_2 is a P channel). As the integration strategy is based on the main component, and as the achievement of auxiliary components must be done by adding a minimum of technological steps, we opted for a four-layer technology type thyristor. In order to make the drain of the opening NMOS, it is necessary to add an additional N^+ box. The main role of this transistor is to short circuit the P base with the N^+ cathode of the thyristor element. For this, a P^+ region is added and linked to the drain. To obtain the NMOS closure, a preformed channel area is added to link the N^- base (drain) to the N^+ cathode (source). The P base serves as a substrate for both MOS transistors. Figure 9.20 shows a schematic cross section of the four layer structure.

This integration is therefore based on the device being able to switch-on and switch-off by itself. The thyristor block can be provided by a pulse command [BRE 96, BRE 98a]. A diode placed in antiparallel ensures the reverse conduction of the device as provided in the dual thyristor. This structure nevertheless has the disadvantage of a boot transistor leakage current prevalent when the device is on hold status. Some developments have been made to reduce these problems, and several references are available on this subject [BRE 97, BRE 98b, BRE 98c, BRE 99, BRE 01, MAR 99, SAN 99c].

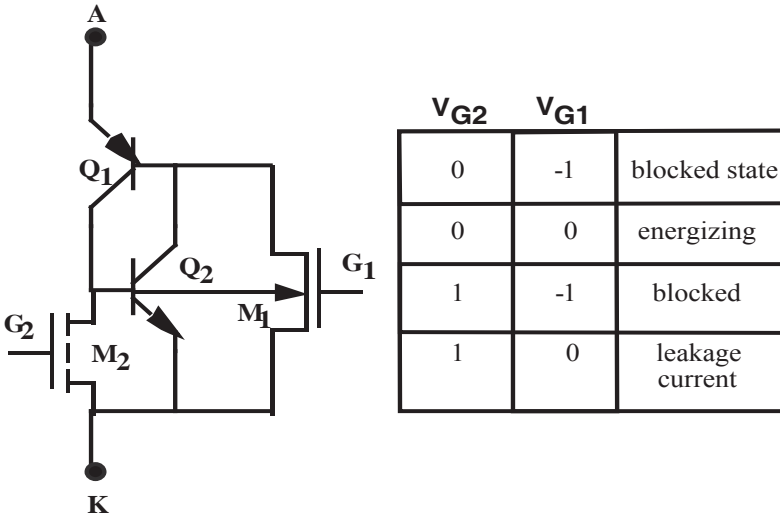


Figure 9.19 Electrical equivalent schematic and functional table of a thyristor able to switch on and off by itself

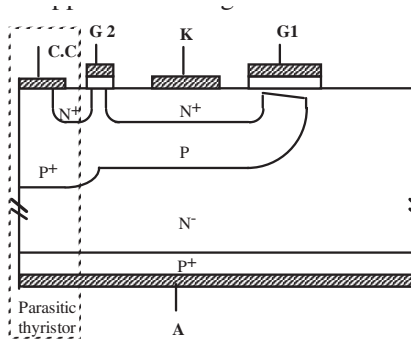


Figure 9.20. Schematic cross-section view of the four layer structure

9.2.2.2. Evolution towards new switch functions

The functional integration of the design and implementation of monolithic specific functions can also be applied to other types of functions [MAR 00]. One example is the power micro circuit-breaker [SAN 99e] or self switch-on and self switch-off structures [LAU 99]. The development of a bi-stable feature becomes an essential basic sub-assembly for more complex functions. Figure 9.21 below shows the schematic diagram of a micro circuit-breaker structure based on the integration

of several building blocks. The associated table on its right summarizes the function of each brick.

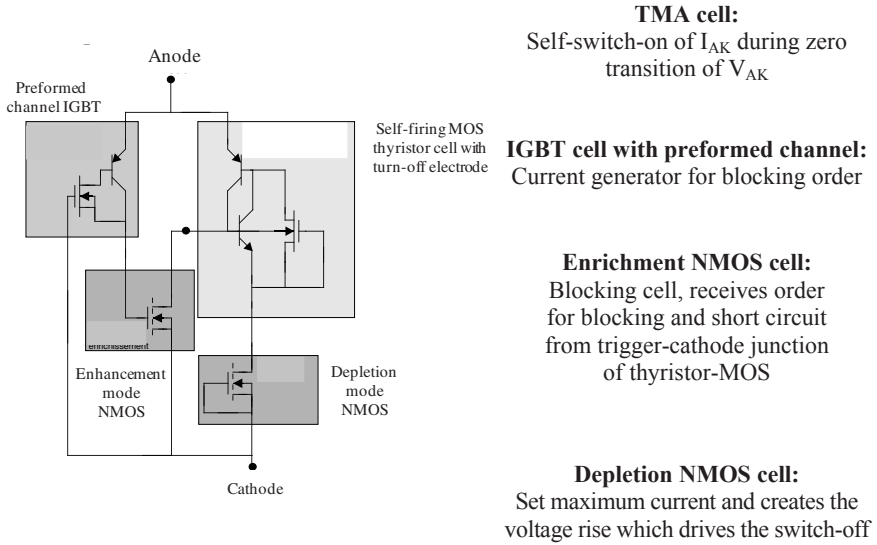


Figure 9.21. Structural schematic of a micro circuit-breaker function

This basic structure may also be implemented to synthesize a self switch-on and self-blocking component. In this case, the device incorporates a sensitivity or a threshold detection of one or two electrical quantities (current and voltage). Depending on the nature of the component, it can block or become a by-pass. Furthermore, through a process of functional integration, this type of specific function can be designed and implemented by association and cohabitation of building blocks. Figure 9.22 shows the principle schematic of such a function.

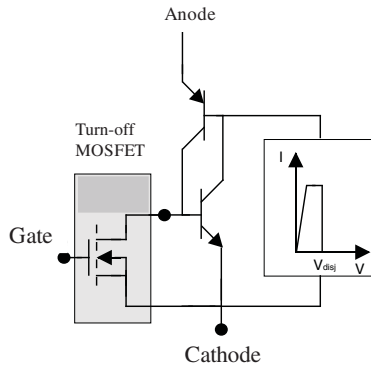


Figure 9.22. Structural schematic of a self-switch-on and self-blocking function

9.3. Integration of functions within the power component

The monolithic integration of functions within a power component is an important aspect, which comes as additional to functional integration. It is based close to or within the power component, on integration of electrical functions to facilitate the implementation but also to improve the characteristics of the integrated component. This process must be completed to limit the additional associated technological costs, without penalizing the characteristics of the main function, namely the power switch. There are command and associated type functions (closely implemented command, supply of the command, mono or two-way communication interface, etc.) and so-called protection functions [ALK 04, LAU 99, MIT 04a]. Other functions, such as state observers or sensors can also be considered. In this chapter we will discuss two examples of function integration to illustrate this theme.

In addition, other types of functions can be integrated. These functions are mainly about the electrical and physical environment of the component, but this time on the power side. As such, we can consider monolithic integration of CALC (circuit aid to the commutation), based on passive components, but also among other thermal functions for the development and/or the evacuation of the heat flow created by the chips. To illustrate this section, we discuss the case of two cooling solutions, integrated within the silicon chip.

9.3.1. Monolithic integration of electrical functions

The reliability and availability of power systems are a concern of current research in power electronics. This requires semiconductor power performances not

only in normal but also in extreme systems. An extreme system is unusual conditions of power component operation: transitional overload, accidental short circuit, wrong operation of the application system, high di/dt and dV/dt , high dissipated energy, special application, etc.

In such conditions, components are at their ability limits, leading to failure of operation, which can, in turn, lead to the destruction of components, and in the most serious cases, destruction of the system. The integration of specific protection circuits in the heart of the component, protecting it from failures of the external circuit, is therefore a valuable contribution for increasing the “reliability” and the availability of power systems [ALK 04, LAU 99].

In order to utilize more powerful devices receiving a close and self-protected command, it is necessary to associate with power component protection and control functions. These functions should not require the implementation of complex circuits. In this case, the power component occupies the largest area and fixes the technology.

Given that polysilicon is used in MOS technology for the manufacture of grids of power components (VDMOS or IGBT), this material can also be used to define the active areas in which we can use a number of protection components (resistors, diodes, MOS transistors). For example, it is possible to produce a layer of polysilicon on the field oxide of power components, this insulates against the power part, and receives the low voltage components (NMOS, diodes, resistors) (see Figure 9.23).

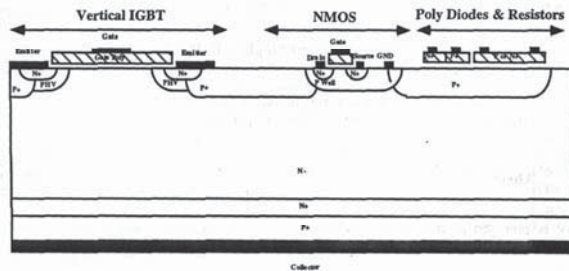


Figure 9.23. IGBT integrating protection circuits made from a polysilicon layer

9.3.1.1. Short circuit protection function

Within this general framework, we are interested in the IGBT protection against short circuits. At the onset of a short circuit, the power switch delivers an important

current with full voltage to its terminals. The dissipated power in the power structure is very high and its destruction is almost inevitable, because the temperature exceeds the allowable temperature for the junction. There are two types of short circuits: the first is already present at the of the power switch-on (type 1) and the second (type 2) appears when the power switch is already in conduction. Monolithic integrated solutions allow IGBT protection against short circuits in both type 1 and type 2.

9.3.1.1.1. Monolithic integrated detection and protection circuit

The short circuit state is detected if two conditions are met simultaneously:

- a switch-on command is applied to the switch grid; and
- power voltage is present on the anode.

The schematic of the electrical circuit protection principle is given in Figure 9.24. The main elements of this design include a power supply, a load resistance R_c , the IGBT, a circuit of grid command (synthesized by a resistance R_g and a voltage source E_g) and the detection and protection circuit against short circuits. This detection and protection circuit consists of an anode voltage sensor, a delay MOS (M_d), a delay resistance (R_{delay}) and a cut-off MOS (M_c).

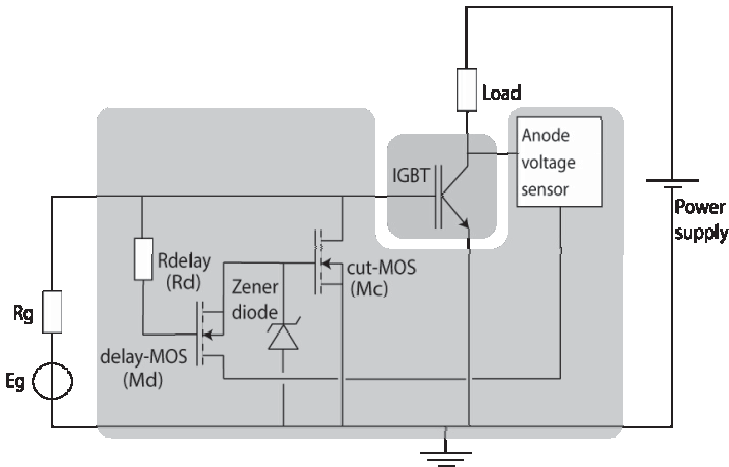


Figure 9.24. Schematic of the detection and protection circuit against short circuits

9.3.1.1.2. Operation principle of the anode voltage sensor

If the detection of grid command does not make a major problem, it is not the same for the detection of anode voltage. Indeed, on the one hand the anode is on the back side of the plate and on the other hand, this voltage can be of very high value (from a few to a few hundred kV). The anode voltage sensor must overcome these two problems.

Figure 9.25 shows a schematic cross-section view of the vertical structure of the anode voltage sensor. It is materialized with the help of two P^+ wells referenced to ground, of a deep and low-doped N^- base (which is naturally present in a power switch and allows the voltage strength) and a P^+ or N^+ implantation on the rear. A heavily N^+ doped region is located between the two P^+ regions, and allows an ohmic contact. This contact can detect a voltage V_{sensor} , which is an image of the voltage applied to the anode. There is no particular technological difficulty in producing this sensor. It may be easily integrated into any process of power technology [LAU 99].

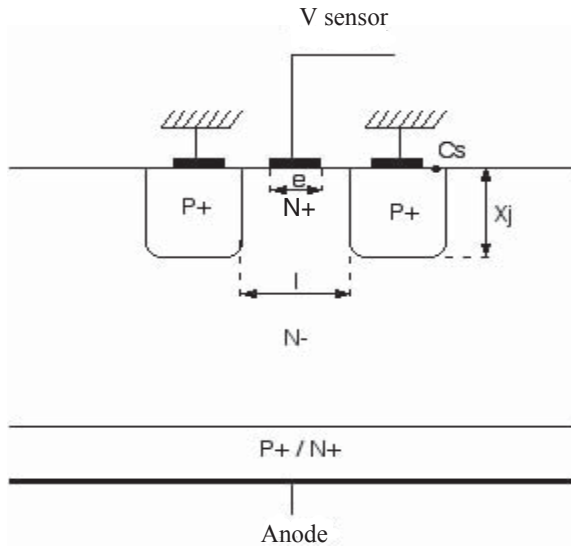


Figure 9.25. Vertical cross-section view of anode voltage sensor

For a given thickness of plate, voltage V_{sensor} depends on the physical characteristics of the P^+ wells (C_s = surface concentration of P^+ wells; X_j = junction depth of P^+ wells); thickness of the plate W ; length l , between wells; length of metallization "e" of ohmic contact, V_{sensor} (its influence remains modest and is

especially significant for high values of anode voltage); and, of course, the voltage applied to the anode. The parameters for optimization of the sensor are thus: e , X_j , C_s and l .

Figure 9.26 illustrates the behavior of the electrical voltage sensor, the change in voltage V_{sensor} , depending on the voltage applied to the anode for different lengths, “ l ”. The technological parameter values used for this example are: $W = 300 \mu\text{m}$, $X_j = 6 \mu\text{m}$, $C_s = 2.10^{19} \text{cm}^{-3}$ and $e = 4 \mu\text{m}$.

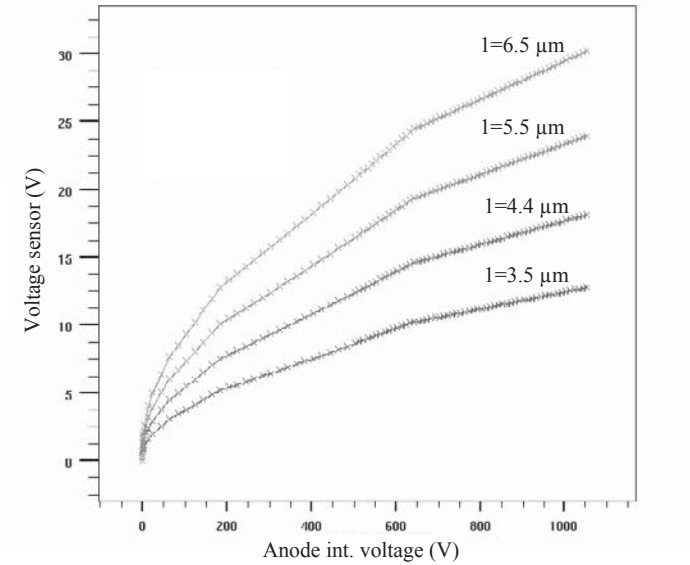


Figure 9.26. Voltage V_{sensor} depending on the anode polarization and the distance l between the two P^+ wells ($X_j = 6 \mu\text{m}$, $C_s = 2.10^{19} \text{cm}^{-3}$, $e = 4 \mu\text{m}$, $W_{\text{plate}} = 300 \mu\text{m}$)

V_{sensor} increases with the voltage applied to the anode but within a much lower range (between 5 and 25 V for a voltage anode up to 1,000 V). This voltage range can be directly used by a signal processing and information circuit. In fact, V_{sensor} is an image of the anode voltage. The optimization of this sensor shows that for a given anode voltage and a thickness W of plate, the increase in technology parameter values X_j and C_s , leads to a decrease in the value of V_{sensor} . Similarly, for identical conditions, a reduction in length will decrease the value V_{sensor} .

These findings on the electrical behavior of the sensor can be explained by the recovery of the potential lines between the two P^+ wells. Indeed, shorter length

and/or deeper P⁺ wells (large X_j and/or C_s), leads to a more effective recovery. Thus, the high potential line values cannot reach the ohmic contact issuing the V_{sensor} value.

9.3.1.1.3. Principle of operation of detection and protection circuit

The integrated structure corresponding to the circuit layout of detection and protection against short circuits (Figure 9.24) is shown in Figure 9.27. Around the IGBT, the elements are integrated in order to obtain a recovery of potential lines between each P⁺ area. There are two possibilities for integration of the delay resistance (R_{delay}). The first is to achieve a diffused layer, the second is to materialize resistance on the surface of the structure with a layer of polycrystalline silicon, deposited on the field oxide.

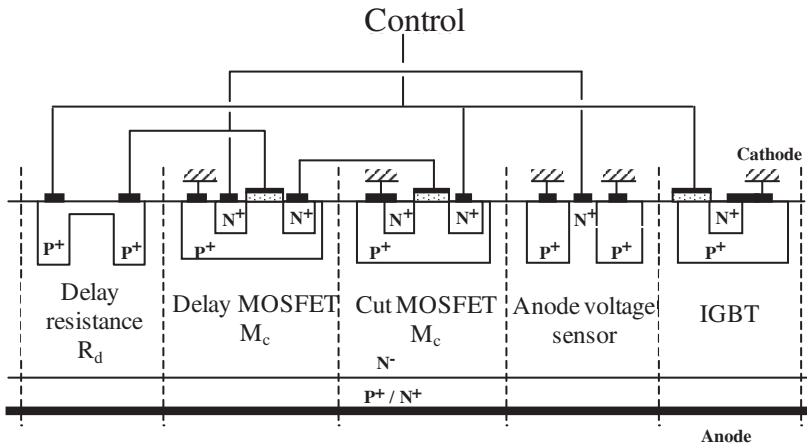


Figure 9.27. Integrated structure corresponding to the electrical diagram of Figure 9.24

At the onset of a short circuit, the anode sensor voltage delivers a continuous V_{sensor} image of the supply voltage. This voltage will trigger the command of the cut-off MOS (M_c) via the delay MOS (M_d). The latter must be calibrated so as to obtain a voltage on the cut-off MOS grid that exceeds its threshold voltage (V_{TC}) when a short circuit appears. In normal operation, V_{sensor} must be significantly lower than the threshold voltage of the cut-off MOS (V_{sensor} < V_{TC}).

In the case of a short circuit of type 1, the delay MOS can load the grid of the cut-off MOS with a delay determined by the time constant RC formed by its grid capacity and the delay resistance (Figures 9.24 and 9.27). Thus, during a normal commutation (transition from state OFF to state ON of the switch without the

presence of a short circuit). This time period allows the grid of the switch to take charge while the anode voltage drops down to a value equivalent to that of the on-state (a few volts). Indeed, without this delay time, the cut-off MOS would immediately be (active) and the switch could not operate. Once active (validation of the presence of a type 1 short circuit), the cut-off MOS discharges the grid for the power switch, making a (controlled) short circuit from the power switch to the ground. Switching to the on-state of the switch is then impossible.

If the phenomenon of short circuit occurs while the power switch is already in the on-state (type 2), anode voltage moves from a low value (voltage drop of the on-state) to full voltage. The anode voltage sensor then delivers a voltage above the threshold voltage of the cut-off MOS, which then discharge the gate of the IGBT. In this case, there is no delay time since the grid command of the delay MOS is already established. Note the introduction of the short circuit detection and protection circuit to the centre of the isolated grid power switch does not change its behavior under static and dynamic operation.

Figure 9.28 shows simulation results showing both the changes in command voltage (E_g) and voltage on the grid of IGBT without the presence of a short circuit, and for a type 1 short circuit. The change in grid voltage without short circuit shows that the presence of the detection and protection circuit does not alter the electrical behavior of the IGBT for a commutation from the on-state to the off-state. In contrast, the grid voltage of the IGBT in case of a type 1 short circuit, goes under its threshold voltage (≈ 4 V) within 300 ns, despite the grid command E_g .

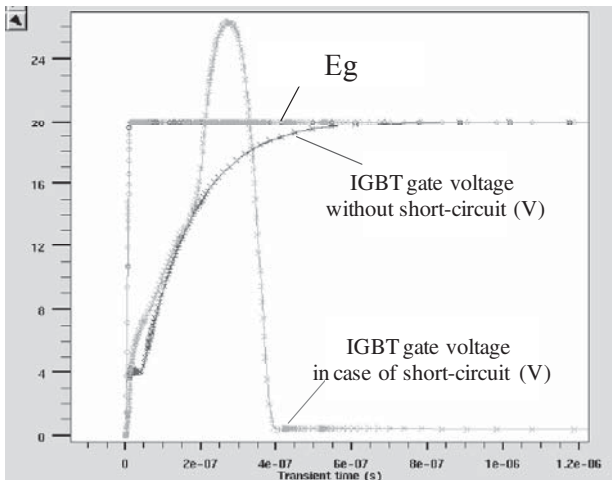


Figure 9.28. Two-dimensional electrical simulation of detection and protection circuit with an isolated grid power IGBT in the case of a type 1 short circuit

9.3.1.2. The self-supply of the close command of an isolated grid switch

In power electronics, supplying the close command of a grid switch is a “basic” brick for its implementation. It helps to provide energy to the close command, usually via a galvanic isolation to ensure the adaptation of voltages. Its integration within the power component has several advantages:

- simplification of the implementation of the component;
- reduction of the connections and increased reliability;
- reduction of conducted type EMC propagation paths; and
- creating a board to supply auxiliary functions.

However, to be “viable” economically and technically speaking, the integration of this type of supply must remain simple, without additional major technological and especially generic cost. To meet these functional but also technology requirements, the best choice is not always the most obvious. International research has shown several ways to supply the command of a grid switch, it now remains to identify those that can be integrated within a VDMOS type power chip.

One of these is to take the energy on the terminals of the component when it is available [MIT 04a]. Its originality lies in the fact that all the active components can be integrated within the power chip through its own technological process. Based on the very simple and general principle of the linear regulator, this solution helps to overcome the problems of galvanic isolation and monolithic integration, while providing a solution for high efficiency conversion. Its electric schematic is given in Figure 9.29.

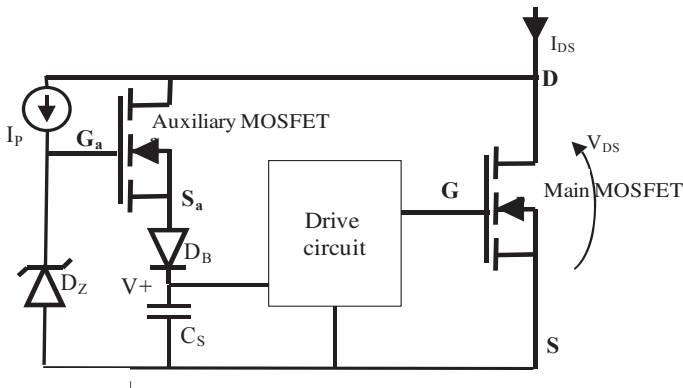


Figure 9.29. Electrical schematic of an integrated function for supplying the close command of a power switch

9.3.1.2.1. Principle of operation

The operating principle is based on a “pulsed” linear regulator placed in parallel with the power transistor. When the main transistor is blocked, the circuit in parallel regulates the voltage of a capacitor storage via an auxiliary power transistor and a branch of polarization. When the transistor enters the on-state, blocking diode Db prevents the capacitor discharge. The energy stored in the capacitor is then used to supply the close command of the switch during its conduction phase. It is important that the main switch be regularly blocked to enable the self-supply system to store renewed energy.

9.3.1.2.2. Realization

The power components all share the same constraints in voltage, which greatly facilitates their monolithic integration. In addition, they all have as a common electrode, the rear side of the component. The low-voltage components can be made on the surface via the technological process of the main transistor. A cross-section view of the whole is given in Figure 9.30. It should be noted that a VDMOS process can, with approximate flexibility, create all the functions. The various elements of the self-supply must be properly designed in order to obtain the desired functional or electrical interface characteristics.

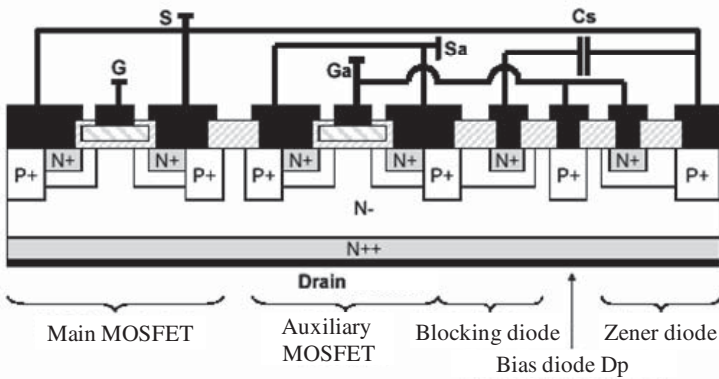


Figure 9.30. Cross-section view of all elements of the supply system as a monolithic integration compatible with the main switch (except the element of storage)

Such a solution is based on a system approach closely coupled with a desire for monolithic integration (Figure 9.31). If it is not universal, it has some advantages as being simple, efficient and very easy to implement [MIT 04c]. Figure 9.32 shows the result of a practical implementation where we can observe the proper operation

of a power transistor via the evolution of its drain source voltage. We can also see that the function regulates (more or less effective following the specification and characteristics of components) the close command voltage.

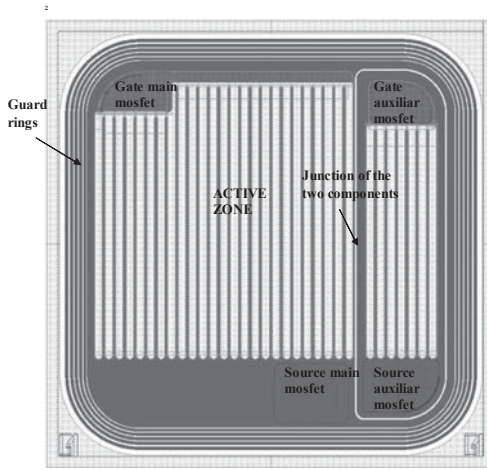


Figure 9.31. Top view of the main and auxiliary components

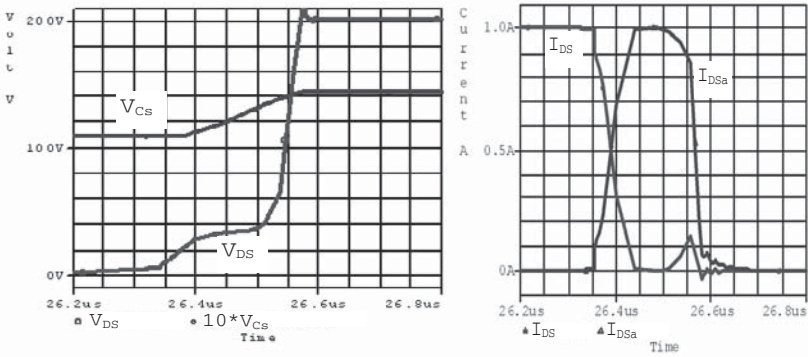


Figure 9.32. Simulation results showing the evolution of waveforms during storage capacitor recharge

Evolution of the close command supply technique can be considered, implementing a JFET type power switch instead of the auxiliary transistor and its

branch of polarization (see Figure 9.33) [MIT 04b]. This component can be fully integrated within the power component, thus providing a simplified solution with similar but different characteristics from the previous solution.

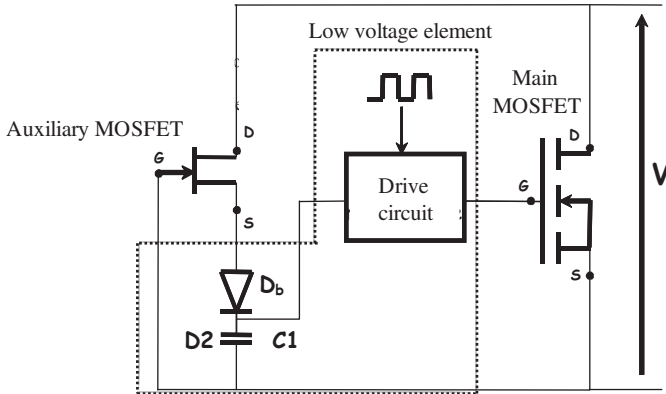


Figure 9.33. Electric schematic of another technical solution (with a JFET transistor) for integration and compatible for supplying the close command

9.3.2. Extensions of integration

9.3.2.1. The passive elements

The reductions in the size and weight of portable equipments (telephones, micro-computers, electronic diaries) are linked to a reduction of power dissipation. This strategic niche has led to development of works related to the development of passive components on silicon, in the prospect of moving towards monolithic converters. This approach should reduce the number of components, their connections and lead to more reliable and less expensive products. Many filtering applications based on RL networks are also involved.

Recent developments in the field of micro-technologies have profoundly changed the microstructure manufacturing possibilities. These new techniques are particularly well suited for the manufacture of windings on silicon. The achievement of resin elements and the electrochemistry of magnetic or conductive materials supports the creation of magnetic cores and windings with a thickness of several tens of microns. Generally, the so-called “cold” technological process is able to operate *post-processing* and therefore consider integration with semiconductor devices. First prototypes with a value of inductance of 35 nH/mm² at 1 Mhz were made. The manufacturing process used is fully compatible with the standard CMOS process and micro-converters with an output power of 1 to 2 W may be

incorporated. The other major passive element that would be good to integrate on silicon is the capacitor. Note, the deep etching technology, which uses the volume of silicon to maximize energy storage per area unit.

9.3.2.2. *The integrated cooling*

The thermal environment of power components determines their proper operation and their electrical performances. On the one hand, it is important to facilitate the evacuation of losses generated by the component and on the other hand, it is interesting to maintain a temperature as homogeneous as possible within the component. For this reason, research is undertaken to integrate within the power chip, a thermal function playing the role of heat distribution, ensuring an isothermic operation of the chip (in case of non-uniform loss). Figure 9.34 shows two possible solutions for silicon: one of them is based on the integration of a single phase micro-channel exchanger, the other is based on the integration of a heat pipe dispatch. Figure 9.35 shows the schematic diagram of a heat pipe for heat dispatching [AVE 02a].

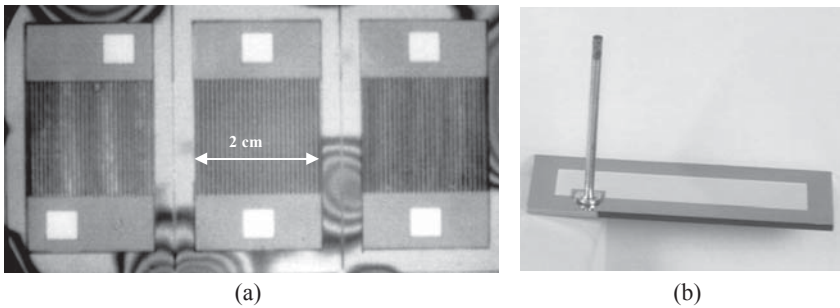


Figure 9.34. (a) All silicon single phase exchangers; (b) all silicon heat pipe

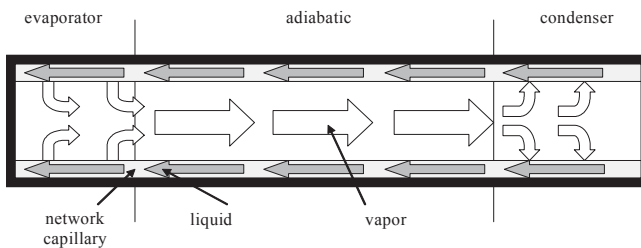


Figure 9.35. Principle schematic of exchanger

The distribution of heat increases the exchange surface with the rear and thus making the flow a more important heat flux. This helps to maximize the current rating of the semiconductor components. For example, for a MOSFET transistor, the current rating may be greater than the conventional specifications if the exchange on the back side is particularly powerful.

The evacuation of heat can also ensure greater uniformity of temperature within the chip. Thus, when hotspots appear locally, the integrated heat dispatcher can limit the local heating; which often makes a thermal runaway, and the destruction of the component possible.

9.3.2.2.1. Realization

The heat dispatcher is created within the crystalline structure of the component. This limits the adverse effect of the interfaces and thus maximizes the performance of the exchanger or the dispatcher. Its integration also helps to spread the flow of heat before the first critical thermal resistance, that of the electrical insulator (usually a ceramic type AlN, Al₂O₃, etc.).

The dispatcher is made using the techniques of deep etching and pasting of plates (silicon wafer bonding). The plates are engraved to create an important exchange surface, a capillary network. The assembly by plate pasting integrates the thermal function into the silicon. The diagram below (Figure 9.36) presents this assembly.

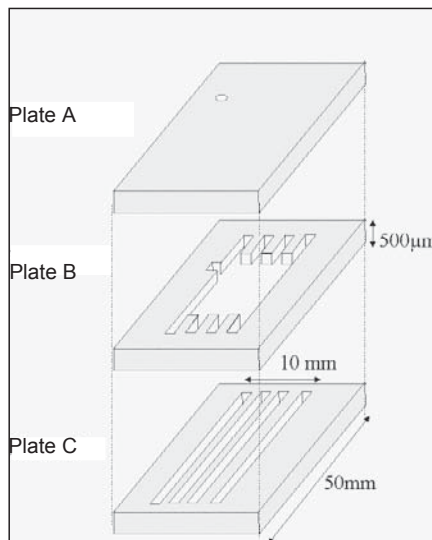


Figure 9.36. Pasting of three layers to produce the thermal function

The photos in Figure 9.37 present some views by using microscope to electronically scan a micro-channel network and a capillary network. The resolution sought is the micrometer [AVE 02b, AVE 04].

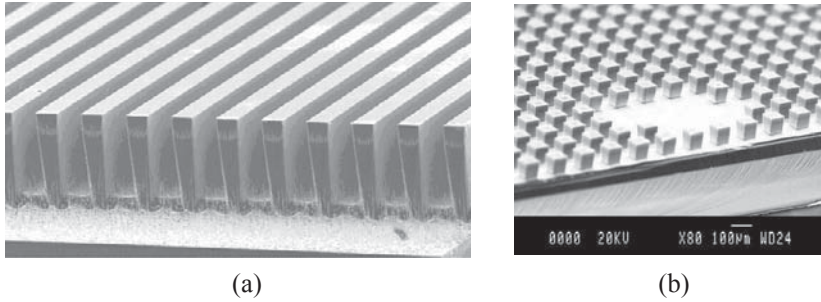


Figure 9.37. (a) Micro-channels network for a single phase heat exchanger;
(b) capillary network for heat pipe structure

9.3.2.2.2. The exchanger

The integrated single phase exchanger evacuates the losses generated by the device via a circulating fluid in a network of micro-channels. The large exchange surface associated with a phenomenon of forced convection helps to maximize the exchanges between the chip and the ambient. The groove size is a major parameter resulting from compromise between the exchange surface and loss of charge and dirt. Indeed, if the achievement of a silicon micro-channel technology poses no particular problem, optimization of such an exchanger does not automatically lead to a very dense network of micro-channels. Studies have been conducted in this way to simplify the design of this type of function but the theory of heat at a micro level does not clearly identify the possible optimum.

In the figure, this type of exchanger can extract a significant amount of heat per unit area. Table 9.1 gives some experimental values for a laboratory prototype.

Q l/min	ΔP : pressure drop	P : electric power delivered Watt	ΔT_j °C	R_{conv} measured K/cm ² ·W	R_{conv} calculated
0.5	0.066	50	33	0.56	0.85
		100	63	0.53	0.85
1	0.22	50	26.6	0.48	0.4
		100	50.2	0.45	0.4

Table 9.1. Figures for an all silicon single phase exchanger

9.3.2.2.3. The dispatcher

The monolithic integrated dispatcher enables increase of the exchange surface and therefore the flow of exhaust heat per unit area, while promoting the thermal balance within the chip. This last feature is based on the creation of a particularly powerful heat sink. This is achieved by a heat pipe that helps maintain an equivalent resistivity near zero within the thermal function. The hot areas, called evaporators are then linked to the cold areas, known as condensers, by a capillary network (Figure 9.35). The liquid trapped in the heat pipe is sprayed on one side, and transferred to the condenser, where it becomes a liquid. The way back is through a capillary network, a real pump of the integrated thermal function. The operating principle is described by the diagram in Figure 9.38.

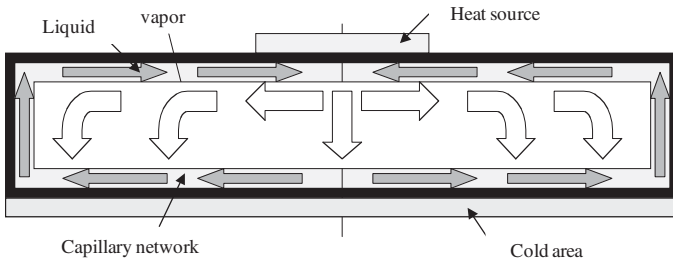


Figure 9.38. Schematic of the heat pipe with heat dispersal

For the heat dispersal function, the evaporator is on the front and the condenser is on the back side. For the heat dispatcher function, evaporators and condensers are both on the front, with only the condenser at the rear.

Figure 9.39 is an illustration of the isotherm and heat transfer effects obtained with the use of a heat pipe in silicon technology.

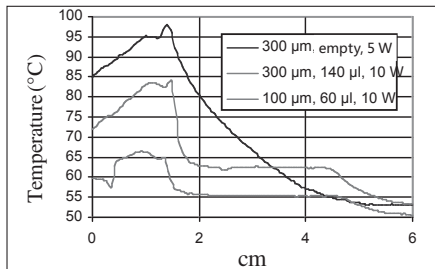


Figure 9.39. Changes of temperatures on surface of an all silicon heat pipe for several filling conditions

This process of thermal integration has the potential to affect power components as has been mentioned, but can also affect other applications of microelectronics, and more particularly the very important market of computers and microprocessors.

9.4. Design method and technologies

9.4.1 *Evolution of methods and design tools for functional integration*

In the past, the design of power discrete devices (diodes, bipolar transistors, MOS, IGBT, thyristors, triacs) was made for a given range of power and frequency. Regardless of the precise characteristics of the future application, electronic power application designers were choosing in a catalog the best-suited devices meeting their specifications. This approach, separating the activities of device designers from those of power systems engineers, is no longer adapted to the design of integrated power functions. A new approach is to develop specific functions knowing as *a priori* the specifications of the functionality, the electrical characteristics of the function, and the constraints imposed by its environment. These specific functions result in a de facto system approach.

As we have previously demonstrated, a device based on the mode of functional integration results from the association of basic cells in the silicon. These associations are the topology, layout and physical characteristics of the different semiconductor layers of a cell that determine its electrical functionality. From this point of view, 2D simulation tools based on solving physical equations of a structure described by the physical characteristics of layers (doping profiles, oxide thicknesses, etc.) and their design, can obtain the mode of operation, and the electrical characteristics of the device, at the cost, however, of a careful description in terms of networking and use of appropriate models and physical parameters. The mode of description, based on the topology of the integrated structure, is at a level too far from the functionality and even electrical characteristics. The exclusive use of 2D simulation tools is not particularly well suited to the design of such functions, even if their development constitutes an essential link in the chain of design.

As the function design is closely linked to the surrounding system, the electrical schematic, as a first step, remains the best suited symbolic representation for designers, even if all the subtleties in terms of electrical interactions cannot always be translated. Thus, each cell must be defined by its electrical equivalent, associated models and surface topologies (drawings of masks).

Several phases lead to the design of an integrated device fulfilling the functions defined by a specification. The first phase is to define the function from an electric viewpoint, the second concerns the design of the integrated structure providing this function. During these two phases, designers do not have the same objective, and

indeed do not have the same approach, nor the same culture. Tools and specific methods of design are therefore needed to obtain a coherent approach taking into account the technological and system components of the problem. In this case, the common denominator is made up of a library of basic elements taking into account: the technological aspects through schematic cross-section views of the cells and surface topology; the electrical aspects represented by the equivalent electrical schematic, and the associated models. These models are based either on a more electrical description for the first phase, or a more physical for second, while generally taking into account both aspects in each case.

The problem in the first phase is to define the electric schematic that ensures the functionality required by the specifications. The designer must have a tool enabling a “functional” approach to the problem, based on purely electric considerations, both in terms of output characteristics, and input parameters. These requirements are consistent with the characteristics and specificities offered by the behavioral models. These are based on a description of the behavior of electrical characteristics corresponding to an operation of the component. These behavioral models are mathematical forms.

The other phase involves the design of the integrated structure, i.e. the determination of technological and geometrical parameters. In this perspective, we need to develop analytical models to highlight the influence of physical and geometrical parameters on the electrical characteristics of the function (or behavior in the application sought). At this stage, a library should allow us to make a quick first design of the structure to be integrated, including the number of cells to integrate (requested surface), and values of technological parameters. With this approach, 2D simulation tools can then be used to validate the results of this design phase before committing to the manufacturing stage. The organizational structure of Figure 9.40 illustrates this design strategy.

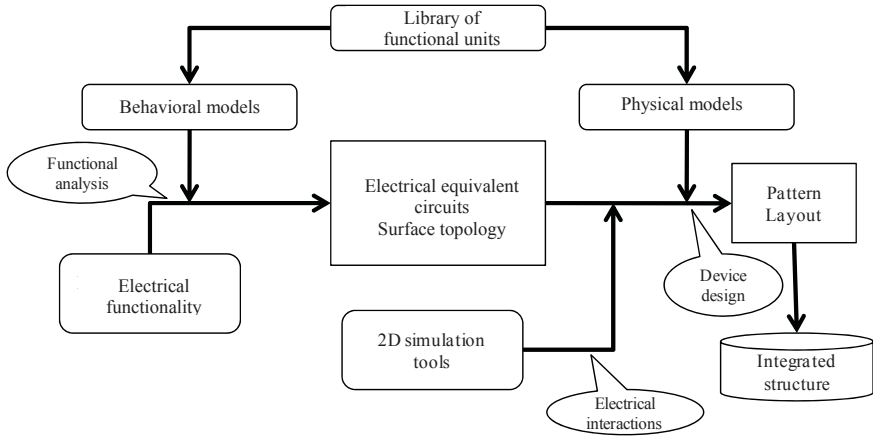


Figure 9.40. Organization chart describing the design methodology for functional integration

The following table (Table 9.2) presents an inventory of the major basic cells listed for a 4-layer N/P/N/P thyristor type technology integrating the four types of MOS transistors, channel N and P, with enrichment and with depletion.

9.4.2. The technologies

The functionality and electrical characteristics of devices based on this method of functional integration depend not only on the arrangement of semi-conductive layers and surface topology but also on the physical characteristics of different regions.

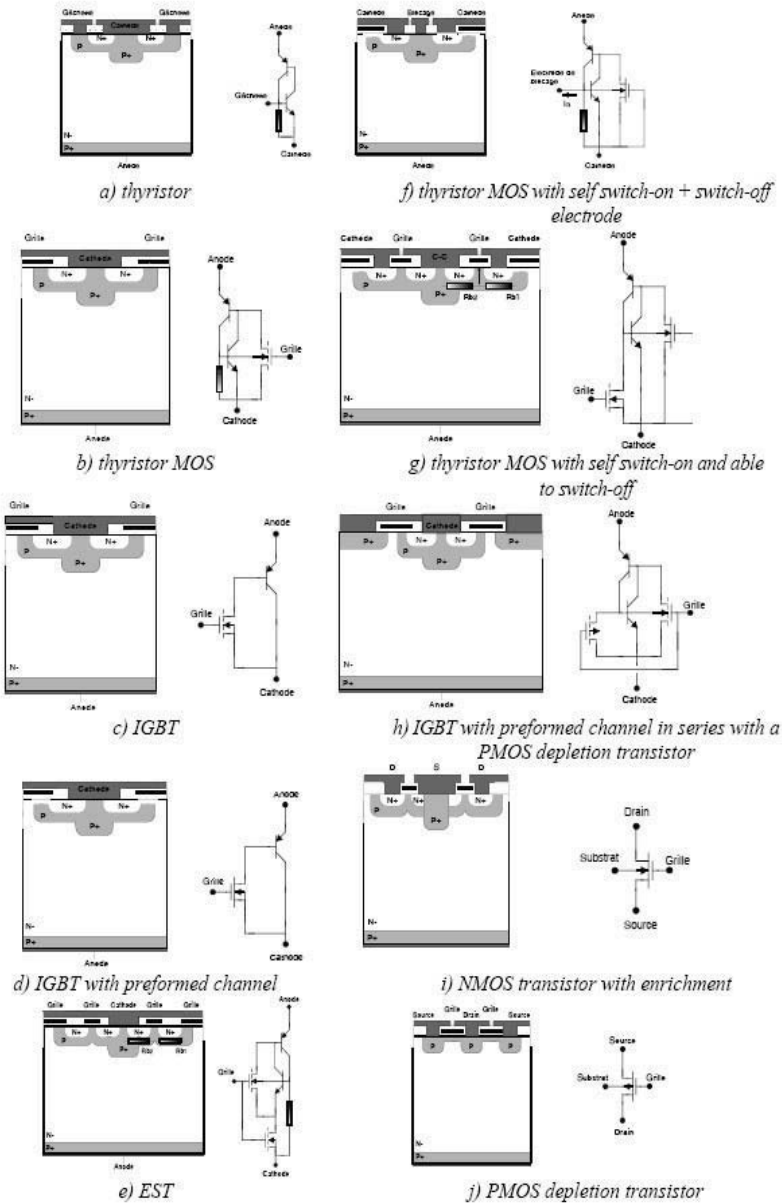


Table 9.2. Major cells used for functional power integration

The technology used in functional integration must therefore be composed of optimized stages, which are compatible with each other. The technological process of producing a structure for an electrical function will be established from the association of all or part of the optimized steps of this sector. This pipeline can be established around an “in-line” process with polysilicon grids in order to achieve basic power devices of the MOS/bipolar family (IGBT, MOS-Thyristor) and supplemented by specific technological steps achieving:

- integrated elements on the rear side;
- the possibility of introducing the four types of MOS;
- the possibility of carrying out two types of P cells;
- P– peripheries;
- P+ cells; and
- the introduction of specific technological steps.

The step sequence must be in accordance with the final heat balance of each step. Figure 9.1 shows the technological step sequence of a flexible chain.

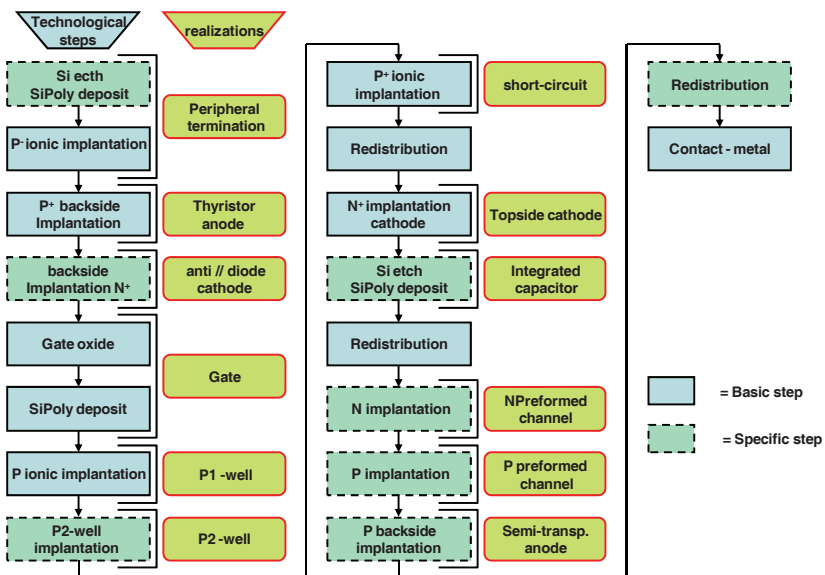


Figure 9.41. Linking technological steps

9.4.2.1. A sequence example

The main building blocks of this technology are made in the following way: implementation of P⁺ cells front and rear, producing the N⁺ cathode on the rear side, creating the N doped polysilicon grid, leading to P cells and N⁺ cathode aligned with the grid and production of preformed N and P channels.

The starting substrate is N-type silicon. P⁺, P and N⁺ regions are made by ion implantation (boron for the P type and arsenic for the N⁺ type). The redistribution of the P⁺ regions (front and rear) and the N⁺ rear cathode is done, during the creation of the gate oxide made at 1,100°C, and during redistributions of P cells and N⁺ cathodes on the front side at 1,150°C. The gate polysilicon is deposited by LPCVD from the decomposition of silane (SiH₄). This is doped by N dissemination of phosphorus. The preformed channels are achieved through the polysilicon by ion implantation of boron for P-type channels and phosphorus for N-type channels. They are then redistributed at a temperature of 950°C. Figure 9.42 shows the sequence of technological steps for the creation of the polysilicon grid, P and N⁺ cells.

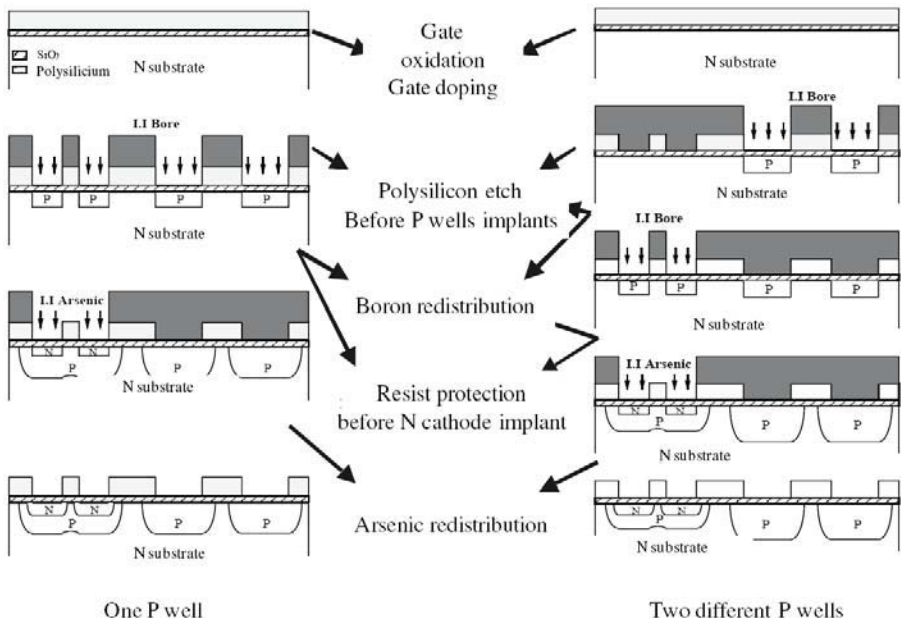


Figure 9.42. Different sequences of technological steps

9.4.2.2. *Specific technological steps*

Increasing the complexity of the integrating power functions leads to the development of specific technological steps compatible with the flexible basic industry process. These developments are attributed to progress made in recent years in the techniques used in the field of micro-technology. The reactive ion etching (RIE), the deep etching of silicon by KOH or EIR, the chemical deposits under high pressure vapor (CVD) or low pressure (LPCVD), the deposits of thick resins, the electrochemical deposition, the thermo migration of aluminum, the report of layer and new techniques of assembling being the main examples. The mastery of these techniques will achieve, over time, variable integrated capacities, micro-windings, micro-transformers, micro-converters, micro-coolers, etc.

The control and integration of these technologies into flexible technology will ultimately allow, the foundations of power structure design to incorporate active and passive elements, and also develop new features.

9.5. Conclusion

Power electronics was developed in parallel with microelectronics, although it has different objectives: increasing controlled powers, and increasing signal processing capacity.

Major technological advances have been made in the field of microelectronics, that over the past 30 years have had interesting consequences for power electronics. In this chapter, we discussed examples of monolithic integration based on silicon technology (hybrid-type integration of circuits is also possible). Two methods stand out: one emphasizes functionality, while the other relies instead on optimizing the operation and related characteristics.

Initially, achievements using the *Smart Power* technology were made in the low voltage field, corresponding to automobile applications. However, the main success of these techniques of integration comes from the conjoining of bipolar and MOS technologies, which has provided many power component prototypes, but also to the IGBT which is today the best component for great power.

The success of the IGBT is a great springboard for promoting the integration of power and it seems likely, as we showed in the last parts of this chapter, that we will evolve to silicon chips, incorporating many features, and achieving a self-contained device ready to use, reliable and compact (integration of auxiliary power supplies, controls, safeguards, cooling, etc.).

It also seems that by adding the integration of some passive components, we can in the next decade, develop autonomous micro-systems performing the switching function for high power and packaging of electrical energy, which is so widespread.

9.6. References

- [ALK 04] ALKAYAL M.F., CRÉBIER J.C., SCHAEFFER C., “A new monolithic adjustable over-voltage protection circuit”, *IEEE IAS'04*, 5-7, Seattle, USA, 2004.
- [ART 93] ARTHUR S.D., TEMPLE V.A.K., “Special 1400 volt N-MCT designed for surge applications”, *Fifth European Conference on Power Electronics and Applications EPE*, p. 266-271, Brighton, United Kingdom, 1993.
- [AVE 02a] AVENAS Y., PERRET C., GILLOT C., BOUSSEY J., SCHAEFFER CH., “Integrated cooling devices in silicon technology”, *The European Physical Journal of Applied Physics*, vol. 18(2), p. 115-123, 2002.
- [AVE 02b] AVENAS Y., GILLOT C., BRICARD A., SCHAEFFER C., “On the use of flat heat pipes as thermal spreaders in power electronics cooling”, *IEEE-PESC'02*, Queensland, Australia, 23-27 June, 2002.
- [AVE 04] AVENAS Y., GILLOT C., SCHAEFFER C., *Caloducs plats en silicium pour composants électroniques*, Techniques de l'ingénieur, August 2004.
- [BAL 79] BALIGA B.J., “Enhancement- and depletion-mode vertical-channel MOS gated thyristors”, *Electronic Letters*, vol. 15(20), 1979.
- [BAL 88] BALIGA B.J., CHANG H.R., “The MOS-Depletion mode thyristor: a new MOS-controlled bipolar power device”, *IEEE Electron Device Lett.*, vol. 9(8), p. 411-413, 1988.
- [BAL 90] BALIGA B.J., “The MOS-gated emitter switched thyristor”, *IEEE Electron Device Lett.*, vol. EDL-11, p.75-77 1990.
- [BAU 91] BAUER F., HALDER E., HOFFMANN K., HADDON H., ROGGWILLER P., STOCKMEIER T., BRUGLER J., FICHTNER W., WESTERMANN M., MORET J.-M., VUILLEUMIER R., “Design aspects of MOS-controlled thyristor elements : technology, simulation and experimental results”, *IEEE Transactions on Electron. Devices*, vol. 38(7), 1991.
- [BOU 02] BOURENNANE A., BREIL M., SANCHEZ J.-L., AUSTIN P., JALADE J. , “New MOS-triac structures for specific mains applications”, *European Power Electronics – Power Electronics Motion and Control Conference*, Dubrovnik 2002.
- [BOU 04] BOURENNANE A., Etude et conception de structures bidirectionnelles en courant et en tension commandées par MOS, PhD Thesis, Paul Sabatier University, 2004.
- [BRE 96] BREIL M., SANCHEZ J.-L., BERRIANE R., RIOS J., “Etude des performances à l'ouverture de dispositifs MOS-Thyristors auto-amorçables et blocables”, *Electronique de Puissance du Futur EPF'96*, p. 51-56, Grenoble, France, 16-18 December 1996.

- [BRE 97] BREIL M., SANCHEZ J.-L., “Analytical Model for the optimization of the turn-off performance of a self firing MOS-Thyristor device”, *Seventh European Conference on Power Electronics and Applications: EPE'97*, p. 3.042-3.048, Trondheim, Norway, 8-10 September, 1997.
- [BRE 98a] BREIL M., Etude d'associations MOS-thyristor autoamorçables et blocables. Exemple d'intégration de la fonction thyristor dual, PhD Thesis, l'Institut National des Sciences Appliquées, Toulouse, 1998.
- [BRE 98b] BREIL M., SANCHEZ J.-L., AUSTIN P., ROUSSET B., ROSSEL F., LAUR J.-P., “Conception et réalisation d'associations MOS-Thyristor blocables basées sur une filière technologique ‘quatre couches’”, *Electronique de Puissance du Futur EPF'98*, Belfort, p. 21-27, 16-18 December, 1998.
- [BRE 98c] BREIL M., SANCHEZ J.-L., AUSTIN P., LAUR J.-P., “Turn-off performance comparison of self-firing MOS-thyristor devices for ZVS applications”, *Bipolar/BiCMOS Circuits and Technology Meeting, BCTM'98*, p. 53-56, Minneapolis, USA, 27-29 September, 1998.
- [BRE 99] BREIL M., SANCHEZ J.-L., AUSTIN P., LAUR J.-P., “A new self-firing MOS-thyristor device: optimization of the turn-off performance and experimental results”, *Microelectronics Journal (Special Issue on Power Devices and ICs)*, vol. 30, no. 6, p. 569-610, 1999.
- [BRE 01] BREIL M., MARMOUGET M., SANCHEZ J.-L., AUSTIN P., BONNET G., “Specific design methodology dedicated to the development of new power functions based on the concept of functional integration”, *Mixed Design of Integrated Circuits and Systems, MIXDES 2001*, p. 225-230, Zakopane, Poland, 21-23 June 2001.
- [CHA 95a] CHARITAT G., SANCHEZ J.-L., ROSSEL P., TRANDUC H., BAFLEUR M., “Power integrations : overview and future”, *Mix VLSI'95, Mixed Design of VLSI Circuits*, p. 47-59, Krakow, Poland, 1995.
- [CHA 95b] CHARITAT G., SANCHEZ J.-L., ROSSEL P., TRANDUC H., BAFLEUR M., “Power integration: overview and future”, *Mix VLSI'95, Mixed Design of VLSI Circuits*, Krakow, Poland, p. 47-59, 1995.
- [CHE 88] CHERON Y., La commutation douce dans la conversion statique de l'énergie électrique, Thesis, INPT, 1988.
- [DAR 86] DAREES D., Contribution à l'étude d'associations monolithiques de composants MOS et bipolaires: le thyristor à gâchette isolée, PhD Thesis, INSA Toulouse, 1986.
- [FOC 78] FOCH H., MAZRTY P., ROUX J., “Utilisation des règles de dualité pour la conception de convertisseurs à transistors”, in *Le transistor de puissance dans la conversion de l'énergie*, p. 293-323, Thomson, Aix en Provence, 1978.
- [GEN 64a] GENTRY F.E., SCACE R.I., FLOWERS J.K., “Bidirectional Triode P-N-P-N Switches”, *Proc. of the IEEE*, p. 355-369, 1964.
- [GEN 64b] GENTRY F.E., GUTZWILLER, HOLLONYAK, VON ZASTROW, *Semiconductor Controlled Rectifiers: Principles and Applications of P-N-P-N Devices*, Prentice-Hall Inc., NJ, USA, 1964

- [JAE 87] JAECKLIN A., "A N FET-Driving power thyristor", *IEEE Transactions on Electron. Devices*, vol. ED-34(5), 1987.
- [LAU 99] LAUR J.-P., SANCHEZ J.-L., AUSTIN P., JALADE J., MARMOUGET M., BREIL M., ROY M., "New integrated device for units protection: circuit-breaker structures", *8th European Conference on Power Electronics and Applications, EPE'99*, Lausanne, Switzerland, 7-9 September 1999.
- [LIL 92] LILJA K., STOCKMEIER T., "The FIBS, a new high voltage BiMOS switch", *ISPSD '92*, p. 261-265, Tokyo, 1992.
- [MAR 99] MARMOUGET M., SANCHEZ J.-L., AUSTIN P., BREIL M., LAUR J.-P., "A new specific design methodology for functional integration", *International Semiconductor Conference, CAS'99*, p. 47-50, Sinaia, Romania, 5-9 October 1999.
- [MAR 00] MARMOUGET M., Contribution au développement d'outils d'aide à la conception de dispositifs de puissance basé sur le mode de l'intégration fonctionnelle, PhD Thesis, Paul Sabatier University, 2000.
- [MIT 04a] MITOVA R., CRÉBIER J.-C., AUBARD L., SCHAEFFER C., "Gate conductor supply of power switches without galvanic insulation", *IEEE IAS'04*, Seattle, USA, 5-7 October 2004.
- [MIT 04b] MITOVA R., CRÉBIER J.-C., AUBARD L., SCHAEFFER C., "Integrated conductor supply for power MOSFET based on vertical JFET", *ISPS'04*, Prague, Hungary, 30 August-3 September, 2004.
- [MIT 04c] MITOVA R., ALKAYAL M.F., CRÉBIER J.-C., AUBARD L., SCHAEFFER C., "Intégration d'un système de l'autoalimentation de la commande rapprochée d'un interrupteur de puissance", *EPF'04*, Toulouse, France, September 2004.
- [NAD 91] NADAKUMAR M., BALIGA B.-J., SHEKAR, TANDON S., REISMAN A., "The base resistance controlled thyristor (BRT), a new MOS-gated power thyristor", *IEEE Electron Device Letter*, p. 138-141, 1991.
- [PEZ 95a] PEZZANI R., QUOIRIN J.-B., "Functional integration of power devices, a new approach", *European Power Electronics (EPE'95)*, p. 2219-2223, Seville, Spain, 1995.
- [PEZ 95b] PEZZANI R., BERNIER E., Programmable protection circuit and its monolithic manufacturing, patent number: RE 35 854, 1995.
- [PEZ 96] PEZZANI R., Monolithic semiconductor switch and supply circuit component, patent number: 5 883 401, 1996.
- [PEZ 97a] PEZZANI R., BERNIER E., BALLON C., "A methodology for the functional power integration. Example, the evolution of the solid state protection in the Telecom area", *European Power Electronics (EPE'97)*, p. 1296-1301, Trondheim, Norway, 1997.
- [PEZ 97b] PEZZANI R., Three-state monolithic static switch, Patent number : 5 883 500, 1997.
- [PEZ 97c] PEZZANI R., Thyristor control switch for a bidirectional motor, Patent number : 5 889 374, 1997.

- [RUM 85] RUMENIK V., “Power devices are in the chip”, *IEEE Spectrum*, p. 42-48, 1985.
- [SAN 90] SANCHEZ J.-L., LETURCQ P., “Thyristor à gâchette isolée planar haute tension (1400 volts) : un exemple d'interrupteur intégré de puissance”, *EPF'90*, Toulouse, 1990.
- [SAN 97] SANCHEZ J.-L., AUSTIN P., BERRIANE R., MARMOUGET M., “Trends in design and technology for new power devices based on functional integration”, *European Power Electronics (EPE'97)*, p. 1302-1307, Trondheim, Norway, 1997.
- [SAN 99a] SANCHEZ J.-L., “State of the art and trends in power integration”, *MSM*, p. 20-29, Puerto Rico, USA, 1999.
- [SAN 99b] SANCHEZ J.-L., “State of the art and trends in power electronics”, *MSM*, p. 20-29, Porto Rico, USA, 1999.
- [SAN 99c] SANCHEZ J.-L., BREIL M., AUSTIN P., LAUR J.-P., JALADE J., ROUSSET B., FOCH H., “A new high voltage integrated switch: the ‘thyristor dual’ function”, *International Symposium on Power Semiconductor Devices and ICs, ISPSD'99*, p. 157-160, Toronto, Canada, 26-28 May 1999.
- [SAN 99d] SANCHEZ J.-L., BREIL M., LAUR J.-P., AUSTIN P., JALADE J., ROSSEL F., FOCH H., “Functional integration for new power switches design: example of the ‘thyristor dual’ function”, *8th European Conference on Power Electronics and Applications, EPE'99*, Lausanne, Switzerland, 7-9 September 1999.
- [SAN 99e] SANCHEZ J.-L., LAUR J.-P., M. Marmouget, AUSTIN P., JALADE J., BREIL M., ROY M., “A new circuit-breaker integrated device for protection applications”, *International Symposium on Power Semiconductor Devices and ICs, ISPSD'99*, p. 315-318, Toronto, Canada, 26-28 May 1999.
- [TEM 86] TEMPLE V.A.K., “MOS controlled thyristor – a new class of power devices”, *IEEE Transactions on Electron. Devices*, vol. ED-33(10), 1986.