Power Electronics Semiconductor Devices
Edited by Robert Perret
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Chapter 8

Power Electronics and Thermal Management

This chapter is devoted to the thermal environment of silicon chips, which is vital during the design of converters.

8.1. Introduction: the need for efficient cooling of electronic modules

The field of power electronics concerns the conversion of electrical energy. Produced mainly by an AC sinusoidal current (50 or 60 Hz), this energy must be adapted to the requests of users. The fields of application of power electronics are large and they range from large industrial powers (electrochemistry, electrometallurgy), to battery chargers of a few watts, which are increasingly used in mobile devices.

Many applications requiring variable frequencies (variation of speed by electric drives, induction heating), or continuous voltages of different values (the continuous transformer does not exist), will also make use of power electronic static converters. Finally, it is often useful to have a high frequency intermediate circuit (from some 10 kHz to about 100 kHz) to reduce the size of passive elements of a converter and consequently to increase the compactness of the devices.

In all these applications, efficiency is absolutely necessary: power electronics differs from traditional electronics. The main constraint of the latter is to preserve

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the integrity of a signal. The technologies of components used for these two disciplines are often very different.

The formatting of electric power is often based on a switching technique, the electronic component working as a fast switch. By controlling the duration of the on-state (the switch conducts), and of the off-state in a periodic process (Figure 8.1), the treatment of electric energy is processed in order to make the characteristics of the source compatible with the characteristics of the load.

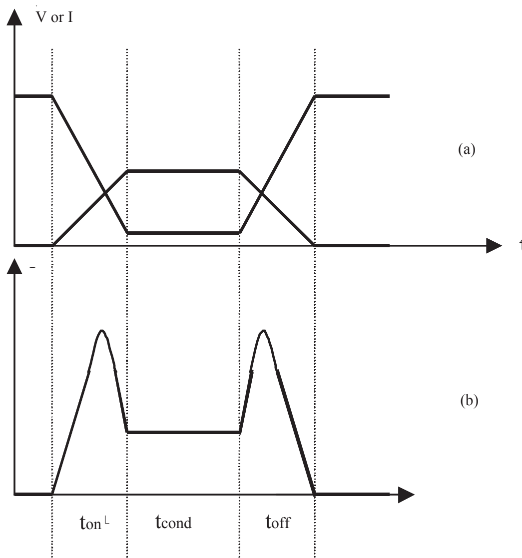


Figure 8.1. *a) Waveforms of voltage and current in a switch; b) instantaneous power dissipated in the switch*

We see in Figure 8.1a that when the switch is conductive, a residual voltage persists at the terminals of the component: this is the cause of conduction losses. Another phenomenon appearing during commutations: at switch-on, there is a time t_{on}, during which there is both a voltage higher than the residual voltage, and a current. Following this is an important instantaneous power (Figure 8.1b) and therefore an expenditure of energy at each switch-on. The same is true for closure, during the time t_{off} [TAN 97].

At blocked-state, in normal operating conditions (Tj < 125°C), leakage currents generate losses that are generally negligible, hence the existing components can be

regarded as perfect. The energy dissipated in the chip can be calculated by integrating the instantaneous power for each period.

Now consider the elementary case of a switching power supply DC/DC whose principle scheme is given in Figure 8.2a.

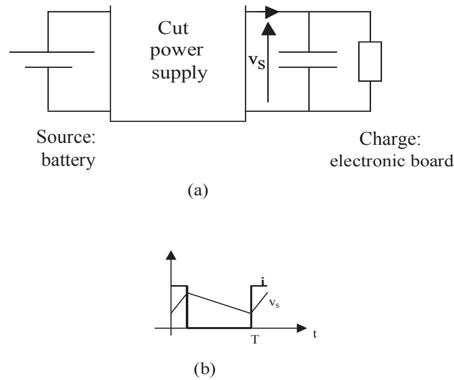


Figure 8.2. *a) Schematic of a DC/DC switching power supply; b) forms of current and voltage*

In this example, we can make a cut on the current i, as shown in Figure 8.2b. The aim is to have a voltage v_s "as continuous as possible". This is achieved with a filter whose RC time constant is the greatest possible compared to the switching period T. It is therefore obvious that as period T shortens, the filter is reduced, that is to say that RC is small, hence the interest of high-frequency (for power electronics, we refer to form kHz to MHz).

As a drawback, the dissipated power during commutations increases proportionally to the frequency. Faster components are therefore (reduced t_{on} and t_{off}) and/or circuit techniques with shifting current and voltage front edges (aids circuit to the commutation, [FOC 98, ROU 90] to reduce as many losses as possible.

It is also necessary to cool the component to maintain its temperature at an appropriate value for operation. The silicon components allow for a maximum temperature of about 120°C to 150°C (note that industrial applications do not exceed 125°C in order to respect the rules of reliability) [MER 00].

Before tackling our main interest, thermal design of the micro-cooler by fluid heat transfer, we will present, in this chapter, the main characteristics of power components that are vital for an understanding of our "all silicon" approach to be

discussed in section 8.2. Finally this chapter will conclude with a reiteration of the heat laws that will be used later in the study.

8.2. Current power components

8.2.1. *Silicon chip: the active component*

Power electronics began with junction components, namely diodes, bipolar transistors and thyristors. Over the past decade, the development of power semiconductors has incorporated isolated grid components (MOS, IGBT). For this last family of components we will design coolers considering currents of 100 A and voltages of about 1 kV. The components of this range typically have the following dimensions: 1 cm × 1 cm for a thickness between 250 and 500 µm. Thus the losses will be generated in the volume of a few tens of mm^3. To evacuate them, given the presence of connections and electrical insulation, only the underside (of 1 cm^2 in this example) is available. A characteristic assembly cross-section for this type of component is shown in Figure 8.3.

We will now consider the origin of individual losses and list the main difficulties encountered to limit them.

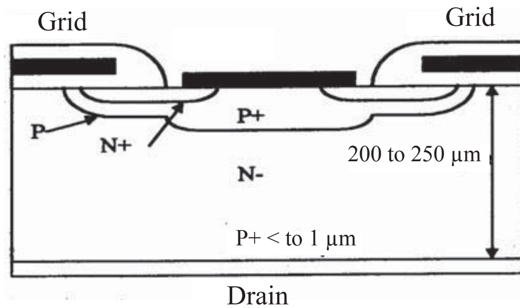


Figure 8.3. *Cut of the silicon chip of an IGBT*

8.2.1.1. *General construction of a power component*

A power component is mainly designed for its voltage strength, which is provided by a layer of silicon slightly doped N^-(10^{13} cm^{-3} to 10^{14} cm^{-3}; resistivity 100 Ω.cm); and relatively thick (a few hundred µm) area of voltage holding. As components of power electronics are of vertical type, this area has a current flow. To make the device a conductor, mobile n or p-type carriers must be injected in vast quantities into the voltage holding area. In the example of a diode, the density

$p = 10^{17}$ cm^{-3}. The presence of this area partly explains the residual voltage, which is even bigger when the voltage to be held during the blocking state is greater. In power components, you obtain residual voltages in the range of 2 V. With a common current density of 100 A/cm², conduction losses are around 200 W/cm².

For these injected charges to complete the role described above, they should not recombine in the voltage holding area. Thus, the length of diffusion must be of the same order of magnitude as the thickness of the area, which corresponds to an important lifetime of p carriers. The presence of the stored charge, which must be injected and eliminated, explains the phenomena observed at switch-on and switch-off. The design of components is therefore a delicate compromise, between residual voltage and importance of stored charge, which directly drives the speed of the power current [ARN 92, LI 98].

8.2.1.2. *Modeling conduction losses*

Whatever the nature of the power component (bipolar, unipolar, mixed), there is, during the conduction, a law between the voltage drop at the terminals, the conduction current and the temperature of the active part, [FAR 94]. The graphs shown in Figure 8.4 clarify the linkages between these three values for three IGBT of the same family. They show the influence of compromises made by the manufacturer between increased speed and reduced voltage drop (voltage existing on terminals of component when in the on-state). The fastest IGBT, Ultrafast, has a dropout voltage almost twice as large as the standard IGBT.

To calculate losses, the characteristic I(V) is usually modeled by a classic linear law:

$$Ve = V_0 + r_0 I$$

where V_0 represents the threshold voltage, and r_0 the dynamic resistance.

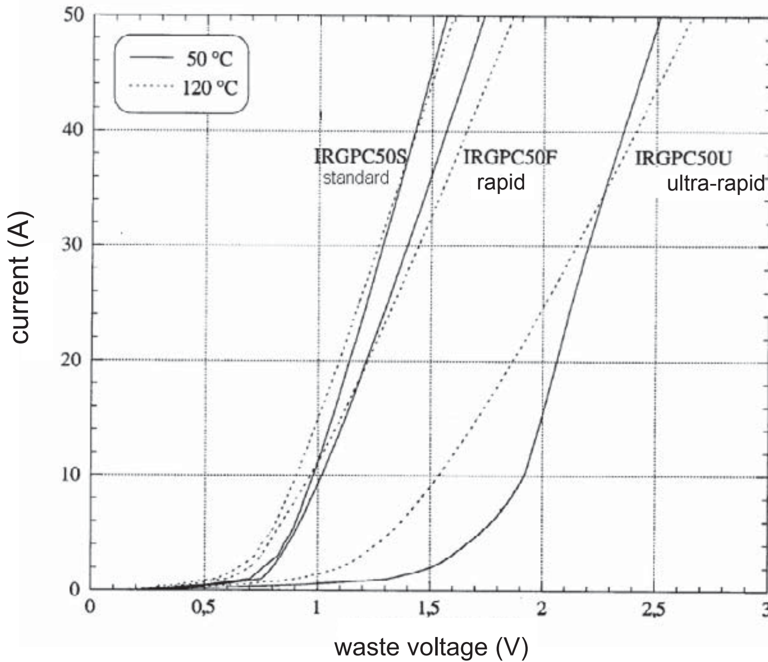


Figure 8.4. *Direct characteristics of standard IGBT, fast and ultra fast at 50°C and 120°C*

As the characteristics of Figure 8.5 show, these parameters change with the temperature of the active part of the component. V_0 decreases with temperature Tj of the area while r_0 increases.

To translate this dependant relationship, we write:

$$V_0 = V_{00} - aTj$$

$$r_0 = r_{00} + bTj$$

From tests run under at least two temperature values, it is possible to identify the values of the four parameters and thus calculate the losses of conduction for a given temperature. If the latter is unknown, we can proceed by iteration.

In conclusion, for the conduction phase, it is quite easy to have a general formula for losses if the temperature and current imposed by the external circuit are known.

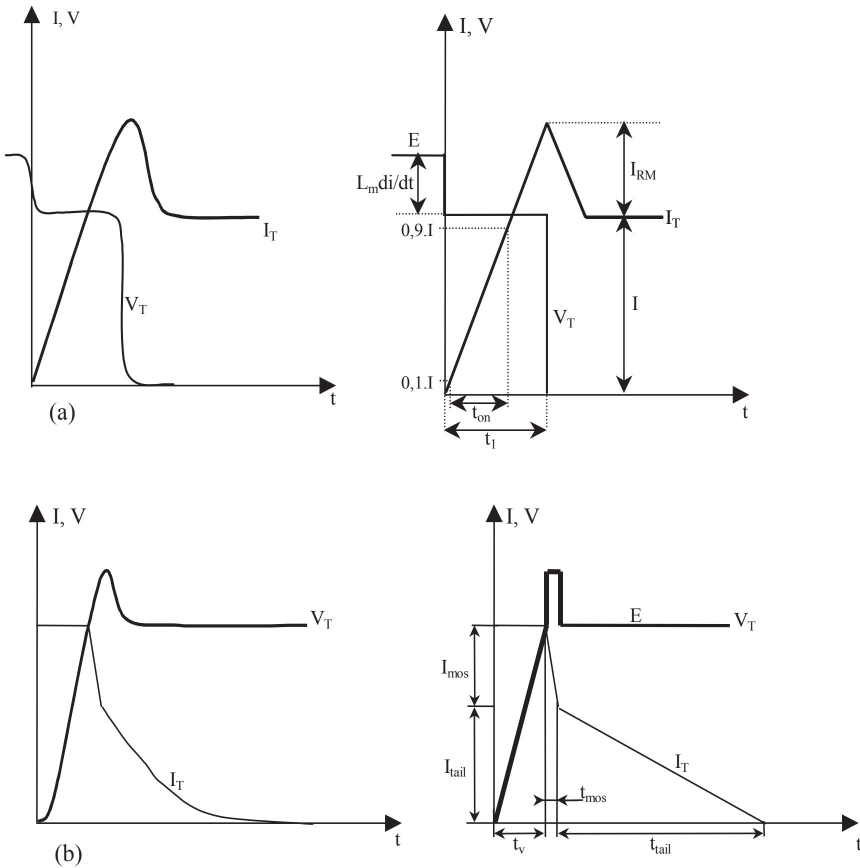


Figure 8.5. *Actual and modeled voltage and current waves, at (a) the closure,and (b) the opening of transistor T of an elementary switching cell (see Figure 8.6)*

8.2.1.3. *Modeling of commutation losses*

For this type of operation, determining losses by a general formula is far more difficult because current and voltage waveforms depend both on electronic components, on their command, on the type of commutation used, and on the external circuit including parasitic elements. Figure 8.6 gives respectively real waveforms and modeled waveforms obtained at the closure and opening of an IGBT, switching with a diode in the case of an elementary switching cell, where L_M represents the parasitic inductance of the mesh (Figure 8.6).

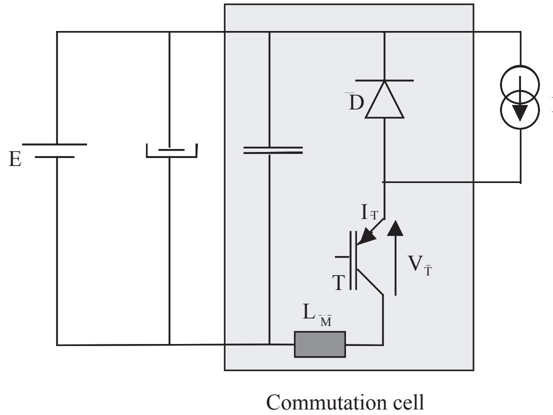


Figure 8.6. *Elementary commutation cell*

In his thesis, S. Raël [RAE 97] offers empirical formulae for estimating the value of energy dissipated in an IGBT at opening (W_{off}) and at closure (W_{on}) (see Figure 8.6).

At closure:

$$W_{on} = k_{on}.E.I\text{-}k'_{on}.I^2 \quad \text{with:} \quad k_{on} = 0{,}4.\frac{t_1^2}{t_{on}}$$

where t_1 and t_{on} are times illustrated in Figure 8.5a.

At the opening, waveforms are more complex and depend very much on the nature of the IGBT used, including the importance of the tail current (current that flows after the end of the grid command and is characterized by I_{tail}). In the experiment described above, we obtain:

$$W_{off} = k_{off}\,EI + k'_{off}I^2$$

$$\text{with:} \quad k_{off} = \frac{t_v}{2} + \frac{2\beta+1}{2(\beta+1)}t_{mos} + \frac{\beta}{2(\beta+1)}t_{tail}$$

$$\text{and:} \quad k'_{off} = \frac{2\beta+1}{2(\beta+1)^2}L_m$$

$$\beta = \frac{I_{tail}}{I_{mos}}$$

With the approaches and characterizations of switching components on an identified circuit (the role of command, of inductance Lm) we obtain formulae for predicting the losses of commutation.

Previous works showed that the values of various parameters also change with temperature (Figure 8.7).

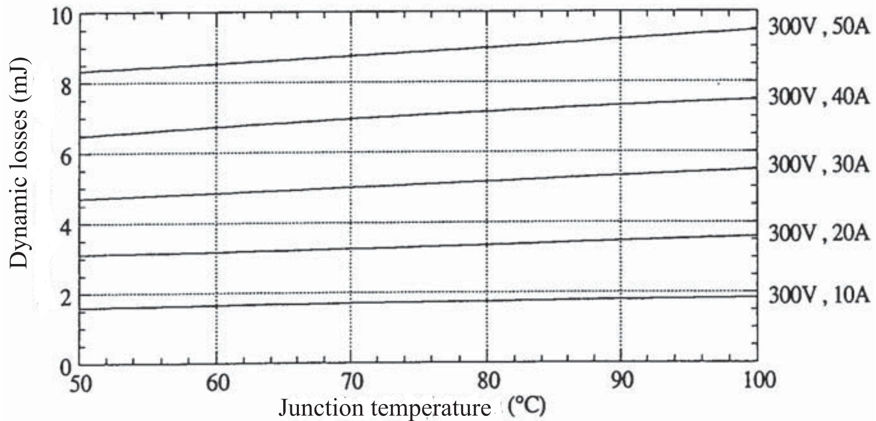


Figure 8.7. *Dynamic losses of a fast IGBT, depending on temperature*

We see that for a component IRGPC50F operating at 300 V, 50 A and 100°C, the losses are around 10 mJ per commutation. Such a component operating at 10 kHz dissipates, therefore, by switching a power of about 100 W, which is quite comparable to the energy dissipated during conduction when the conduction time and blocking time are equal.

8.2.1.4. *Conclusion*

The studies outlined above show that in modern electronic power components, for the voltages and currents considered, energies lost by switching and conduction are of the same order of magnitude: lost power to be evacuated on the rear panel of the silicon chip can reach 300 to 400 W/cm².

8.2.2. *Distribution of losses in the silicon chip*

A question is often asked: how are the losses located in the volume of silicon and, therefore, how is the temperature distributed within the component?

This is a complex issue because losses depend on temperature, which depends itself on cooling [FAR 94, HSU 96].

Losses may be developed in the vicinity of junctions, in load space areas, or in the area of voltage holding, creating for instance very localized hotspots. Measurements of component temperature were taken by an infrared camera, giving an accurate picture of the temperature at each point on the surface, thus establishing a temperature distribution map. The typical gap between the maximum and minimum temperature of a component of 1 cm^2 can reach 30°C.

Knowing and taking into account the allocation of losses and the mapping of temperature in silicon are both interesting and important when considering the electro-thermal behavior of a component, especially in the case of serial or parallel associations, but also for the behavior of components in transitional systems [MAN 97].

If the objective is the design of a cooler adapted to power electronics, able to dissipate 300 to 400 $W.cm^{-2}$, the precise location of losses is not a determining factor: the electronic power component will then be regarded as a surface, uniform, and homogeneous source of heat. The temperature of the chip, known historically by by the incorrect terminology "junction temperature" is defined as the average volume temperature at each point (x, y, z) of the volume of the chip.

$$T_j = \frac{1}{V_p} \iiint T(x,y,z)\,dV$$

where Vp is the volume of the chip.

8.3. Power electronic modules

8.3.1. *Main features of the power electronic modules*

The "bullet" of silicon in which the component is manufactured cannot be used alone, it must be mounted. Figure 8.8 represents a multi-layer cross-section view of a classic power module.

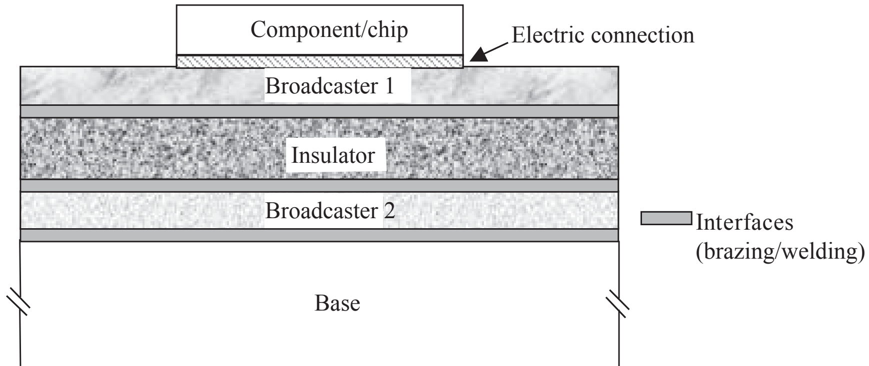


Figure 8.8. *Typical cross-section view of a power module*

As can be seen in Figure 8.8, the classic assembly consists of five layers of different materials, each is linked to the others by a very thin transition (brazing, welding), called an interface. Each of these layers has a particular role.

The first broadcaster (broadcaster 1) is directly under the chip. It must be a good electrical conductor, since it performs the electrical connection between the back of the chip and the outside, but must also be a good heat conductor: it takes part in the evacuation of the heat generated in the chip by allowing the flow of heat to spread and thus to benefit from the increased exchange surface. In the conventional modules, the broadcaster is copper, a material combining the two qualities.

Under the first broadcaster, there is electrical insulation. Its role is to electrically isolate the component from the rest of the module, and in particular from the associated cooler. It also provides electrical insulation between the various components of a single module when, for example, several IGBT are mounted in parallel. The material used must be a sufficiently strong insulator to withstand the voltages applied, but it must also have enough thermal conductivity to allow heat evacuation. Finally, it must have good combination capabilities with copper. The most efficient material seems to be the aluminum nitride (AlN), so that it is currently most often used in modules.

The second broadcaster which is a link with the base (commonly copper), enables good mechanical support, and its rear provides a link with the outside environment, especially with the heat exchanger.

All these materials are assembled together by welding or brazing. These joints have a low thermal conductivity, rather strongly degrading the ability of the module to dissipate the heat generated by the chip.

The module is covered with silicone and the whole is encapsulated in a plastic casing, with the exception of the rear of the basement which will exchange heat with the outside world.

8.3.2. *The main heat equations in the module*

The flow of heat through the module, from the chip to the rear of the basement, flows by conduction: heat transfer from one region to another is due to the temperature difference between these regions. As we have seen above, we consider that the component delivers a uniform heat flux. This flow P, represents the amount of heat crossing a surface per unit of time (expressed in watts):

$$P = dQ/dt$$

where dQ is the amount of elementary energy issued during an elementary time dt.

The heat density vector is also defined, φ, expressed in $W.m^{-2}$, characterizing for each point the direction and the intensity of the heat flux.

$$P = \iint_S \vec{\varphi}.\vec{n}.dS$$

and we write Fourier's law:

$$\vec{\varphi} = -k.\overrightarrow{grad}(T)$$

where k is the thermal conductivity of the material flowed. This is expressed in $W{\cdot}m^{-1}{\cdot}K^{-1}$.

By applying to an element of volume the first principle of thermodynamics and the law of Fourier, and making the assumption that the thermodynamics transformation is under constant pressure, the equation of the heat conduction is established for an isotropic body:

$$\rho C_p \frac{\partial T}{\partial t} = div(k\, grad(T)) + q$$

where ρ is the density, Cp the calorific capacity, k the thermal conductivity, and q the volume density of internal sources.

The thermal conductivity k depends on the temperature of the material, which does nothing to simplify the processing of previous equations.

For silicon: $k = 150\ W{\cdot}m^{-1}{\cdot}K^{-1}$ at 25°C, then it decreases as the temperature increases to reach $k = 100\ W{\cdot}m^{-1}{\cdot}K^{-1}$ at 125°C. To overcome this difficulty, one may assume a linear variation for a range of temperatures, or set an adapted constant value.

The importance of choosing materials with good thermal conductivity for the design of the module is clear, as is the negative influence of interfaces. Indeed, since the latter has low thermal conductivity, they are subject to strong temperature gradients that degrade the ability to evacuate the heat by conduction of the module.

To characterize the heat exchange that takes place between the chip and the base, we introduce the concept of thermal resistance, R_{th}, by analogy with the electrical resistance. It links the rise of temperature of the chip, T_j, with the ambient temperature T_a, for a dissipated power P. In permanent operation, it is given by:

$$R_{th} = \frac{T_j - T_a}{P}$$

This resistance is expressed in $K{\cdot}W^{-1}$. The more thermal resistance reduces, the more the chip produces a low heating due to dissipated losses.

Take for example the standard IGBT from Figure 8.8: the thermal resistance of the housing is $0.3K{\cdot}W^{-1}$. For a switching operation corresponding to a dissipation of 100 W, the heating of the chip obtained for a perfect cooling of the base would be 30°C.

In practice, the temperature control on the back side of the base is provided by a cooler, and is qualitatively characterized by a thermal resistance R_{thra}. For example, a standard air cooler has a resistance of $2K{\cdot}W^{-1}$. The IGBT, in the previous example, would, therefore, heat up to 230°C, which is not acceptable for a silicon chip. If we want to limit the heating to 60°C, for example, a cooler with a thermal resistance of less than $0.3\ K{\cdot}W^{-1}$ is required. It may be another air cooler, larger or better ventilated than the previous one.

Thus, we see that to take the current indicated by the manufacturer, an adapted cooler is required. More, the installation of a cooler whose thermal resistance would be $0.05\ K{\cdot}W^{-1}$, a water cooler for example, would allow the recommended current of 15 A to be exceeded, even doubled, for a temperature of 60°C [GIL 99, SCH 99].

The distribution of heat flow and temperature inside the module is completely conditioned by the heat exchange which will take place between the rear of the basement and the environment, i.e. ambient air or the associated cooler, the exchange being a convection.

8.3.3. *Cooling currently used for components of power electronics*

We have seen that postponement of housing the cooler is absolutely necessary, and may even be very beneficial in terms of increasing nominal current or operating frequency.

There are several kinds of coolers, but the principle is the same for all: submit a maximum exchange surface with a fluid that will absorb the heat. The exchange is by thermal convection, which is a process of transferring energy through the movement of molecules. We talk about natural convection when this movement is due to a simple difference in temperature within a space (the hot air going up, leaving room for cold air, for example) and forced convection when the movement is imposed by external action, by a pump or a fan.

This book does not look at the mechanics of fluids in a precise manner, but only to the heat exchange between the solid wall and fluid defined by a coefficient linking the heat flux φ through the wall and its temperature. The coefficient is called the coefficient of thermal exchange, h, and is defined as follows:

$$h = \frac{\varphi}{T - T_a}$$

This coefficient is expressed in $W \cdot m^{-2} \cdot K^{-1}$. We will return to this coefficient with more details in the following section.

In most cases, in power electronics, coolers are air type, forced convection, or water type. Water was chosen for its very good thermal capacity and its very simple use. It can be used in a closed loop, as long as the increase in temperature between input and output channels is controlled, which is very interesting in the case of embedded systems. On the other hand, water is not a good electrical insulator, and the establishment of an electrical insulator between the base and the cooler is often necessary. To avoid this insulation layer, which degrades the thermal performance of the housing, the water can be deionized. We can also make use of dielectric fluids (inert fluor, liquid nitrogen, etc.). Handling is cumbersome and low gain in terms of thermal performance compared to the design involving a layer of insulation makes their use unfavorable.

When the fluid is chosen, there are two possibilities for forced convection. It may be single or double phase:

– In the case of a single exchange phase, the fluid, liquid or gaseous, does not change phase during its circulation in the cooling device. A pump imposes a speed and its temperature rises as it progresses in the cooler. A compromise must be found between the speed of the fluid (including a best value which maximizes the evacuation of the heat) and the loss of pressure in the channels which are directly proportional to the cost and size of the pump.

– In the case of a double phase exchange, the heat absorbed modifies the state of the fluid which rises from the liquid state to a gaseous state: liquid and steam coexist [HEW 69]. Under the effect of heat, the temperature of the liquid rises to reach the saturation temperature, the liquid will then begin boiling. A secondary cooling system called the condenser cools the steam, thereby reducing fluid in the liquid state. These coolers have good performances, but they are not yet widely used in power electronics, mainly because of their design difficulty [MEY 98].

After going through the different techniques of coolers, we will speak now about a copper channel cooler, operated by forced convection water, single phase, because it is at present the cooling device most responsive to the needs of power electronics (e.g. size, performance, instrumentation) [TUC 81].

To increase the exchange surface (S_c), for a given chip surface (S_p), channels are designed in the copper base. In this case, the exchange surface Sc is defined as the sum of all channel surfaces: S_c = number of channels x length x width x height, i.e. $S_c = n \cdot l_c \cdot D \cdot L_y$. These parameters are defined in the schematic in Figure 8.9.

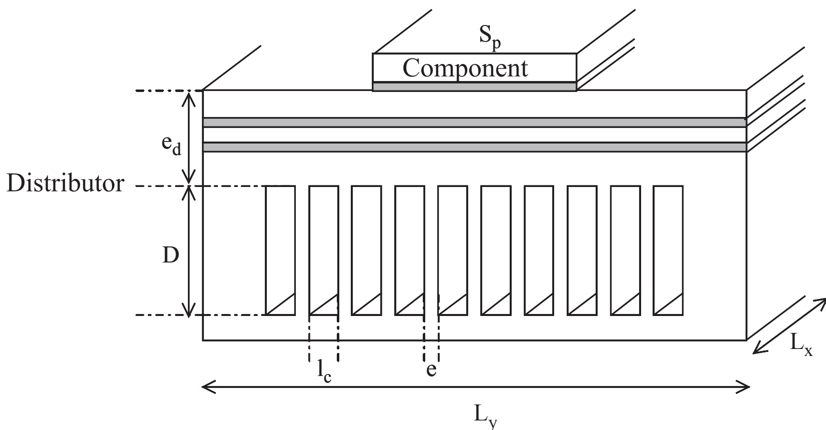


Figure 8.9. *Layout of a copper cooler including key geometric parameters*

The water flows through these channels. The performances are as follows: with a pump of 0.9 W power, the water flow is 1.3 $l \cdot min^{-1}$ for a loss of pressure of about 0.4×10^5 Pa. The cooler is able to evacuate a power corresponding to a reduced density on the component $350 W \cdot cm^{-2}$ for a junction temperature rise of 60°C. These results are obtained from a configuration where the chip and the water are not electrically isolated from one another. The cooler has been designed in LEG in collaboration with the CEA/GRETh and Alstom ([RAE 97] and [MEY 98]).

The performance of such coolers was further improved by C. Gillot who proposes double-sided cooling in his thesis [GIL 99].

This cooling method is very effective, but as we shall see, it has several drawbacks which we would like to overcome in this study.

As we have said previously, there are several layers of different materials between the chip and the cooler: silicon chip, copper broadcaster, AlN of insulation and different solders (Figure 8.8), and finally the copper cooler. All these interfaces deteriorate thermal performance and generate mechanical fatigue: the different materials have different thermal behaviors since they do not have the same coefficient of thermal expansion, thereby reducing the lifetime of the system by thermal fatigue.

In addition, the cooler is carried out in a copper base whose weight can be a problem, especially for use in embedded systems.

Finally, with this type of cooler, as with coolers of older generations: the component and the cooler are designed independently of one another, limiting the manufacturer of component for the level of the maximum current; and thus excluding the hypothesis of a collective achievement of an integrated converter, where you could find in a single bloc, the power part, the command and the cooler.

For these reasons, and especially the latter, this question was proposed as the subject for a thesis, and a "*full silicon*" type solution was suggested.

8.3.4. *Towards an "all silicon" approach*

The design of a full silicon cooler has been studied in the thesis of [PER 01]. Indeed, this new approach can solve a number of problems encountered during the implementation and use of copper micro-coolers. Although from a purely thermal point of view silicon is less efficient than copper (its thermal conductivity is almost two and half times lower ($150 W \cdot K^{-1}$ compared to $360 W \cdot K^{-1}$), it nevertheless

presents several advantages providing for consideration a micro-cooler with good performances in several respects.

First, the mechanical strength of silicon and the methods of engraving allow the creation of channels and fins whose critical dimensions (width, depth, etc.) are much smaller than those supported by copper. This allows a considerable increase in the exchange surface available for a given chip surface. Although it is more difficult to handle, being more fragile, the silicon micro-cooler has the advantage of being lighter than copper.

However, the greatest advantage of this cooling technique is without doubt that it involves the use of a single material: the chip and its cooler are both in silicon. Either the chip is carried on a silicon base on which channels will have been etched, or channels are made directly into the back of the chip. Indeed, the achievement of micro-coolers is fully compatible with a classic CMOS technology. All this leads to two positive important advancements: the chip can be delivered directly from the white room with its integrated and adapted cooler, and all problems of thermal fatigue are eliminated at the same time as with the different solders that are usually inserted between heating and cooling sources. This is also a way to consider the components of high integration we are talking about. Many works are underway to achieve this [SAN 97].

Finally, as we said earlier, the establishment of a dielectric layer between the chip and the refrigerant fluid, in the case of copper, degrades thermal performance significantly. Here, the silicon can again provides an improvement: the electrical insulation made by insertion of a thin layer of silicon oxide (Figure 8.10). This oxide has two advantages: it is a very good dielectric (low thickness is necessary) and its coefficient of thermal expansion is substantially the same as silicon: its presence does not therefore introduce significant thermo-mechanical constraint.

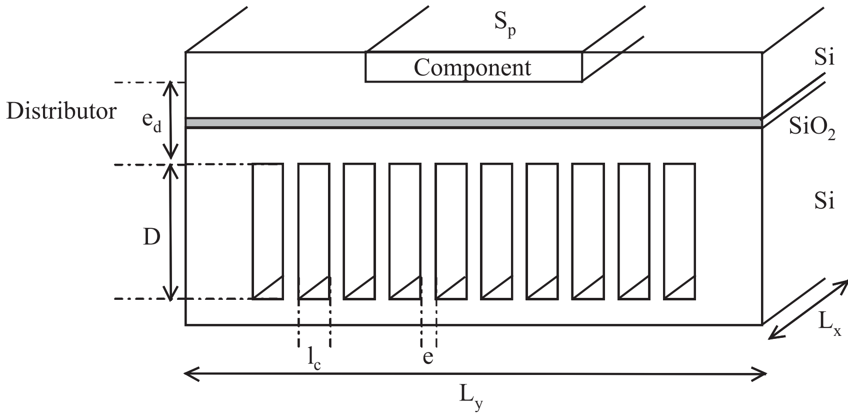


Figure 8.10. *Isolation of the electrical part from the thermal part by incorporating a layer of silicon oxide (of a few microns)*

To illustrate these remarks, therefore, we will study the cooling of a single chip, with the assumptions made above: the flow of heat is considered as an injection surface of heat in the cooler. The principle is water forced cooling, with mono-phase convection.

To give an idea of the size of micro-coolers, here are the magnitudes of each geometric parameter (Figure 8.10):

– D: depth of a channel: 400 to 800 µm;

– lc: width of a channel: 80 to 150 µm;

– e: width of a wing: 80 to 150 µm;

– Lx: length of a channel: 2 cm;

– Ly: width of a grid of channels: 2 cm;

– n: number of channels: 60 to 130.

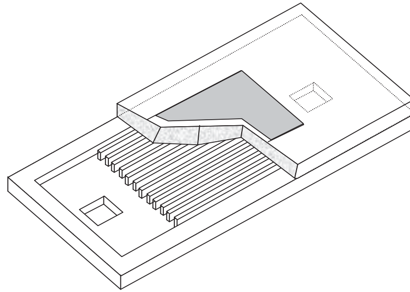


Figure 8.11. *Schematic of a cooler created in silicon*

Figure 8.11 presents a cross-section view of the cooler.

The fluid is water, chosen for its good thermal performance and its ease of use. We summarized in Table 8.1 thermal and hydraulic constants of water, coolant fluid used in this study.

Density ρ	995 $kg{\cdot}m^{-3}$
Viscosity μ	0.000651 $kg{\cdot}m^{-1}.s^{-1}$
Thermal conductivity kl	0.628 $W{\cdot}m^{-1}{\cdot}K^{-1}$
Calorific capacity Cp	4.178 $J{\cdot}kg^{-1}{\cdot}K^{-1}$

Table 8.1. *Thermal and hydraulic constants of water*

8.3.5. *Conclusion*

We have seen that power components are becoming more efficient in terms of speed, which compared with their losses appear to be constant or even increasing. In addition, compacting makes cooling more difficult. Significant progress has been made on the coolers that currently have good performances. However, designs of components and coolers remains independent, which is harmful. An approach integrating the cooler module is an attempt to answer this problem, with the "all silicon" approach being a step further in this direction.

8.4. Laws of thermal and fluid exchange for forced convection with single phase operation

8.4.1. *Notion of thermal resistance*

As we have already mentioned, the thermal resistance is analogous with the electrical resistance: where the electrical resistance connects the current to the fall of voltage between its terminals, thermal resistance establishes a link between the flow of heat entering a system and the temperature difference between two points of the system, hence the “thermal Ohm” law recalled here:

$$Rth = (Tj - Ta)/P$$

In our case, the evacuation of the heat is carried mainly by the cooler (radiation is neglected). The total thermal resistance is the sum of three terms:

– thermal resistance due to heat conduction through the R_{diff} of the broadcaster; the broadcaster as part located between the chip and the top of the channels (Figure 8.10). It is made from one or more materials as previously mentioned;

– convection resistance reflecting the exchange between the channel walls and the fluid, R_{conv}; and

– capacitive resistance representing a rise of temperature of the fluid between the channel input and output, R_{cap}.

8.4.1.1. *Thermal resistance of diffusion, R_{diff}*

Two cases are different in regard to the broadcaster resistance: the heat flow is unidirectional (resistance with one dimension), or it is two-dimensional (resistance with two dimensions). We define here two surfaces (Figure 8.12):

– the chip surface, S_p:

$$S_p = L_{px} \cdot L_{py}$$

– and the surface of the broadcaster cooler’s, S_d:

$$S_d = L_{dx} \cdot L_{dy}$$

where L_x and L_y are the dimensions of the chip and broadcaster.

The first case is relevant when the component and the cooler have the same size ($S_p = S_d$) and in the second when the cooler is larger than the component ($S_p < S_d$).

8.4.1.1.1. Dissemination resistance with one dimension

In the simple case of a single layer broadcaster, i.e. made of a single material, this resistance is the easiest to define, since it is only to describe the passage of heat flow through a uniform material (Figure 8.12.a):

$$R_{diff} = \frac{e_d}{k_d.S_d}$$

where e_d is the thickness of the broadcaster, k_d is the thermal conductivity expressed in $W \cdot K^{-1} \cdot m^{-1}$, and S_d the surface flowed by the flux.

In this case, it is easy to reduce the importance of this resistance by reducing the thickness of the broadcaster, within the mechanical limits of the system, of course.

When the broadcaster is made up of several layers, we add the dissemination resistances of each layer:

$$R_{difftotal} = \sum_{i=1}^{n} R_{diffi} = \sum_{i=1}^{n} \frac{e_{d_i}}{k_{d_i}.S_d}$$

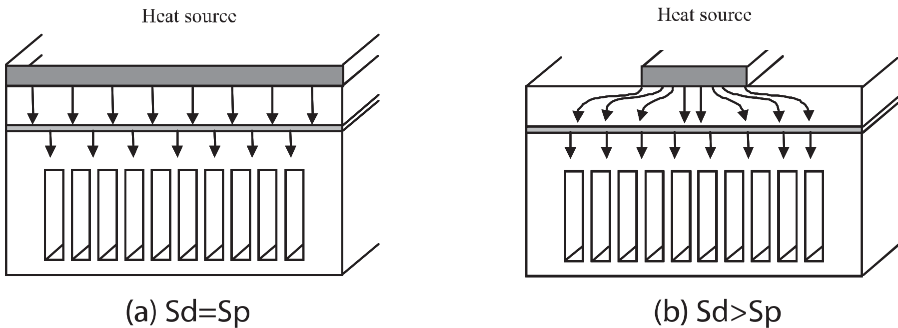


Figure 8.12. *a) Unidirectional heat flow, b) dissemination of heat flow*

8.4.1.1.2. Dissemination resistance with two dimensions

Let us study now when the heat flow is two-dimensional (Figure 8.12b). This occurs when the component is smaller than the cooler, and is amplified when the broadcaster incorporates a thermal barrier. As we have said before, to achieve a cooler where the silicon component and the fluid will be electrically isolated, we

will need to integrate a layer of silicon oxide inside the broadcaster. Due to its low thermal conductivity, this layer will cause heating, but it will also "slow down" the flow of heat and thus force it to disseminate in the area above it. The barrier is a negative result of the thermal cooler's performance, but a well-optimized design can reduce this defect. Indeed, if the surface of the cooler is sufficient and if the position of the insulation layer and its thickness are carefully selected, the exchange can be improved by the simple fact that the flow of heat encounters a bigger surface than in the cases of a one dimensional flow. We can now see that a compromise is required when adding an electrical insulator, between its thickness, its position in the broadcaster and the surface of the cooler. A more complete modeling must be effectuated for each configuration.

8.4.1.2. *Thermal resistance by convection, R_{conv}*

As we have said, convection means the exchange between the walls of channels and fluid. We defined above the concept of heat exchange coefficient h. The convection thermal resistance is inversely proportional to this coefficient:

$$R_{conv} = \frac{1}{h.S_c}$$

where S_c is the surface of heat exchange, i.e. the surface of the channel walls.

The difficulty in characterizing the heat convection is to determine the value of coefficient h. It depends on many parameters such as the convection mode (natural or forced), the geometry of the cooler (plan, with rectangular or circular channels, etc.), the nature of the flow (laminar or turbulent) and its thermal and hydraulic operation. It can be seen, considering the number of parameters, that there is no exact formulation of this coefficient for all cases. In general, its value is taken into empirical tables.

It is vital that the thermal resistance be improved to enhance the overall performance of the cooler. There are two methods using parallel to achieve the reduction of this thermal convection resistance: increasing the exchange surface S_c adapting critical dimensions of channels and fins, and increasing the thermal exchange ratio amending the form of channels, the flow system, and so on.

8.4.1.3. *Capacitive thermal resistance, R_{cap}*

This thermal resistance varies slightly from the other two: the first two take into account differences in temperature in the flow of heat plane, the latter is on the rise

in temperature of the fluid between the channel inputs and outputs, i.e. in a plane perpendicular to the flow of heat. This temperature rise is due to the amount of heat absorbed by the fluid during its passage. It depends on the nature of fluid, its calorific capacity, and the flow imposed on it:

$$R_{cap} = \frac{1}{2.m.C_p} = \frac{T_m - T_e}{P} = \frac{T_S - T_e}{2P}$$

In this equation, m is the mass flow of fluid, C_p its calorific capacity, T_e temperature of the fluid at the channel entrances, T_s the temperature of the fluid at the channel exits, and T_m the average of these two temperatures.

The thermal resistance must be limited especially in the structure we would like to use, the closed loop. In this case, a secondary cooling system is necessary to ensure the fluid entering the channels is always at the same temperature T_e. If the temperature of the fluid at the exit of the main cooler is limited, the secondary cooling circuit is simpler and less expensive.

8.4.1.4. *Square thermal resistance R_c*

To facilitate comparisons between the performances of different micro-coolers, designers are accustomed to using a thermal resistance per area unit, which they call square resistance R_c, expressed in $K{\cdot}W^{-1}{\cdot}m^{-2}$. We note for example:

$$R_{ctot} = R_{tot} \times S_p$$

with S_p, the surface of the heating source.

8.4.1.5. *Total square thermal resistance, R_{ctot}*

The total square thermal resistance is the sum of three square resistors:

$$R_{ctot} = R_{cdiff} + R_{cconv} + R_{ccap}$$

We can now see all the compromises that will be needed to reduce total thermal resistance without increasing too many other constraints: choice of the thickness of the broadcaster between dissemination and the thermal barrier; compromise between the reduction of critical dimensions and mechanical constraints; compromise between an increased rate of flow of the fluid, for a reduced rise in temperature, and a minimum loss of pressure; choice of flow system of the fluid, etc. All these issues will be resolved during the global optimization of the cooler.

8.4.2. *Laws of convective exchanges from a thermal and hydraulic point of view: the four numbers of fluids physics*

In the preceding section, we saw that the convection part is essential to the performance of coolers. In this part, we will revisit the laws calculating the coefficient of thermal exchange h and characterizing the fluid flow (loss of pressure, nature of the flow, etc.).

These laws are expressed in terms of four dimensionless numbers traditionally used by specialists.

8.4.2.1. *The Reynolds number*

The flow can be laminar or turbulent. In the first case, the fluid flows in the form of nets parallel to the walls; in the second, the concept of a net no longer exists, and the movement of fluid particles is uncertain.

To find the flow system, this Reynolds number, Re, must be incorporated, which depends on the density of the fluid ρ, its viscosity μ and the hydraulic diameter of the channels, D_h, as follows:

$$Re = \frac{\rho.v.D_h}{\mu}$$

with $D_h = \frac{4.s}{p} = \frac{D.l_c}{2.(D + l_c)}$ in the case of rectangular channels,

with s and p respectively the section and perimeter of the channel, D its depth and l_c its width.

This Reynolds number defines the transition from a laminar flow to a turbulent flow. The value corresponding to this transition is well established for channels and micro-channels (flow is laminar if Re < 2,300, otherwise turbulent, for channels of dimensions in the order of a millimeter). However, in the case of micro-channels (critical dimensions of about 100 microns or less), this limit is not clearly known. In literature, the hydraulic designers evaluate it, according to the methods used, from Re = 400 to Re = 5,000 ([MOH 97, PEN 94, ZHU 97]). That is why, as a first step, we will not make any assumption on the flow system instead we will try to determine it by a more experimental approach.

8.4.2.2. *The Prandtl number*

The flow can be established thermally and/or hydraulically. We talk about thermally or hydraulically established system, when the temperature profile, or the speed of the fluid in the channel no longer depends on its position along the channel. The distance between the channel entrance, and the position from which the profiles no longer evolve is called length of establishment. The Prandtl number, Pr, gives information on the establishment of flow. This dimensionless quantity is defined by:

$$Pr = \frac{\mu C_p}{k_l}$$

where μ is the viscosity of the fluid, C_p its calorific capacity and k_l its thermal conductivity.

For the design of coolers, the flow is always regarded as being thermally and hydraulically established. This assumption is necessary in order to facilitate the stationary state design. Knowing that the heat exchange is still slightly better when the flow is not established, if this hypothesis is not verified, the design result will simply underestimated compared to reality.

8.4.2.3. *Friction coefficient and pressure losses*

When considering a flow of fluid, there is also the loss of pressure between input and output of channels. This loss of pressure depends on the coefficient of friction C_f, speed v, density of the fluid ρ, length of the channels L, and their hydraulic diameter D_h, such that:

$$\Delta P = \frac{4.C_f.L}{D_h.}.\rho\frac{v^2}{2}$$

The coefficient of friction C_f, can be calculated by two empirical formulae, one for a laminar flow system:

$$C_f = \frac{4.7 + 19.64\,G}{R_e} \quad \text{with} \quad G = \frac{\left(\frac{D_h}{l_c}\right)^2 + 1}{\left(\frac{D_h + 1}{l_c}\right)^2}$$

where G is a dimensionless parameter determined experimentally, taking into account the form factor in the case of rectangular channels.

For a turbulent flow system:

$$C_f = (0.0929+1.01612\ Dh/L).Re^{-0.268-0.3193Dh/L}$$

8.4.2.4. *Nusselt number*

This number depends on the channel geometry and the nature of the fluid flow. In the laminar system and where the flow is established thermally and hydraulically, it is possible to calculate the Nusselt number analytically, as long as the speed profile in the channels is known, and then the heat equation is solved. In the case of cylindrical channels, it is relatively easy, but for more complex sections, such as rectangles, it quickly becomes complicated, and we prefer then to determine the Nusselt number empirically [TAI 89]. To this end, there are an array of experimental values of the Nusselt number according to ratios in formed channels [KAY 80]. It is possible, as demonstrated by [BEJ 84] to obtain from these experimental values, an analytical equation of Nusselt according to the geometric parameters of the channels. Two cases are distinguished:

– the four walls of the channels are involved in the heat transfer;

$$Nu = -1.047+9.326G$$

– the fourth wall, the bottom of the channel, is adiabatic;

$$Nu = -14.859 + 65.623\ G - 71.907\ G^2 + 29.384\ G3$$

These formulae are valid when we make the assumption that the flow of heat is uniformly shared on the walls involved in the exchange.

In the turbulent system, the Nusselt number is less sensitive to the geometry of the channels. There are many correlations to approach analytically approaching the Nusselt number. We consider those of [GNI 76] that are valid irrespective of the boundary conditions on the walls:

$$Nu = 0.0214.\ (Re^{0.8} - 100).Pr^{0.4},\ \text{when } 0.5 < Pr < 1.5 \text{ and } 10000 < Re < 5.10^6$$

$$Nu = 0.012.\ (Re^{0.87} - 280).Pr^{0.4},\ \text{when } 1.5 < Pr < 500 \text{ and } 3000 < Re < 10^6$$

The Nusselt number is directly linked to the coefficient of thermal exchange h by the formula:

$$Nu = \frac{h.D_h}{k_l}$$

This formula is valid in the case of rectangles, with $\delta = D_h/lc > 1$.

Depending on the nature of systems, we can draw curves $h(\delta)$:

$$h(\delta)=\frac{k_l.Nu(G(\delta))}{D_h(\delta)}$$

We note, while the coefficient of heat exchange h is growing with δ in the case of a laminar flow (Figure 8.13), it decreases in the case of turbulent flow (see Figure 8.14).

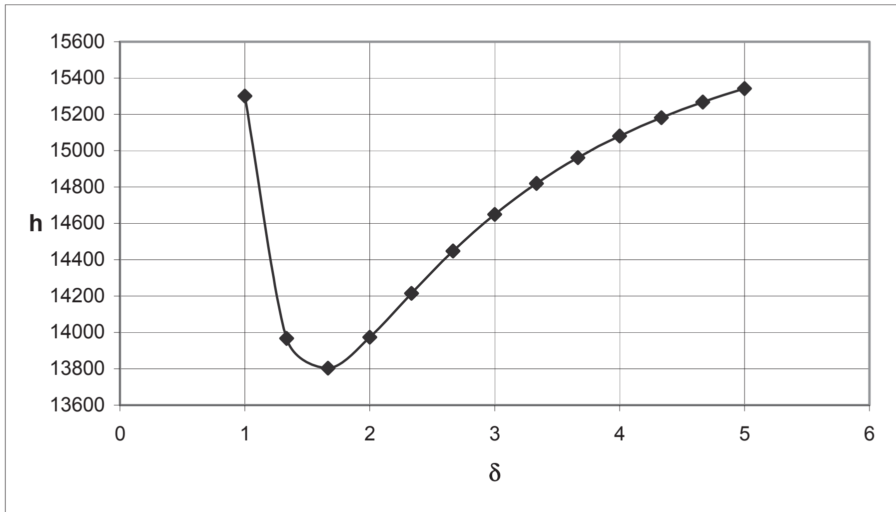


Figure 8.13. *Change of the coefficient of thermal exchange h according to the ratio $\delta = D_h/lc$ (depth divided by channel width) in the case of laminar flow*

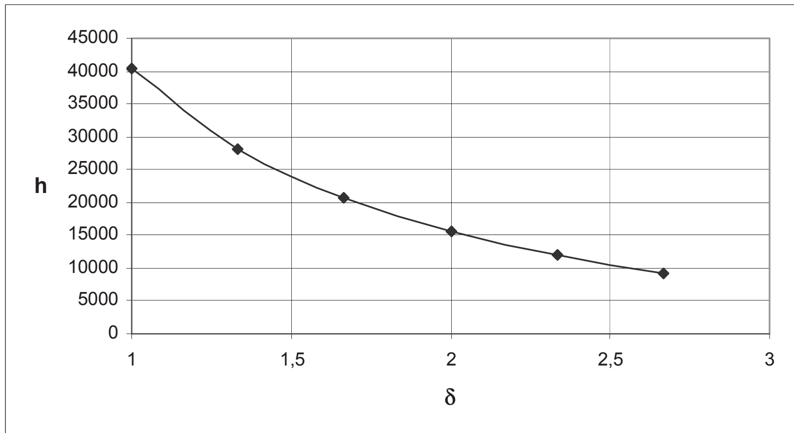


Figure 8.14. *D/lc change of the heat exchange coefficient h according to the ratio $\delta = D_h/lc$ (depth divided by channel width) in the case of a turbulent flow. Curve is limited to <2.5 because for higher values, flow becomes laminar*

There are several other formulae giving Nusselt values, which may be multiplied by 2, [BEJ 84, GNI 76, KNI 92, TAI 89]. All these formulae are provided with an error of 20%, and for areas corresponding to different Reynolds numbers.

$$Nu = 0.027.Re^{0.8}.Pr^{\,0.33}$$

The Nusselt number is directly linked to the square convection resistance since:

$$R_{convc} = \frac{1}{h} = \frac{D_h}{k_1 Nu}$$

8.4.2.5. *Conclusion*

In this chapter, we recalled key relationships that can aid the design of a micro-channel cooler with a coolant fluid. The more comprehensive calculation is done in the referenced bibliography. In the next chapter, we will develop the calculation of the distribution of temperature in the module, the cooler being represented by the exchange ratio h.

8.5. Modeling heat exchanges

To carry out this modeling, analytical methods are typically involved, as semi-analytical or digital methods. Below, we describe the two last approaches on examples treated within a research group.

8.5.1. *Semi-analytical approach*

Calculating of temperature distributions or heat flows in the operating devices, is based on solving the equation of heat in the three dimensions of the devices volume [PET 95, SZE 97]. However, solving this equation is generally not easy when one proposes to take into account the boundary conditions that are necessary for describing the realistic operating conditions that apply to this device for cases that have immediate practical interest. The heat equation is a partial differential equation. The analytical methods of solving the latter are essentially based on two techniques that can reduce the problem with three dimensions to a problem with one dimension. There are:

– methods based on the use of Green’s functions associated with real sources and image sources; and

– methods based on the use of integral transformations adapted to the lateral limit conditions set for the problem.

8.5.1.1. *The methods based on the use of integral transformations.*

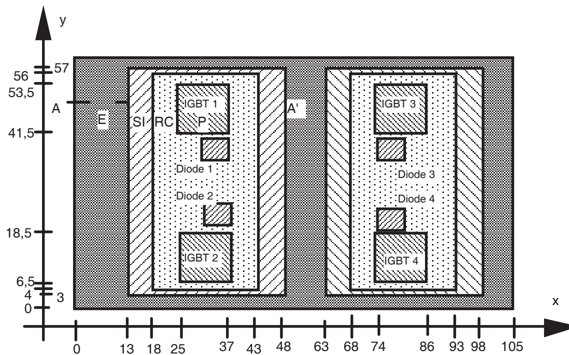
There are scopes for preferential application of each of these methods depending on the problem to be addressed. Thus, a problem where lateral limit conditions have little importance is easy to deal with using the first method (Green’s functions), while the second method (transformation) is more suited for solving problems where the lateral limit conditions play a crucial role.

Whatever method is adopted, the analytical solution is finally obtained in the form of a series involving more or less terms and, in cases of practical interest, can only be operated with numerical calculation. That is why we prefer to use the term semi-analytic method. In the following, we will show how it is possible to apprehend with realism, the calculation of distributions of temperature and heat flux, based on a semi-analytical method using the Fourier transformation. The structure on which this method can be applied is the already complex hybrid power module with several chips. The time needed to calculate the distribution of temperature or heat flow through the proposed method can be surprisingly short. For simplicity and

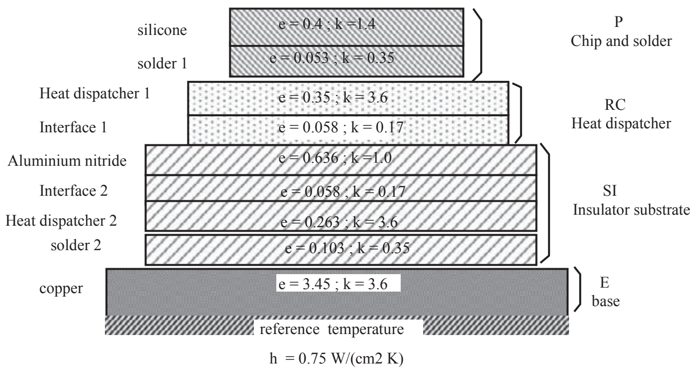
brevity, however we will reduce our demonstration, to the semi-analytic calculation of distributions of temperature obtained under the static system of power dissipation.

8.5.1.2. *Stating the problem – key assumptions*

Figure 8.15 provides a schematic overview of top views and cross-section views of a hybrid power module with IGBT and diodes. As shown in Figure 8.15b, it is assumed that this module is cooled in an effective manner on its underside because of the large power dissipation which is often characteristic of this device in normal operation [BEL 97].



(a) Top view (all sizes in mm)



(b) Cross-section view following AA' (e in mm, k in W·cm^{-1}·K^{-1})

Figure 8.15. *Schematic view of a hybrid power module*

From the thermal point of view, this module can be regarded as an assembly of various layers of rectangular form materials, characterized by different thermal conductivities and diffusivities. In this assembly we must also not underestimate the role of interfaces between layers, which even of practically negligible width, may have, because they are non-ideal, a considerable weight in the thermal behavior of the whole. If one considers the flow of heat dissipated in the active areas of the components, this will be in a preferred direction "z" while allowing the flow of heat to flourish more or less locally following the other two directions (x and y), depending on the flowed materials. It is assumed that the underside of the assembly exchanges heat with a heat sink, maintained at a temperature of reference. This exchange of heat is characterized by a convective coefficient of exchange, h, expressed in $W{\cdot}cm^{-2}{\cdot}K^{-1}$ and whose dimension is identical to the heat conductance per area unit, g, that characterizes the heat exchange between two adjacent layers separated by a non-ideal thermal interface.

If the cooling established at the bottom of the structure is really effective (forced air convection or circulation of a coolant liquid), one can ignore the heating power evacuated from the top and the side edges of the structure by natural convection and radiation. These last two mechanisms for the exchange of heat are indeed characterized by exchange factors that are very low if the temperature of the structure remains within acceptable limits in practice. In these circumstances, we may make a simplifying assumption, considering that all sides in contact with the environment are adiabatic, with the exception of the lower side which is in contact with the heat sink.

As the thickness of active zone (100 microns) is generally very small compared to the total thickness of the pile, it is convenient to consider that dissipated heat is on a surface rather than in a volume. This allows us to use a simplified form of the equation of heat, and impose the flow of heat as a limit condition on the surface at the limit of active zones, which are located in the immediate vicinity of the upper surface of the pile.

Moreover, if we considers the side view given in Figure 8.15b, it may be noted that a detailed analysis of the thermal behavior of the entire structure must take into account the fact that the latter is divided into parallelpiped blocks, each of them including multiple plane layers interfaced one over the other. Thus the analysis of the structure outlined in Figure 8.16 is used to identify 13 blocks which are:

– the eight chips and underlying welding (block "P");

– the two dispatchers of heat (blocks "RC");

– the two insulating substrates (blocks "SI");

– the copper base (block "E").

The mathematical formalization of the calculation of temperature across a structure as described in Figure 8.15 must therefore be divided into two stages:

– calculating the distributions of temperature and flow in each of the blocks which constitute the complete structure;

– taking into account the thermal interaction between various blocs according to their relative positions.

8.5.1.3. *Principle of calculating of temperature and flow distribution in a block*

Figure 8.16 shows the mathematical problem of heat flowing in a block [LET 93]. The distribution of heat flow is assumed to be known on the upper side (in the plane z = 0) and the distribution of temperature is assumed to be known on the underside of the block (in the plane $z = z_n$). We must first calculate the distribution of temperature at the top of the block, and the distribution of heat flow to the lower surface. When both values are determined, we can remove one or the other of these quantities in any internal plan of the block if necessary.

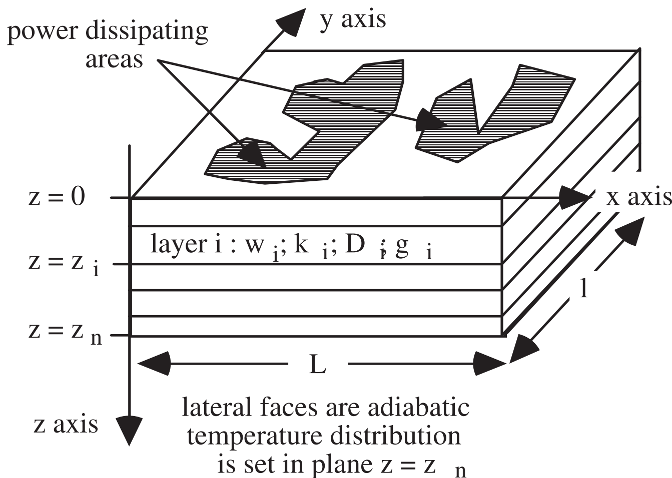


Figure 8.16. *Geometric and thermal description of a multi-layered block*

If the assumptions made above are correct – the flow of heat is imposed on the upper side of the block and the distribution of temperature is defined on the lower

surface, with the other sides of the structure being adiabatic – we must solve the following system of equations:

$$\begin{cases} \text{Heat equation in layer i: } \nabla^2\theta_i = 0 \\ \text{Thermal conductivity at interface i: } k_i \left.\dfrac{\partial\theta_i}{\partial z}\right|_{z=z_i} = k_{i+1} \left.\dfrac{\partial\theta_{i+1}}{\partial z}\right|_{z=z_i} \\ \text{Thermal conductivity at interface i: } \theta_{i+1} = \theta_i + \dfrac{k_i}{g_i}\left.\dfrac{\partial\theta_i}{\partial z}\right|_{z=z_i} \\ \text{Boundary condition in z = 0: } \mathrm{p}(\mathrm{x,y}) = -k_1 \left.\dfrac{\partial\theta_i}{\partial z}\right|_{z=0} \\ \text{Boundary condition in z = z}_\mathrm{n}\text{: } \theta_n(x,y,z_n) = \theta_{ref}(x,y) \\ \text{Boundary condition on lateral sides: } \left.\dfrac{\partial\theta_\mathrm{i}}{\partial \mathrm{x}}\right| = 0\,,\ \left.\dfrac{\partial\theta_\mathrm{i}}{\partial \mathrm{y}}\right| = 0\,,\ \forall \mathrm{i} \end{cases}$$

Using an appropriate linear transformation, we can transform in each layer the Laplace equation into a regular differential z equation. Given the boundary conditions on the lateral sides, this transformation is in this case turned into a double cosine transformation which must be applied to distributions of temperature $\theta_\mathrm{i}(x, y, z)$ [DOR 96] as follows:

$$\Theta_i(n_x, n_y, z) = \frac{1}{Ll}\int_0^L\int_0^l \theta_i(x,y,z)\cos\left(n_x\frac{\pi}{L}x\right)\cos\left(n_y\frac{\pi}{l}y\right)dxdy$$

Laplace equations in each layer i are transformed into:

$$\frac{d^2\Theta_i}{dz^2} = m^2\Theta_i \quad \text{with} \quad \mathrm{m}^2 = \left(n_x\frac{\pi}{L}\right)^2 + \left(n_y\frac{\pi}{l}\right)^2$$

where n_x and n_y are wave numbers, with theoretical values between 0 and infinity, and m can be defined as a spatial pulse.

As the double cosine transformation is linear, all conditions of continuity and boundary conditions defined for distributions of temperature and flow also apply to transformations of these distributions. The solution of the equation for the layer i can be written:

$$\Theta_i(m, z) = C_i(m)e^{+mz} + C_i'(m)e^{-mz}$$

For a solution, we should in principle calculate the coefficients $C_i(m)$ and $C'_i(m)$ for each layer i using the continuity and boundary conditions equations imposed in $z = 0$ and $z = z_n$. This provides the expression of the transformation of temperature $\Theta_i(n_x, n_y, z)$ or flow $\Phi_i(n_x, n_y, z)$ being determined in the plane where we want to calculate the solution, this expression can be further evolved by the following reverse transformation:

$$\theta_i(x, y, z) = \frac{4}{Ll} \sum_{n_x=0}^{\infty} \sum_{n_y=0}^{\infty} \Theta_i(n_x, n_y, z) \frac{\cos\left(n_x \frac{\pi}{L}\right)\cos\left(n_y \frac{\pi}{l}\right)}{\left(\delta_{n_x,0}+1\right)\left(\delta_{n_y,0}+1\right)}$$

In practice, the direct and inverse transforms will be discrete and carried out by numerical methods, which as *a priori* excludes the possibility of infinite wave numbers. A highest value must be retained for wave numbers depending on the maximum spatial resolution you want to deal with. For this limitation, one can directly apply Shannon's sampling theorem. For example, if we seek to obtain a spatial resolution equal to Δx and Δy following x and y respectively, the maximum wave numbers n_{xmax} and n_{ymax} should verify the following inequalities:

$$n_{\text{xmax}} \geq 2\text{L}/\Delta \text{ , } n_{\text{ymax}} \geq 2\text{l}/\Delta.$$

8.5.1.4. *Calculation of temperature or flow distribution in a block*

In practice, there is no particular need to look for direct expressions of coefficients $C_i(m)$ and $C_i'(m)$ in each layer i. And it may be noted that these factors can be eliminated by involving transformed distribution expressions of temperature and flow ((Θ_{iE}, Φ_{iE}) at the entrance to the layer i (at $z = z_{i-1}$) and (Θ_{iS}, Φ_{iS}) at the output of the layer (z = zi). You can then write the relationship matrix as follows:

$$\begin{pmatrix}\Theta_{iE}\\ \Phi_{iE}\end{pmatrix} = \left[\mathrm{A_i}(m)\right]\cdot\begin{pmatrix}\Theta_{iS}\\ \Phi_{iS}\end{pmatrix} \text{ with } \left[\mathrm{A_i}(m)\right] = \begin{bmatrix}\cosh(me_i) & \dfrac{\sinh(me_i)}{mk_i} + \dfrac{\cosh(me_i)}{g_i}\\ mk_i\sinh(me_i) & \dfrac{mk_i}{g_i}\sinh(me_i) + \cosh(me_i)\end{bmatrix}$$

where [$\mathbf{A_i}(m)$] is the chain matrix (according the theory of quadrupoles) representative of the layer i which gives distributions of temperature according to distributions at the output of layer i.

The major advantage of the introduction of formalism to the theory of quadrupoles at this level is to treat a block with any number of layers without difficulty. It should be noted that for a number of layers equal to n whose thickness and thermal conductivities are known, we can link the transformed entry distributions (Θ_S, Φ_S) to those of the exit (Θ_S, Φ_S), by a chain matrix [$\mathbf{A}(m)$] that we calculate directly, using the product of elementary chain matrices whose coefficients are calculated for each layer in the following order:

$$[\mathbf{A}(m)] = [\mathbf{A_1}(m)] \cdot [\mathbf{A_2}(m)] \cdot \ldots\ldots \cdot [\mathbf{A_n}(m)]$$

Such a procedure offers the advantage of guaranteeing a perfect numerical calculation, even if the calculation of the chain matrix of a complex structure, formed by a succession of many layers and for very large wave numbers is required.

For example, suppose we want to calculate the distribution of temperature at the surface of the block where the distribution of dissipated power is known, and where the distribution of temperature is imposed on the underside of the block. By applying the previous formalism of quadrupoles to the thermal problem, it becomes:

$$\begin{pmatrix} \Theta_E \\ \Phi_E \end{pmatrix} = [\mathbf{A}(m)] \cdot \begin{pmatrix} \Theta_S \\ \Phi_S \end{pmatrix} \Rightarrow \begin{cases} \Theta_E = \dfrac{1}{A_{22}(m)} \Theta_S + \dfrac{A_{12}(m)}{A_{22}(m)} \Phi_E \\ \Phi_S = \dfrac{1}{A_{22}(m)} \Phi_E - \dfrac{A_{21}(m)}{A_{22}(m)} \Theta_S \end{cases}$$

where [A(m)] is the chain matrix of the complete block and $A_{ij}(m)$ designate the coefficients of this chain matrix.

The procedure for practical calculation will be facilitated and will proceed as follows:

1) The transformations of θ_S and ϕ_E are made digitally by applying a Fast Fourier Transform algorithm, which allows us access to the m spectrum of these quantities.

2) The output we want to calculate is established using the adequate relationship of the m spectrum.

3) The inverse transformation of this new m spectrum is proceeded, and this provides the distribution of the sought after quantity.

Such a procedure allows for the quick calculation of temperature or flow map, even in cases where a high spatial resolution is required. For example it takes between 15 and 20 seconds to calculate a temperature or flow map of 128 by 128 points [DOR 97]. It should be noted that in many problems, the spatial resolution of the calculation in a block may be limited, thus accelerating the calculation procedure speed. We can of course, without any particular difficulty, complicate the calculation process to access the distributions of temperature or flow in a plan located anywhere in the block. In practice, it may be particularly interesting to calculate the distributions of temperature at the interfaces between layers so as to reveal the flow of heat on each layer.

8.5.1.5. *Extension of calculation to a complex assembly of blocks, s*

Regardless of the complexity of the defined block assembly, we can show that the procedure of calculation can be reduced to the implementation of a recurring basic procedure, which is to look for the flows at the interface between two superimposed blocks, as shown in Figure 8.17.

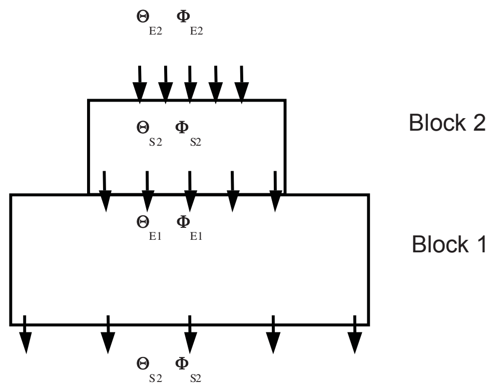


Figure 8.17. *Schematic view of a basic assembly of two blocks*

The search for the distribution of flows to the interface between blocks 1 and 2 is iterative and implements a relaxation algorithm for which a simplified chart is given in Figure 8.18.

As shown in Figure 8.18, we can see that the algorithm uses a weight coefficient set between 0 and 1 whose choice is crucial for two reasons:

– it is often necessary to obtain the convergence of iterative processes;

– it sets the speed of convergence of iteration.

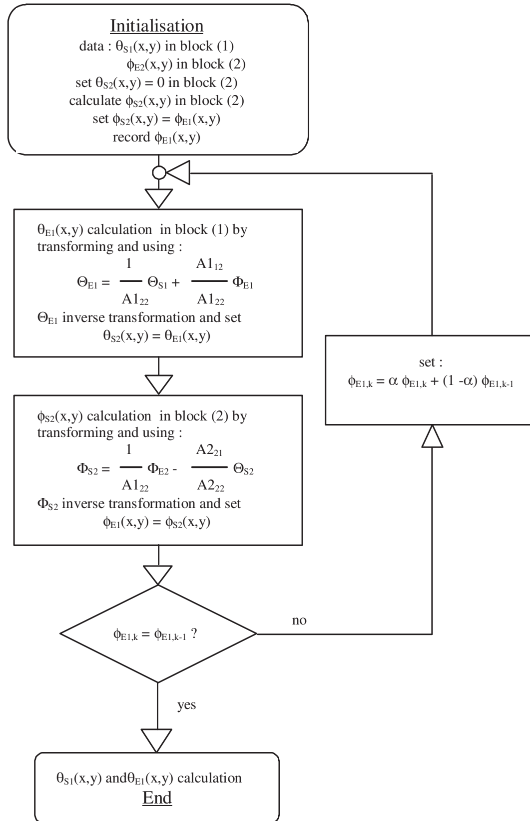


Figure 8.18. *Simplified iterative procedure for 2 blocks*

The practice of numerical calculation shows that there is no convergence problem during assembly, such as the upper block (2) has a lower conductance than the lower block (1), and in these conditions, the coefficient may be made equal to 1, leading to the fastest convergence. Now, when block (2) is a better heat conductor than block (1), the choice of a weight coefficient equal to 1 leads to a divergence in the calculation. The convergence can be restored if we reduce the weight coefficient ($\alpha < 1$); the choice of its value, however, reduces the convergence speed of the iterative process, often very a low factor, ensuring the convergence of computing after a very high number of iterations. To establish an optimum weight coefficient

value and ensure convergence of the iterative process within a minimum number of iterations, a more serious analysis of its dependence on the thermal properties of blocks 1 and 2 is required. By finely analyzing the iterative process between the two blocks, whose lateral dimensions are identical (to be able to apply the same transformation), we can show that transformed $\Phi_{E1,k}$ entering the block 1 during iteration number k is

$$\Phi_{E1,k}\alpha\left(\frac{1}{A2_{22}}\Phi_{E2}-\frac{A2_{21}}{A2_{22}A1_{22}}\Theta_{S1}\right)\left(1+q+q^{2}+...+q^{k}\right),\ q=\left[1-\alpha\left(1+\frac{A2_{21}A1_{12}}{A2_{22}A1_{22}}\right)\right]$$

where $A1_{ij}$ and $A2_{ij}$ designate chain matrix coefficients of blocks 1 and 2 respectively.

This expression shows that $\Phi_{E1,k}$ is the sum of the terms of a geometric progression, with reason q, which actually depends on the weight coefficient chosen and on the thermal properties of blocks 1 and 2, via the chain matrix coefficients on these blocks. The calculation process will converge if the module of q remains below 1, which leads to the inequality:

$$\alpha<\frac{2}{1+\dfrac{A2_{21}A1_{12}}{A2_{22}A1_{21}}}$$

The coefficients $A1_{ij}$ and $A2_{ij}$ of chain matrices depend on the spatial pulsation m. It is necessary to ensure that inequality is respected in the worst case i.e. for the maximum value of the spatial pulsation m (hence the biggest wave numbers corresponding to the transformation are made on the distributions of temperature and flow within these two blocks). In cases where the lateral dimensions of blocks are different, we can make a similar mathematical analysis, but the practical operation of the results of this analysis is too difficult to implement. It is better to choose a weight coefficient according to criterion α simply ensuring that in the upper block (2) the maximum spatial pulsation remains less or equal to the maximum value defined for the lower block (1).

The extension of the calculation procedure does not become a problem if you divide the complete structure of the model into sub-assemblies under the same level of interconnection. In referring to the case of the structure outlined in Figure 8.15b and going back from the base to the chips, we can successively define the following subassemblies:

– level 1: there is 1 subset formed by the base "E", which supports both insulating substrates, "SI" right and left;

– level 2: there are 2 subassemblies formed by the insulating substrate “SI” right and left that support heat dispatchers “RC” right and left, respectively;

– level 3: there are also two subassemblies formed by heat dispatchers “RC” right and left that support chips $IGBT_1$, $IGBT_2$, D_1 and D_2 and there are chips $IGBT_3$, $IGBT_4$, D_3 and D_4.

Such a decomposition may be made on any structure and each defined subset may be individually treated with the algorithm of the Figure 8.18. An identical algorithm can be implemented to find the flow into the base that supports all other blocks. We simply note that when a subset is characterized by a weight factor α less than 1, the convergence of calculation can be assured if we proceed for this subset with local iterations preserving the stability of the local calculation.

8.5.1.6. *Computer implementation and a calculation example*

In order to apply the calculation principles developed in the preceding sections, a computer program called LAASTHERM was developed. In its current version, this program can treat structures with a maximum of 100 blocks spread over 10 levels of interconnection. A set of 300 layers can be freely distributed among the 100 blocks and the power dissipation on each block can be accurately described through a set of 1,000 rectangular shape basic sources that can be arranged on the upper surface of this block. The LAASTHERM software also makes a pre-analysis of thermal properties for each of the blocks which have been defined and determines:

– for each block, the minimum spatial resolution required;

– for each level of interconnection, the weight coefficient α, which will be chosen for the stability of local iterative calculation.

Figure 8.19 gives a calculation example of the temperature and flow distributions, made by LAASTHERM for the structure described in Figure 8.15a (geometric structure and thermal data) and for the following distribution of power dissipation:

– $IGBT_1$, 140 W; D_1, 70 W; $IGBT_2$, 120 W; D_2, 60 W;

– $IGBT_3$, 100 W; D_3, 75 W; $IGBT_4$, 130 W; D_4, 80 W.

Figure 8.19a gives the general map of surface warm-up; such as an infrared camera would reveal in a view from above, whose case had been opened. Figures 8.19b and 8.19c show the heat flow distribution maps, leaving the dispatcher heat

“RC” and the insulating substrate “SI” of the right side of the module. Figure 8.19d shows the distribution of heat flux that leaves the underside of the base. The spatial resolution is 16 by 16 points for all blocks, except Block “RC” for which it is 16 by 32 points and the base “E” for which it is 32 by 32 points. The calculation time required to obtain all these results is less than a minute on a workstation.

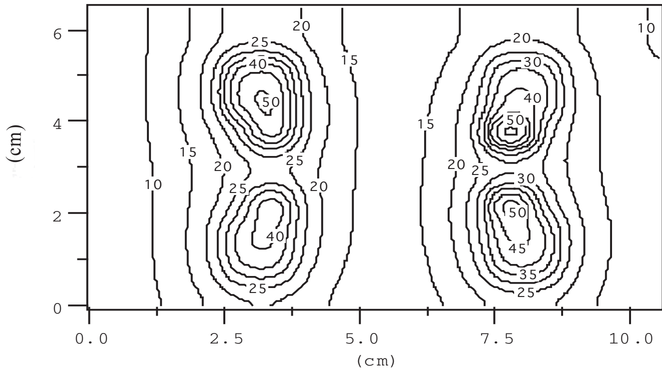
8.5.2. *The numerical models*

In this section, we will outline the two digital simulation softwares that we used. Other softwares are marketed, especially Ancys that many designers recommend.

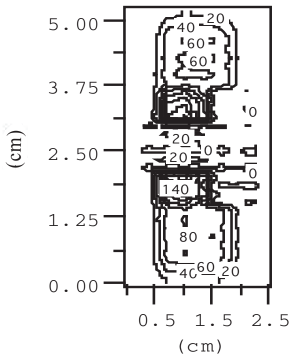
8.5.2.1. *Flux 3D*

8.5.2.1.1. Description

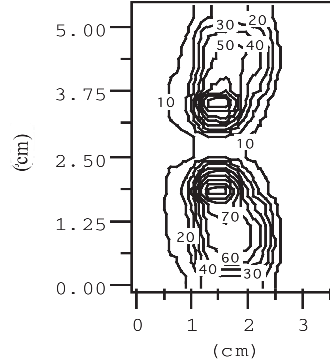
The Flux 3D software developed at Electrical Engineering Laboratory in Grenoble [SAB 86] allows us, through the module Fluxtherm, to solve the equation of heat in a system, in permanent system. The user must define the geometry of the problem, creating points and lines, surfaces and volumes. He must assign physical properties to these areas and volumes (for example, in our case, the thermal conductivity of silicon and water). Then comes the important step of meshing: this is a finite element software: each line of the geometry includes points more or less close together according to the desired accuracy of calculation. The software then creates a mesh whose elements are tetrahedrons. The last step is to implement the boundary conditions on the borders of the system. The convection is characterized by the heat exchange conditions along the walls where the convection takes place: the user must provide the value of coefficient h.



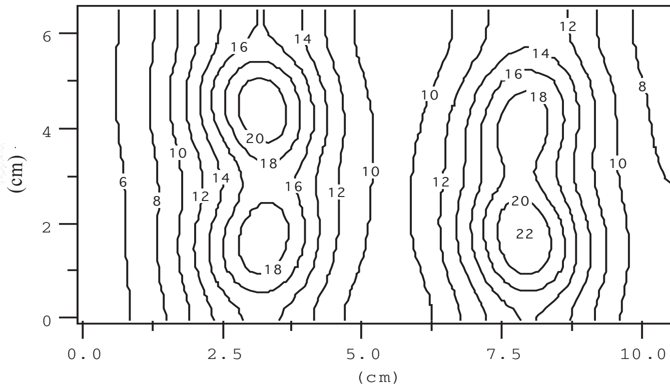
(a) Surface heating



(b)



(c)



(d)

Figure 8.19. *Calculated temperature and flow distributions*

The simulation gives, as the main result, the temperature at any point in the field under study: we deduce the average volume temperature of the junction, which in turn allows us to calculate the square thermal resistance of convection and diffusion:

$$R_{cconv} + R_{cdiff} = \frac{[\frac{1}{V}\iiint_{v} T(x,y,z).dV - T_a]}{\varphi}$$

8.5.2.1.2. Advantages

The Flux 3D software provides two major attributes for modeling thermal electrical devices, namely:

– This software promotes research into electro-thermal coupling (module Flux Chip) [RAE 97]. However, in this study, which deals mainly with design of micro-coolers, we will not take this opportunity and we will instead, consider the power dissipated as a given value.

– Typically, the default of finite element software leads to long computing times when the mesh is dense, as is the case if one wants to have a good consideration of interface phenomena. Indeed, they require the very thin mesh areas, leading to numerous elements and therefore equations to solve. In Flux 3D, the problem is greatly simplified by the potential introduction, of superficial elements with breaks to represent very thin areas (skirmishes, brazing). Their introduction provide precision areas with very different thicknesses.

8.5.2.1.3. Defects

Finite element softwares like Flux 3D essentially present three limitations:

– warm up and moving fluid are not taken into account: the fluid is considered as isothermic. The convection is therefore governed solely by the coefficient h, which is difficult to assess, and needs to be imposed by the user;

– the time of calculation, which nevertheless remains high (about ten minutes to several hours if we simulate the cooler in its entirety);

– the need for a new meshing when changing the geometry of the cooler, makes this method badly-suited to the design.

8.5.2.2. *Flotherm*

8.5.2.2.1. Description

The software was developed by the Flomeric Company to model the thermal and hydraulic aspects encountered in various applications ranging from the air conditioning for a room, to the cooler for power electronics. By solving the Navier Stockes equation, in addition to those of heat, we obtain the temperature at any point in the field, the speed and pressure of the fluid at any point. As with Flux 3D, the average temperature of the heating source is treated as a junction temperature and we get the total square resistance.

8.5.2.2.2. Advantages

The design of the Flotherm software provides, in our case, four advantages over the previous one:

– it allows for consideration of the fluid-wing convection: the h coefficient is not imposed by the user, but determined from the hydraulic and thermal equations;

– it takes into account the fluid mechanics: the problem can be solved in various situations, such as an established or not hydraulic system, a laminar or turbulent system;

– the software has libraries of materials, geometric shapes, and objects (fan, pump, etc.); and finally,

– other conditions such as heat radiation or natural convection can be treated.

8.5.2.2.3. Defects

Flotherm presents the following limitations:

– the parallel piped mesh does not permit the calculation of heat exchange on curved surfaces or ramps. It is therefore not possible, for example, to simulate coolers with trapezoidal or cylindrical channels;

– the software does not take into account the electro-thermal coupling;

– computing time is relatively short for simple applications, however, for the same reasons as those cited for Flux 3D, it remains too long to reach an optimization: the resolution time varies between one minute and ten hours

depending on the complexity of the problem (the calculation convergence difficulties arise mainly from the hydraulics).

8.5.2.3. *Simulation results*

We have now addressed the relevance of the two programs, namely knowledge of the junction temperature of a heating component according geometric and hydraulic parameters and a cooler.

Let us now examine what other results it is possible to obtain. As we said, Flux 3D solves the equation of heat along a wing. It is then possible to trace the isotherms in this wing, as seen in Figure 8.20. Given the different symmetries, and to gain calculation time, we simulate a part consisting of a channel and its two half-fins located on both sides.

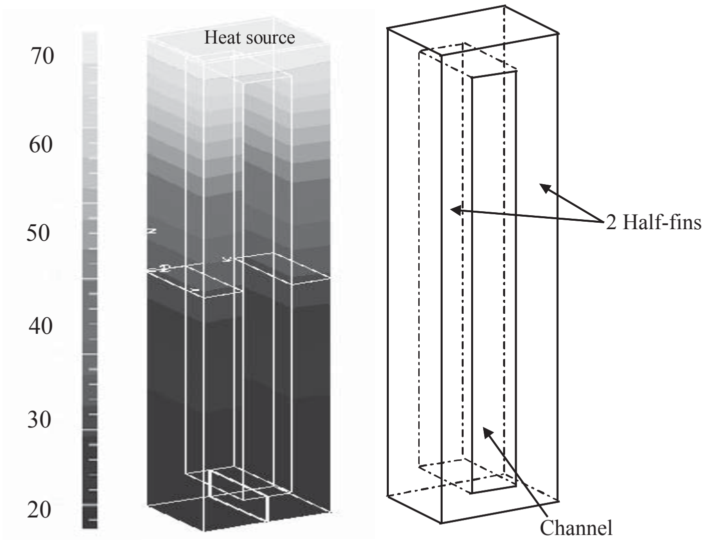


Figure 8.20. *Isotherms in two half-fins, data from Flux 3D: simulation of a channel and its two silicon half-fins*

In this figure, we see that the isotherms are all parallel to each other and perpendicular to the fins axis. The flow of heat is therefore unidirectional expressed by the vertical axis.

The Flotherm software also takes into account the fluid flow within the cooler. By simulating the entire structure, we gain access to the temperature map inside the

cooler (Figure 8.21), to the distribution of load losses (Figures 8.23 and 8.24) and to the velocity vector (Figure 8.22). Through these simulations, we have seen, for example: that the fluid is distributed uniformly in the channels when the holes are centred (which is the case of our coolers), see Figure 8.22 and 8.23; and a movement of fluid when the holes placed on the diagonal, which does not allow as good a distribution (Figure 8.24).

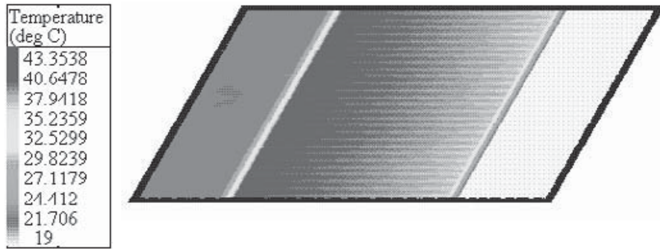


Figure 8.21. *Mapping the temperature of fluid in the cooler*

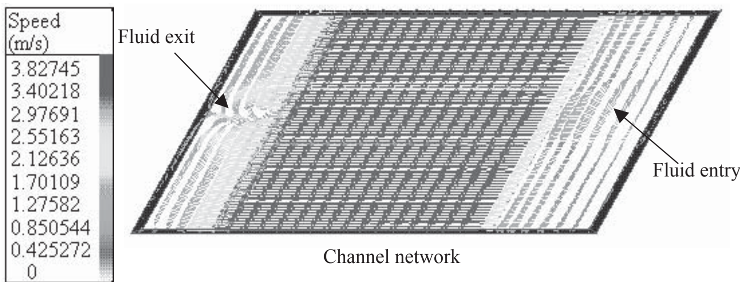


Figure 8.22. *Distribution of fluid velocity in the cooler*

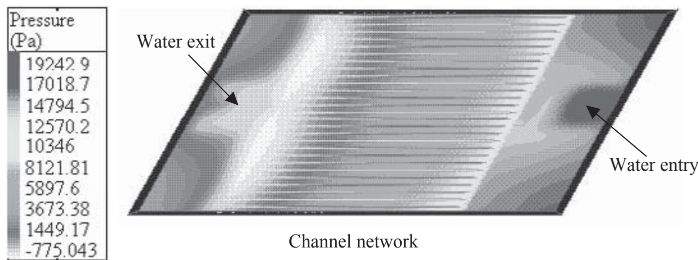


Figure 8.23 *Mapping the fluid pressure in the cooler whose holes are centred in relation to the collectors*

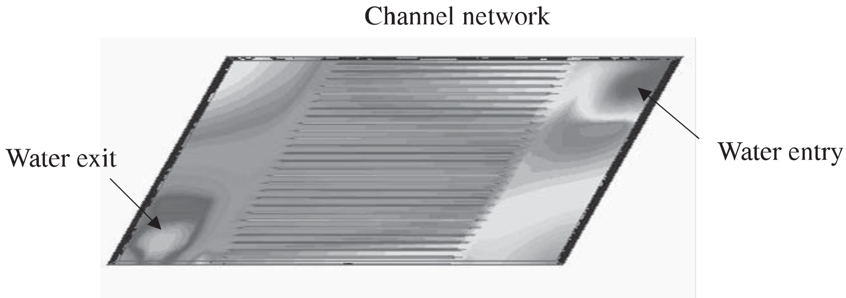


Figure 8.24. *Mapping the fluid pressure in the cooler whose holes are on a diagonal*

8.5.3. *Taking into account electro-thermal coupling*

In the power circuits for electrical energy conversion, power components act as switches with cycles from a state of high impedance (blocked-state), to a state of low-impedance (passing-state). If we analyze the power dissipation of such a component during a cycle of commutation, we can usually see that in the blocked-state the leakage current remains low enough to make the power dissipated by the component negligible. The component only accounts its power dissipation in the passing-state when its losses during commutation switching frequency becomes significant. As the electrical component characteristics, depend on temperature and as its commutation times are also influenced by temperature, there is interaction between the power dissipated in the component and its warm-up: this fact is called electro-thermal coupling. Figure 8.25 illustrates the concept of electrothermal coupling with a simplified functional diagram [BEL 97, HEF 93].

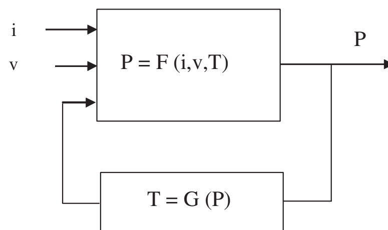


Figure 8.25. *Functional diagram representative of electro-thermal coupling*

Despite the apparent simplicity of the functional diagram in Figure 8.25, solving an electro-thermal coupling problem is not trivial. Indeed we must have software to

calculate the temperature (and/or its distribution) in electrically active areas of the component. We should also put into equations the power dissipation in active areas taking into account the fact that their temperature varies.

8.5.3.1. *Various possible approaches*

Given the level of sophistication expected in the modeling of the electro-thermal coupling, two types of approaches are possible.

8.5.3.1.1. Without taking into account the distributed power dissipation

This procedure is often used when we simulate the operation of a complex circuit with a circuit simulator or a behavioral simulator. In this case, we assume that the active area of the component is characterized by a single temperature. The thermal equations are introduced to assess the temperature of each active area and the electrical equations used to calculate the voltage and current through the active areas are dependent on temperature. This type of procedure is simple to use but it does not provide information on the intrinsic behavior of the component because it completely ignores the distributed nature of current lines in the active area of the component.

8.5.3.1.2. With consideration of distributed power dissipation

This procedure is more accurate because it takes into account that the current density is not uniform in the active area of a power component subject to heating. A distributed thermal simulation must be coupled with a procedure for calculating local power dissipation, taking into account distributions of voltage, current, and temperature in the active areas. Although the waveforms of voltage and current in the component are generally complex in converters, it is practically impossible to use a circuit simulator to calculate the local quantities i(t) and v(t) in the active areas. In order to achieve such a goal, the nature of the distributed component should considered; this requires the description of each elementary part of this component, by a complete electrical model. Given the practical difficulties that we encounter when we digitally simulate the operation of a circuit, with multiple components, whose electric models are usually non-linear; it is difficult to envisage this solution. Now, analytical simplified procedures may be developed for calculating the distribution of power dissipation based on reasonable assumptions. This procedure makes it possible to discover in greater detail, the electro-thermal behavior of a large component or group of components.

The electro-thermal modeling made in the context of section 8.5.3.1.1 is relatively common and one can find many examples in the literature. Electro-thermal modeling according the context of section 8.5.3.1.1 is rarer, however, and the following development will focus exclusively on this technique. With this

technique it is possible to determine whether the electro-thermal behavior of a large component, or of a power module is stable, and, if it would prove unstable, also whether there is an electro-thermal instability, locally or globally.

8.5.3.2. *Determining the power equation*

To simplify and maintain the brevity of the statement, it is limited to a static evaluation of the effect of electric and thermal coupling on large components or components mounted in parallel to achieve power modules. We assume further that the power dissipation in components is mainly due to losses resulting, during the passing-state, of a global current in components imposed by the external circuit.

For almost all the components used in the converters circuits, the calculation of power dissipation in the passing-state can be done without too much error by the approximation of a dropout linear voltage according to the passing current. If this component is isothermal, its direct voltage drop V_{on} can be written:

$$\begin{cases} V_{on} = V_S + R_{on} I_{on} & \forall \quad I_{on} \geq 0 \\ \quad I_{on} = 0 & \forall \quad V_{on} \leq V_S \end{cases}$$

where I_{on} means the passing current imposed by the external circuit, V_S is a threshold voltage and R_{on} is a series resistance. These last two terms depend on the operating temperature of the component. The second condition is applied to prohibit any possibility of reversing the current I_{on} when the voltage V_{on} becomes less than the value of the V_S threshold voltage.

In practice, the expression above, describing a component approaching a direct voltage drop is all the more valuable when the component is subject to a passing current of strong intensity. The resistance R_{on} of controllable components (MOS and IGBT transistors) can be determined by the value of the voltage command applied to the command electrode of the component (e.g. grid-source voltage for a VDMOS transistor).

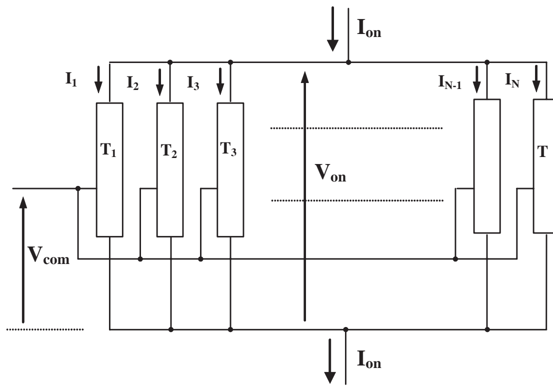


Figure 8.26. *Schematic spread of the active zone of a non-isotherm component*

When the component is no longer an isotherm, we should represent its active area as shown in Figure 8.26. The active zone should be treated as a parallel assembly of basic components, operating so that the direct voltage drop, V_{on}, is common, and sharing common current I_{on}, depending on the local temperature. Assuming that the common current I_{on} is imposed by the external circuit and that the distribution of temperatures in the active area is known, we can calculate the current I_i and common voltage drop V_{on} in solving the system of equations:

$$\begin{cases} I_i = \dfrac{S_i}{S} \dfrac{V_{on} - V_S(T_i)}{R_{on}(T_i)} & \forall 1 \leq i \leq N \\ \displaystyle\sum_{i=1}^{N} I_i = I_{on} & \end{cases}$$

where S refers to the total surface of the active area and S_i to the surface of element i at temperature T_i of the active area [VAL 97]. This system of equations implicitly assumes that each element of the active area is still characterized by the law $V_{on}(I_{on}, T)$, which was defined for isotherm components.

To better meet the physical reality, we must prevent the emergence of negative currents I_i, when solving the system of equations. Under these conditions, numerical resolution can no longer be calculated analytically, but should be done only by looking for iterative values of V_{on}, which can verify that the sum of all currents I_i is equal to the current I_{on} imposed on the component by the outside circuit. When

appropriate allocation of the current I_i is obtained, we can simply calculate the distribution of dissipated power in the active area with the relationship:

$$P_i = \left[V_S(T_i) + \frac{S}{S_i} R_{on}(T_i) \right] \cdot I_i$$

Knowledge of the distribution of power can then revive the calculation of temperature distributions, and complete electro-thermal calculation can be achieved by implementing a numerical algorithm whose simplified process is given in Figure 8.27.

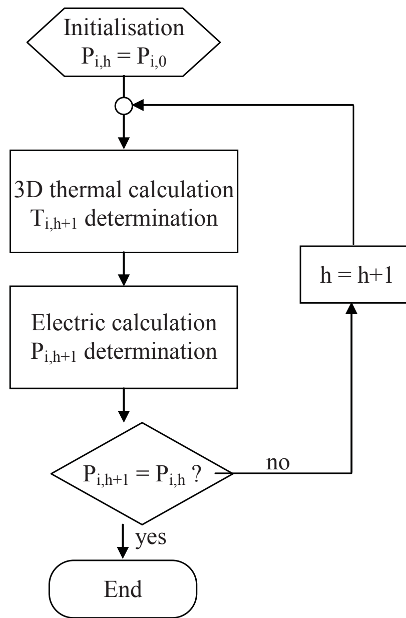


Figure 8.27. *Simplified electro-thermal calculation process*

8.5.3.3. *Examples of electro-thermal simulation*

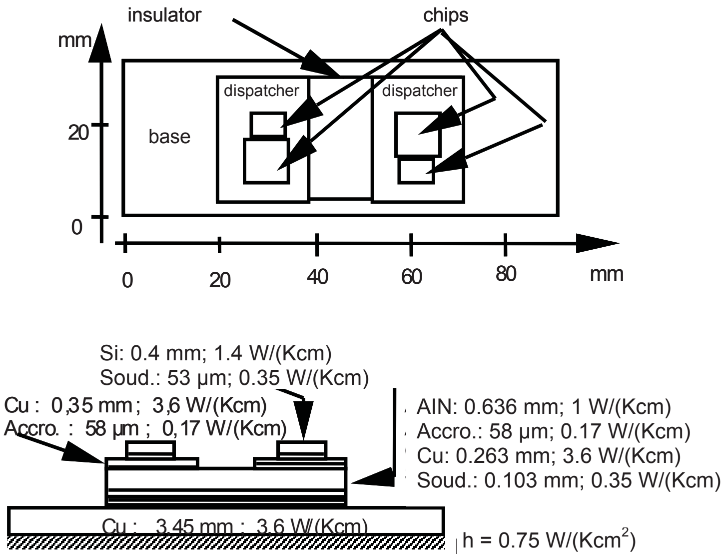
8.5.3.3.1. IGBT module

Figures 8.28a to 8.28c give examples of a simplified electro-thermal calculation conducted on a chip module IGBT MG75J2YS40, whose data on the geometric layout and thermal structure are recalled in Figure 8.28a. For purposes of electro-thermal calculation, the active area of an IGBT has been divided into 64 by 64

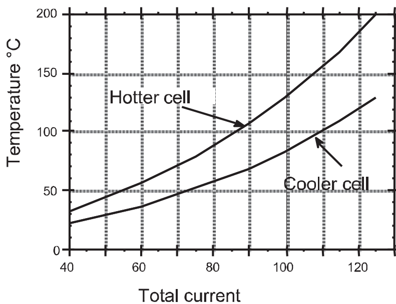
thermal cells. The direct voltage drop during the passing-state of the IGBT can be calculated from the threshold voltage, V_S, of the on-state resistance, r, whose values in relation to the temperature are:

$$V_S(T) = 1.7213 - 1.644\ 10^{-3}\ T - 1.229\ 10^{-5}\ T^2$$

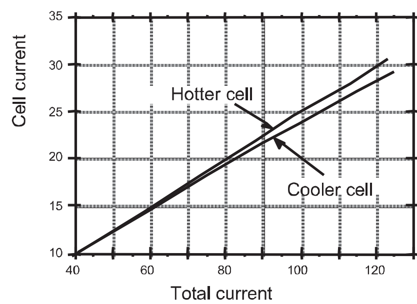
$$r(T) = 1.198\ 10^{-2} + 8.74\ 10^{-5}\ T$$



(a) Geometric behavior and thermal structure



(b) Temperatures calculated on the chip



(c) Current calculated in the cells

Figure 8.28. *Example of an electro-thermal simulation module IGBT MG75J2YS40*

Figure 8.28b shows the calculated evolution of the highest and lowest temperatures of the active area, depending on the external current imposed on the chip, while Figure 8.28c gives an indication of the distribution of this current in the different thermal cells which have been defined. It should be noted that in this case the local electro-thermal behavior of IGBT is stable, which makes in practice a very low dispersion between the minimum local current established in the hottest cells and the maximum local current established in the coldest cells.

8.5.3.3.2. MOS transistor module

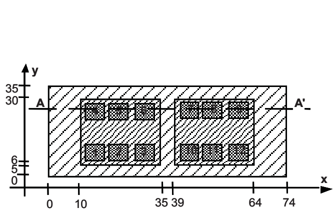
The following example focuses on the electro-thermal study of a hybrid module including MOS transistor reference MTM 8N60 mechanically mounted as shown in Figure 8.29a and assembled as a bypass, six by six, for the electrical operation. Figure 8.29b recalls data on the thermal structure of the module, and the direct voltage drop during the passing-state for a thermal cell of index, i, and temperature, T_i, of a MOS transistor is calculated from its resistance, r_{oni}, during the passing-state. This is given by the relation:

$$r_{oni}(T_i) = 0.432\ N\ (1 + 2.864\ 10^{-3}\ T_i + 1.371\ 10^{-5}\ T_i^2)$$

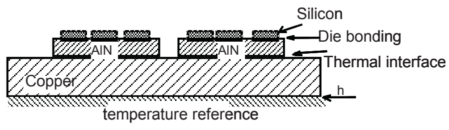
It is assumed for this study that only chips 1 to 6 are active and share a common current imposed by the external circuit.

Figure 8.29c shows the calculated evolution and the maximum temperature reached by chips no. 1 and 2 according to the total current imposed by the external circuit. Note first the good homogeneity of maximum temperatures which are very similar when the external current increases, thereby demonstrating that the power dissipated by each of MOS transistors remains well balanced and that the electro-thermal local stability of the MOS transistors module is very good.

Figure 8.29d shows a comparison of the maximum temperature evolution that can be achieved depending on the current; considering on the one hand a R_{on} independent of temperature, and on the other hand the full effects of the electrical and thermal interaction. We can see that taking into account the full electro-thermal interaction leads to a significantly lower current value at the limit of overall thermal stability. The latter is crossed when the power dissipation is no longer compatible with the power, which can be evacuated by the cooling device.

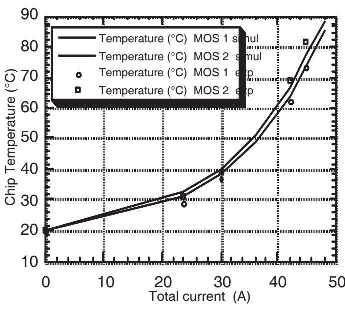


a) geometrical layout of the different blocks (all sizes expressed in mm)

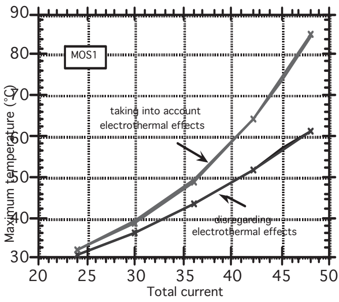


Copper width = 2.5 mm ; k = 3.6W/(cm.K); D = 1.03 cm2/s
AlN width = 0.7 mm ; k = 1.1W/(cm.K); D = 0.48 cm2/s
Die bonding = 0.08 mm ; k = 0.35W/(cm.K); D = 0.27 cm2/s
Silicon width = 0.3 mm ; k = 1.6W/(cm.K); D = 0.93 cm2/s
Convective exchange coefficient h = 0.5 W/(cm2.K)
Thermal interface: Rth = 0.06 cm2.K/W

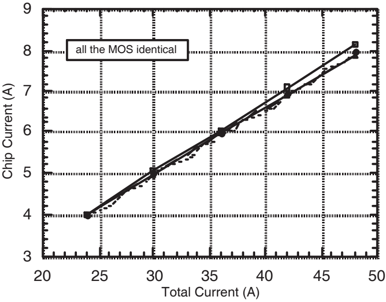
b) thermal structure along the line AA'



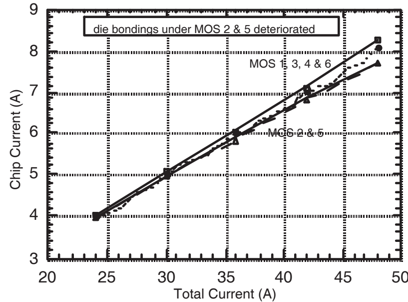
(c) Evaluation of temperatures



(d) Comparison of heat-up calculated with or without electro-thermal coupling



(e) Sharing of currents between the chips



(f) Influence of an imbalance between thermal resistances

Figure 8.29. *Example of electro-thermal simulation of a MOS transistor module*

Figure 8.29e shows the evolution of currents conducted by the various chips according to the total current imposed on the module. It should be noted that these currents are very similar for different chips, even when approaching the thermal limit imposed by the stability of cooling. By way of comparison, Figure 8.29f shows the impact of a degraded thermal contact under chips 2 and 5: it is assumed that the thermal resistance of the weld of chips 2 and 5 is increased by a ratio of one to three compared to welds of other chips. While this situation leads to a significant overheating of chips 2 and 5, the current conducted by these chips only decreases slightly. We can therefore say that in practice, if we observe, in a MOS transistor module whose chips are mounted in parallel, strong maximum inequalities of temperatures between chips, this disparity in temperatures is caused by the imperfections in the thermal environment near chips.

8.6. Experimental validation and results

In this section, we will present the experimental results obtained from two test benches. The first operates a direct measurement of temperature and the second an indirect method. Both methods are commonly used.

8.6.1. *Infrared thermography*

8.6.1.1. *Overview*

General principles of radiation physics teach us that, the surface of a body brought to an absolute temperature, T, radiates a power density p (expressed in $W{\cdot}m^{-2}$) into the surrounding space proportional to the fourth power of its temperature (Stefan-Boltzmann law). The radiated wavelengths and their relative intensity depend on the temperature provided by Planck's law. Conversely, we can use the radiated power, detected in an appropriate wavelength range to determine, under certain specified conditions, the temperature of the body under observation: this is the principle of infrared thermography which operates with electromagnetic radiation commonly in the wavelength range of 2 to 10 μm. There is no attempt here to rebrief on theoretical infrared thermography, which may be found in the above cited works, we simply to show how it is possible to operate in practice to measure the temperature of the active parts of hybrid integrated circuits when they are operating. Currently, infrared thermography is practiced with an infrared camera connected to an electronic monitor, whose role is to interpret the radiometric image directly in the form of a map of temperature, provided that the local emissivity of the surface on which the radiation is studied is known.

8.6.1.2. *Precautions*

It should be noted first that measuring the operating temperature of a component by infrared thermography requires direct observation of its surface and therefore requires the investigator to work on components whose environment has been altered to make this observation possible. In particular, the junction temperature of an encapsulated component cannot be accessed by thermography. At least the case must be opened and all the protective layers removed to give direct access to the optical surface to be observed.

Then take into account the fact that the surface to observe has multiple areas of a different nature (the semiconductor oxide or passivant, metal), characterized by very different emissivities that make it difficult to directly interpret the radiometric image under the form of a thermal map. In general, we get good results only if the surface emissivity is homogeneous. For this, the easiest method is to paint the surface with a thin layer (10 to 15 µm) of black paint to ensure a uniform emissivity value close to unity (≥ 0.95) with the wavelength range operated by the IR detector of the camera.

When dealing with the surface in order to standardize its emissivity, we should be vigilant of the paint deposit thickness. Figure 8.30 shows the problem of determining a constant temperature, T, from the temperature, T_M, measured by the infrared camera on the surface of the deposit of paint of thickness e, conductivity, k, and assuming that the heat was evacuated by convection (characterized by the coefficient h) from the surface of the deposit of paint. Under these conditions, we can easily show that the quantities

ΔT_M ($= T_M - T_A$) and ΔT ($= T - T_A$) are linked by the relationship:

$$\Delta T = \left(1 + \frac{he}{k}\right)\Delta T_M$$

This relationship clearly shows that the difference in measured temperature ΔT_M drops representative to the real temperature difference ΔT, as soon as the ratio he/k remains low compared to the unit. We conclude immediately that if the measured temperature must remain representative of the temperature sought, the filing of paint which is generally characterized by a low thermal conductivity (≤ 0.01 $W \cdot K^{-1} \cdot cm^{-1}$) must be much finer if it is to be associated with the large convective exchange ratio observed at the surface.

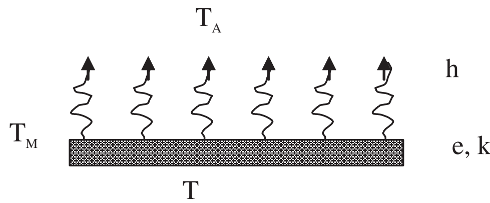


Figure 8.30. *Classic problem of measurement by infrared thermography*

The general purpose infrared cameras are made to provide the radiometric images at a rate of 30 to 100 images per second. In these circumstances, it is as if the thermal scene was observed sampled at a frequency of 30 to 100 Hz. Applying the classic rules (Shannon's theorem) on sampling, we should restrict this technique to observe static or at least slow phenomena, characterized by relatively long time constants (≥ 0.1 s). We may therefore observe the slow transitional heating resulting from the gradual heating of the housing, characterized by constant timespans of several seconds or even minutes. The rapid heating on chips in cases of accidental electrical overload, are often thermal transients characterized by time constants ranging from a few µs to the ms.

8.6.1.3. *Example of thermo-graphic survey*

Figure 8.31 shows a thermography record done on a power IGBT module (MG 200 JYS1 from Toshiba). For the purposes of experimentation, the module was mounted on a water cooler which helps maintain its underside in contact with water at a constant temperature. The upper part of the case has been removed, as well as the freezing filling, contributing to the electrical passivation of the components and their protection against corrosion. The surface of the module was covered with a black paint to make its emissivity uniform. A preliminary calibration was done by heating the module; by circulating a water at regulated temperature to verify that the emissivity of the surface is actually homogenous, and close to 0.9. This actually helps to interpret the radiometric image as a map of temperatures. For this experience, chips 1 (top) and 2 (bottom) are mounted in parallel and share a total current of 90 A under a common voltage drop equal to 2.94 V. The total power dissipated by the module is 265 W and is divided into 140 W for chip 1 and 125 W for chip 2, which explains why chip 1 seemed hotter according to the thermography.

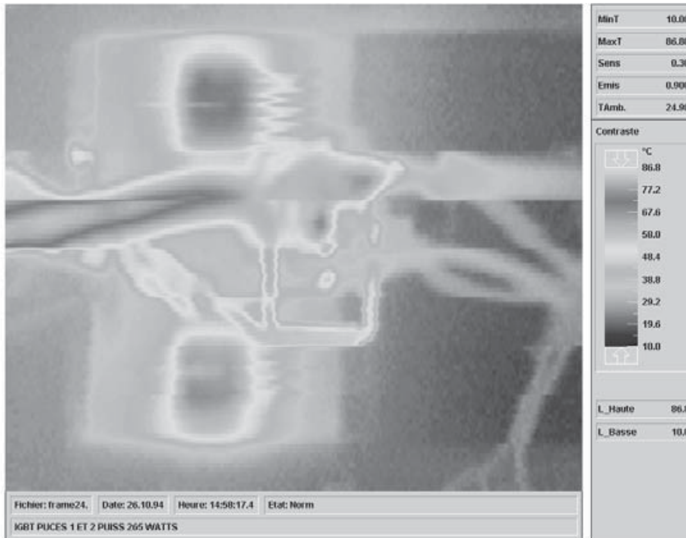


Figure 8.31. *Example of thermography statement for an IGBT power module*

The thermography also shows that the power dissipation is far from negligible in the connection wires that bring the current to the IGBT chips collectors. The distortions of the observed temperature distribution in the active areas of the IGBT chips are due to the local connection wires. A more detailed study and comparison calculated temperature distributions and those measured by infrared thermography determined with certainty that the cooling module is characterized by a convective coefficient exchange whose value is not constant but varies, depending on the position at the base of the module.

8.6.1.4. *Conclusions*

Due to the constraints applied to the sample under test, it is clear that the infrared thermography is not an appropriate technique for junction temperature measurement, for components operating in normal conditions. However, the fact that it is able to provide with good definition (an image is commonly made up of 100 lines with 256 pixels, and is even better for the most recent devices) information on the distribution of the surface temperature of the studied components, this technique can be an excellent tool for validation of thermal modeling results.

8.6.2. *Indirect measurement of temperature from a thermo-sensible parameter*

8.6.2.1. *Description of the measurement bench*

We present in this chapter measurements taken on an IGBT equipped with a cooler made of micro-channels flowed by the circulation of water.

The measurement bench, presented in Figure 8.32 consists of a hydraulic open-loop, a heating source and different systems for measuring temperature.

The hydraulic system itself is composed of a debimeter, a 10 µm filter limiting the risk of channel obstruction and a digital gauge measuring the loss of water pressure between the input and output of the cooler at collector limits, with an uncertainty of 10 mBar.

To characterize a cooler, we should apply a constant power P to its upper side – this is the role of the heating source – and have access to three temperatures: that of water at the input of cooler T_e, that of water at the output T_s and that of the upper surface of the cooler, which we called junction temperature T_j.

From these different measures, we deduct the thermal square resistance by the equation:

$$R_{cmestot} = \frac{T_j - T_e}{\varphi} \text{, where } \varphi \text{ is the heat flow}$$

The water temperatures at the entrance and exit are measured through thermocouples inserted in the hydraulic pipes, and linked to an acquisition system using the Madena software. The uncertainty on the measures is around ± 0.5°C.

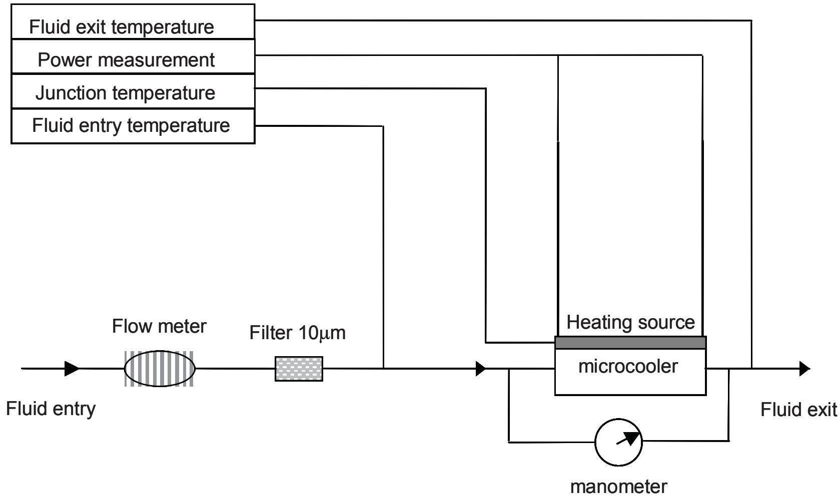


Figure 8.32. *Schematic of the measurement bench*

In the case of copper coolers, an IGBT without case is directly soldered onto the upper side of the cooler, which also plays the role of connector with the drain. The measures of current and voltage give the power value ($P = \varphi \cdot S_P = U \cdot I$). The temperature at the junction of IGBT in this case is equal to the temperature of the upper surface of the cooler, since the thermal resistance of the solder can be considered negligible (less than 1% of the total resistance) [LAF 96]. The measure of this junction temperature is made indirectly by measuring an easily accessible magnitude, called the thermo-sensitive parameter (TSP), whose value varies with temperature following a known law. The TSP usually chosen is the voltage drop when the device is flowed by a low measurement current I_e (10 mA) [GRA 85]. The circuit in Figure 8.33a allows us to make flow a current of the form given in Figure 8.33b. The current I_{ch} issued by the pilot switch, ensures the heating of the IGBT. The time of application must be sufficient to achieve a permanent heat operation (around 100 ms) [MEY 98]. For the measurements, this current is blocked by the pilot switch. The component under test, is then flowed by a calibration current supplied by an auxillary source. V_{sat} is measured on its terminals. The measurement time is about 100 µs.

The law V_{sat} (T_j) is linear and increasing with a slope close to 2 mV/K. This method has mainly been used for copper cooler characterization experiments. Some previous work has shown that this temperature is near the volume average temperature of the chip in steady state operation [FAR 94]. This is the definition that we gave to the junction temperature:

$$T_j = \frac{1}{V_p} \iiint_{V_p} T(x,y,z)\,dV_p$$

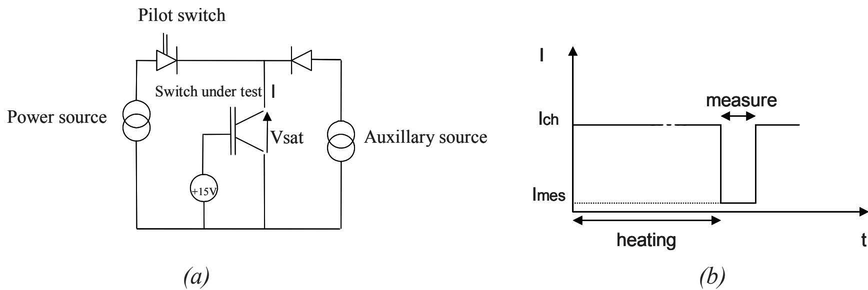


Figure 8.33. *a) Mounting allowing the measurement of the TSP of the test component, b) waveform of the current flowing through the device under test*

8.6.2.2. *Results of measurements*

The following results were obtained on copper coolers prototypes made by Luc Meysenc during his thesis [MEY 98]. Table 8.2 gives their main characteristics.

	channel depth D (μm)	**channel width** lc (μm)	**fin width** e (μm)	**thickness spreader** e_d (μm)	**channel no.** n	**size of red channels** $L_x = L_y$	**section**
Prototype Cu 1	3,040	311	288	1,800	27	1.6x1.6 cm²	rectangle
Prototype Cu 2	730	230	165	1,800	41	1.6x1.6 cm²	rectangle

Table 8.2. *Key geometrical parameters for two copper prototypes made by LEG*

Here, the thermo-sensitive parameter method measurement introduced in the first section was used.

In the best case, it is possible to dissipate, through these copper coolers, a power density of 300 W·cm^{-2} for a junction temperature rise of 60°C. Note that this cooler does not include electrical insulation between the chip and the fluid.

	Q (l·min^{-1})	**φ (W·cm^{-2})**	**R_{cmes} (K·cm^2·W^{-1})**
Proto Cu 1	0.63	156	0.27
	1.33	156	0.24
	1.75	156	0.23
	2	156	0.22
	3.5	156	0.2
Proto Cu 2	0.5	156	0.31
	0.7	156	0.26
	1	156	0.23
	1.3	156	0.22

Table 8.3. *Results of measurements on copper micro-coolers (Q is flow of water)*

8.7. Conclusion

Throughout this chapter, we examined the various aspects involved in cooling power electronic components. We recalled the basic rules for evaluating the losses. We have presented different heat exchanges involved in this type of devices. A substantial portion of the chapter was devoted to thermal modeling of modules on a few examples of software tested during national research operations. It is obvious that this presentation is not exhaustive and that there are other tools that can lead to comparable results.

These modeling approaches, especially those made from analytical equations (which are much faster) are required to design coolers well suited for this type of application.

Finally, we presented some measurement methods and experimental results that validate simulations with acceptable accuracy for this type of problem.

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