Power Electronics Semiconductor Devices
Edited by Robert Perret

Chapter 7

Commutation Cell

7.1. Introduction: a well-defined commutation cell

The concept of a commutation cell developed by H. Foch made it possible to describe in a rational manner the operation of the structures of power electronics. It is a powerful analytical approach, which allows us to determine the key players during a comutation. Initially applied only to the study of the overall operation of converters, this approach may also find application in the study of the finer phenomena of switching, if the whole environment of semi-conductors is well represented.

An example to illustrate these words: consider a three-phase voltage inverter produced on printed circuit board (Figure 7.1a). According to the modes of command, a switch will always commutate on an another one under the voltage of the power bus, the load operating as an instantaneous source of current. As a result, the basic commutation cell will always be of the same type on a structural level, the famous "chopper" cell or "inverter" cell according to the terminology (Figure 7.1b). Suppose now that we are interested in the phenomena of commutation or electromagnetic compatibility problems. It is no longer possible to ignore the influence of tracks, decoupling capacitors, packaging of semi-conductors and common mode capacitors. Figure 7.1c then shows a commutation that differs completely from another, since they are not the same elements (semi-conductors, tracks, common mode capacities, etc.), which are important.

Chapter written by James ROUDET and Jean-Luc SCHANEN.

The "switching cell" analysis tool must therefore take into account all the modeling from the beginning.

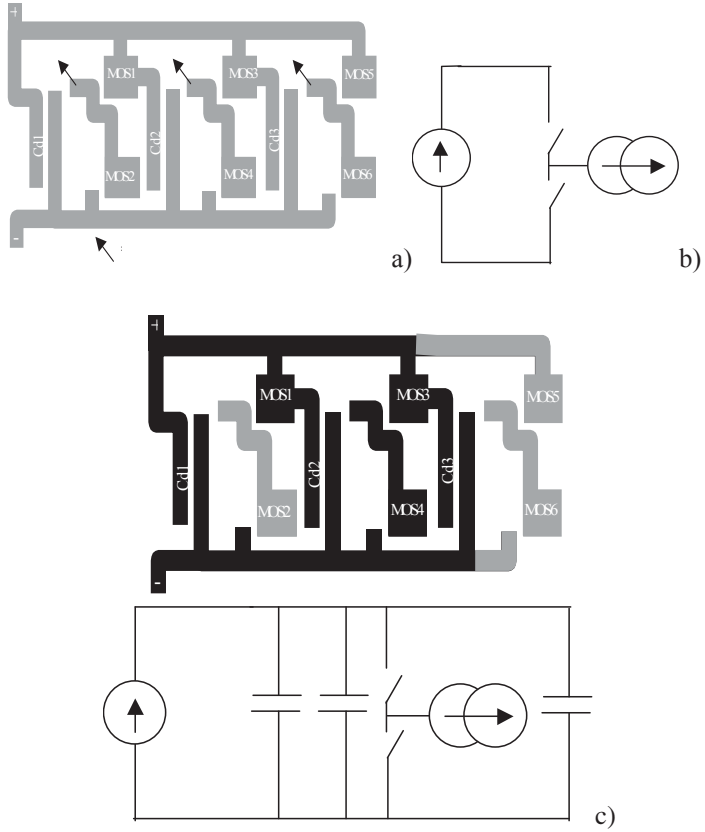


Figure 7.1. *Commutation cells for a three-phase inverter [TEU 97]:*
a) complete converter (with 3 decoupling capacitors);
b) structural commutation cell: identical for any commutation in this structure;
c) "technological" commutation cell during the commutation from MOS 3 to MOS 4

7.2. Some more or less coupled physical phenomena

The study which is conducted in this section is intended to define what must be represented, in a commutation cell, so as to be solved simultaneously. Indeed, the various physical aspects are not of the same degree of coupling, and it is not necessary to take into account everything at the same time; some problems can be resolved in a sequential manner.

Traditionally, we define strong couplings, which would require a concurrent resolution, and weak or unidirectional couplings authorizing a sequential approach. The fields of physics involved in the simulation of a static converter are:

– electromagnetics for any semiconductors and wiring aspects (power, control, conducted and radiated EMC);

– thermal and hydraulic physics (heat sink design);

– thermo-mechanics (differential dilatations, causes of breakage, etc.);

– thermoelectrics (on the one hand, physical parameters of semiconductors and wiring and, on the other, calculation of losses);

– electromechanics (tearing of bus bars in case of a short circuit, forces on supports);

– electrostatics – even electrodynamics – (partial discharges, dielectric breakdowns).

Some aspects can be clearly ranked among the weak couplings; it is evident that mechanical deformation in the wiring of power electronics will have extremely low influence – in normal operation – on the electrical wiring! Similarly, thermo-mechanical aspects can be handled independently of the electrical behavior of devices. The study of dielectrics may also be classified in the category of unidirectional couplings.

That leaves more sensitive aspects which concern the electromagnetic and thermal phenomena. For the pure calculation of a heat sink, hydraulic and thermal considerations, independent from a power electronics circuit, need to be carried out. But to determine the quantities of heat to remove, it is necessary to know semiconductor losses, and therefore the results of a temporal simulation. However, the electrical behavior of switches (and to a lesser extent wiring resistance) depends on their temperature. This is a bidirectional relationship. However, in a vast majority of cases, the efficiency of cooling and thermal constant times are such than an indication of the average operating temperature is sufficient. It therefore seems quite reasonable to predict the thermal state of the system to carry out a complete simulation, and to verify afterwards that – given the calculated losses – the forecast was right. This procedure must converge relatively quickly (2 or 3 iterations) and is much simpler than a complete electro-thermal resolution which is not really justified.

The different fields of physics have been limited to a mere (!) electromagnetic study, but there is still an analysis of various electrical phenomena in a converter. These can be cataloged under “power”, “command”, “conducted EMC” and “radiated EMC”.

It has been shown [YOU 98] that radiation aspects can be deduced from the knowledge of currents in conductors. In addition, the influence of radiated fields by the power signals on the electrical characteristics is negligible at the frequencies considered: the equivalent resistance of radiation at 100 MHz for conventional printed circuit systems does not exceed a few mΩ, which has no significant influence on waveforms.

$$R = 20 \cdot \beta^4 \cdot L1^2 \cdot L2^2$$

with β = wave number = ω/v. For L1 = L2 = 5 cm (radiation loop considered), R = 2.4 mΩ in vacuum (v = c) at 100 MHz.

The "conducted EMC" aspect is a little trickier: it seems fairly clear that the power waveforms depend very little on conducted emissions in most cases, but a few exceptions must be reported. The common mode current, led by strong voltage changes within the structure, flows through the power circuit and is therefore added to the switch current (Figure 7.2). While it is important, the change is significant and may even in some cases lead to malfunction of the mounting [LAP 98].

Without examining cases that are so bad, we are entitled to wonder if the phenomena are decoupled. [TEU 97] showed that in relatively realistic cases, waveforms are actually very dependant on the "EMC" environment to be added to the "power" commutation cell: dV/dt is not affected by the common mode capacities of the power circuit. This is not necessarily the case for the common mode capacity of a drive circuit (direct disruption of the board).

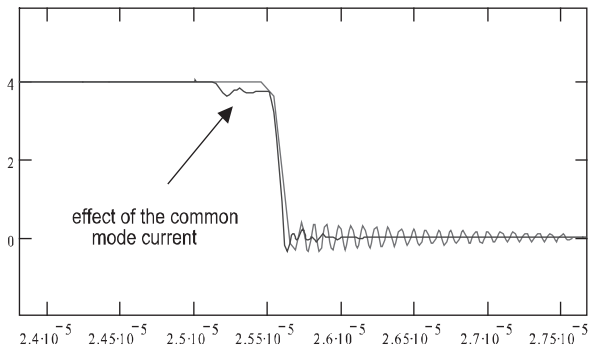


Figure 7.2. *Common mode current in a chopper cell changing the power current. Simulation of power circuit alone and adding a common mode capacitance of 1 nF (deliberately exaggerated value)*

In this case of unidirectional coupling, in a first approach, simulations of a power circuit may be performed, and then these waveforms may be injected in an "EMC" environment to obtain conducted disturbances. Figure 7.3 shows an example of low-coupling "power-EMC".

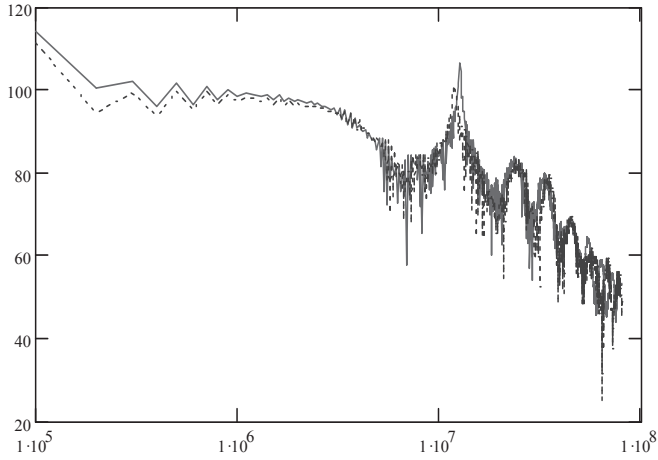
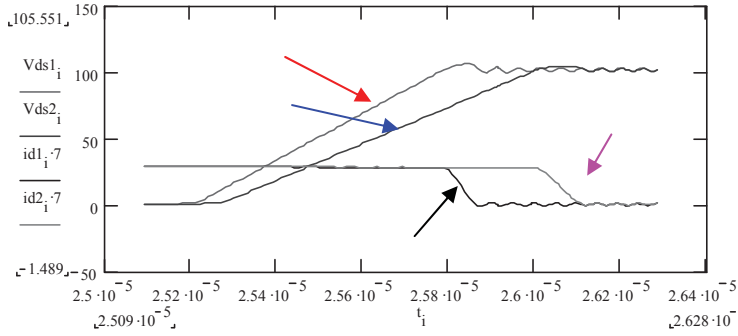


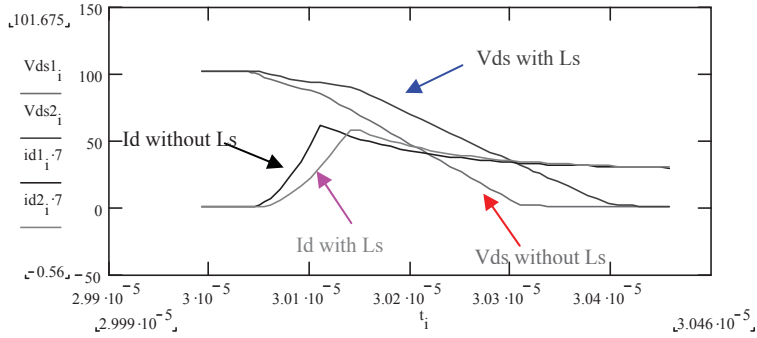
Figure 7.3. *Example of conducted disturbance (voltage on supply terminals on a Line Impedance Stabilizer Network)*

If, however, this assumption were too simplistic, taking into account the environment of the system in order to take account of this "EMC" aspect would be required. It is not too complicated insofar as this is only classic R, L, M, C circuit elements, and not heavy finite element calculations.

As far as other phenomena must be taken into account, the decoupling is no longer possible: these are interactions between semiconductors and wiring. Two examples may illustrate this assertion: the calculation of the voltage surge at the opening of a power switch, and interaction power-command phenomena by common impedance.



a) opening



b) closing

Figure 7.4. *Interaction power-command for an isolated grid component: the term Ls.di/dt reacts on the grid circuit, changing the commutation behavior. It must therefore be considered during the simulation. Simulation conditions: Rg = 50Ω, total mesh inductance 70nH: comparison between Ls = 0 and Ls = 20 nH (+ 50 nH on the mesh in this case)*

Concerning the voltage surge at the opening due to inductance of the switching mesh, Figure 7.5 clearly shows that decoupling is not possible in the case of fast commutations: indeed, the di/dt depends on the mesh inductance, and a simulation that does not take it into account is no longer realistic. Note however that for commutations where the component is greatly slowed down (strong grid resistance), the decoupling can be justified (Figure 7.14).

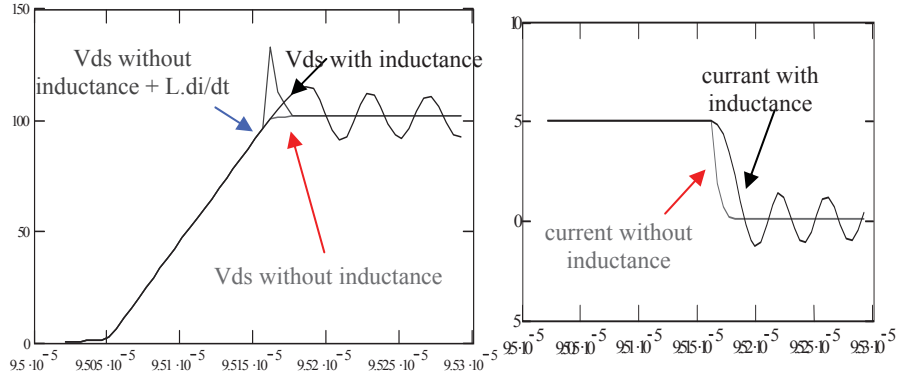


Figure 7.5. *In the case of a fast commutation, it is not possible to calculate the voltage surge at the opening L.di/dt without taking into account the inductor L in the simulation (we note that currents have different slopes) (simulation on PSPICE, MOS IRF.150, Rg = 10 Ω, L = 50 nH)*

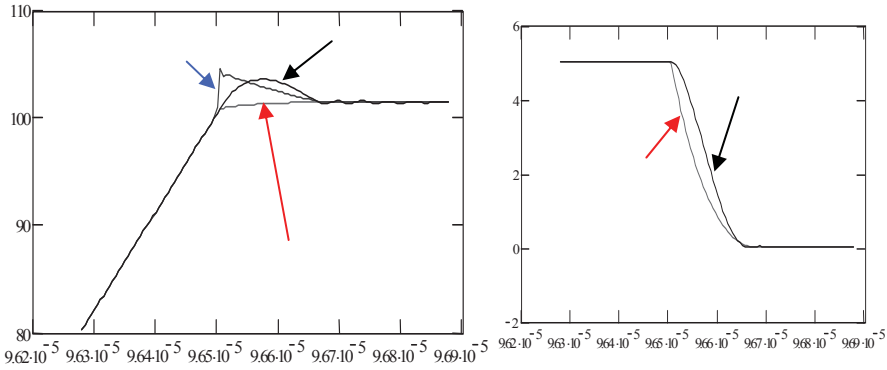


Figure 7.6. *For a commutation where the component is slowed (here 100 Ω as grid resistance), we can calculate the voltage surge afterwards without a too important mistake*

In conclusion, the minimal commutation cell to be simulated includes, in addition to the intentional active and passive elements (semiconductors, capacitors, possible magnetic components), inductive imperfections due to wiring. An indication of the average operating temperature is also necessary. A single commutation can be simulated with models as accurate as possible for each component mentioned.

7.3. The players in switching (respective roles of the component and its environment)

The semiconductor-wiring interactions are always very complex in nature since they involve the two semi-conductors of the commutation cell and electromagnetic environment. We were able to show that even if the determination of parasitic elements involves significant knowledge of electromagnetism and more or less complex resolution methods, the fact remains that their evaluation is linked to the knowledge of the strict geometry of the wiring. The geometric parameters are known with great precision and lead to reproducible results. It is not the same with the active components where, for example, the influence of the manufacturing process is fundamental.

Using finite element type fine modeling seems to us, given the current state of computers, a challenge. That is why we prefer a phenomenological approach quantitatively described by equations revealing analytical equations, efficient for various sensitivity analyses.

In this section, we are limited to the study of hard commutation phenomena, which is very widely used. The behavior of semiconductor commutation may appear easier to handle when commutation is of the "soft type", since the waveforms are governed by the passive components. We should not neglect the poor knowledge of recombination charge phenomena, for example in an IGBT under a voltage which is set through parasitic capacities.

Other restrictions: we are only discussing the MOSFET, the use of bipolar becoming increasingly marginal. Most of our conclusions may be adapted to the case of IGBT (with the exception of the tail current).

The purpose of this part is therefore to "dissect" a commutation cell made from a MOSFET-diode in order to determine "which does what" in a hard commutation, and if necessary, propose simple models which explicitly reflect these players in the commutation. The analyses that will follow are from various fine simulations, the only possible way of exploration. The study focuses on the commutation cell presented in Figure 7.7 below. It may indeed be shown that this representation based on three decoupled inductors is the simplest and most representative of phenomena [AKH 00, JEA 01, MER 96].

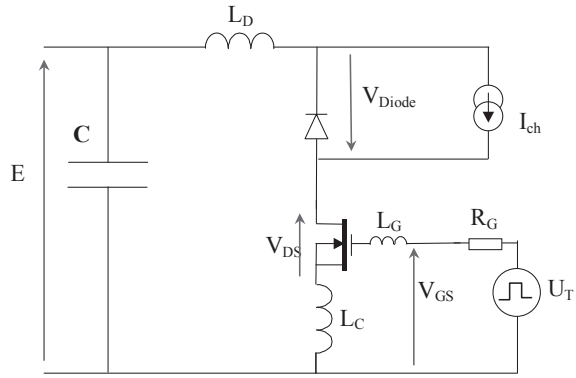


Figure 7.7. *Outline of the studied commutation cell and notations*

7.3.1. *Closure of the MOSFET*

7.3.1.1. *Qualitative analysis*

Figure 7.8 shows waveforms idealized during the closure of the MOSFET. First, the grid circuit is in charge until the grid source voltage reaches the threshold voltage Vth. Then the current source of MOSFET becomes active:

$$Imos = gm.(V_{gs} - V_{th})$$

During this phase, the diode is conductive, it can be concluded that its voltage is zero. The V_{ds} voltage of MOSFET remains relatively constant, there is only the voltage drop $(L_D + Lc).di/dt$ (with notations from Figure 7.7). As soon as the diode begins to "take the voltage" (i.e. as soon as an area of space charge appears), there is competition between the MOS speed, the speed of the diode and the Kirchoff equation governing the power circuit. Indeed, the diode voltage depends on the evolution of the size of the area of space charge. In addition, the grid circuit, as mentioned later, also governs the changing of the MOSFET voltage. Finally, the sum of voltages V_{ds}, V_{diode} and $(L_D+L_c).di/dt$ is kept constant at the value of continuous bus.

When commutation of the diode is completed, the current is constant, and Vds voltage continues to evolve, managed solely by the speed of the grid circuit and the component. The commutation is considered completed when the MOSFET reaches its ohmic area, i.e. that the voltage V_{ds} reaches $R_{dson}*I_o$. We should note that in some cases (low grid resistance or especially slow diode after the recovery), we can see the end of voltage switching before the end of current switching.

A particular case must be reported (Figure 7.9): it is either very fast MOSFET switching or a very strong inductor mesh (limit of switching circuit to aid the closure). In this case, voltage V_{ds} falls very rapidly to zero, due to strong term $(L_D+L_c).di/dt$ (either strong L_D+L_k or strong di/dt). As a result, $V_{diode} \approx 0$, $V_{ds} \approx 0$ and di/dt is therefore determined solely by continuous bus voltage, E and mesh inductance L_D+L_k. The rest of the commutation is completely governed by the diode.

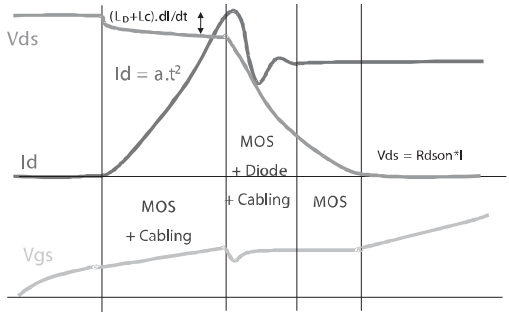


Figure 7.8. *Closing the MOSFET. The areas of dominance*

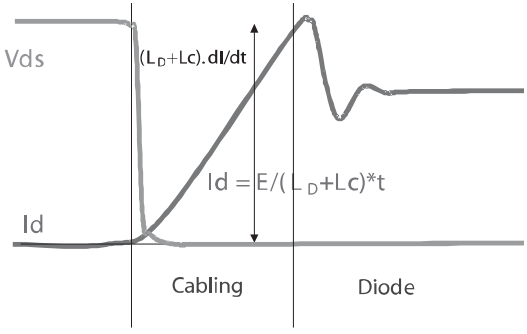


Figure 7.9. *Closing the MOSFET. Case of very fast MOSFET or very inductive wiring*

7.3.1.2. *Quantitative analysis*

The previous qualitative analysis has the merit of showing the different actors responsible for commutation waveforms. We will now examine more carefully the weight of these players during a sensitivity analysis.

We will consider the influence of inductor mesh and grid resistance, settings which are easy to tune. We will study more carefully the impact of semiconductors through their internal characteristics, that are closely related to their design (surface, doping, etc.).

7.3.1.2.1. Influence of wiring and grid resistance

Influence on the current

Here, the simulation allowed to vary easily mesh inductance L_D, and thus to assess the influence of this parameter for different grid resistances. We conducted several simulations (Figures 7.10, 7.11, 7.12). Within each series, we kept constant values of components (inductance and resistance) of the grid, and we vary the value of mesh inductance. In all cases we switched the same current of 7.5 Amps with a voltage of 200 V.

The first series of simulations was carried out with a grid resistance Rg = 2Ω.

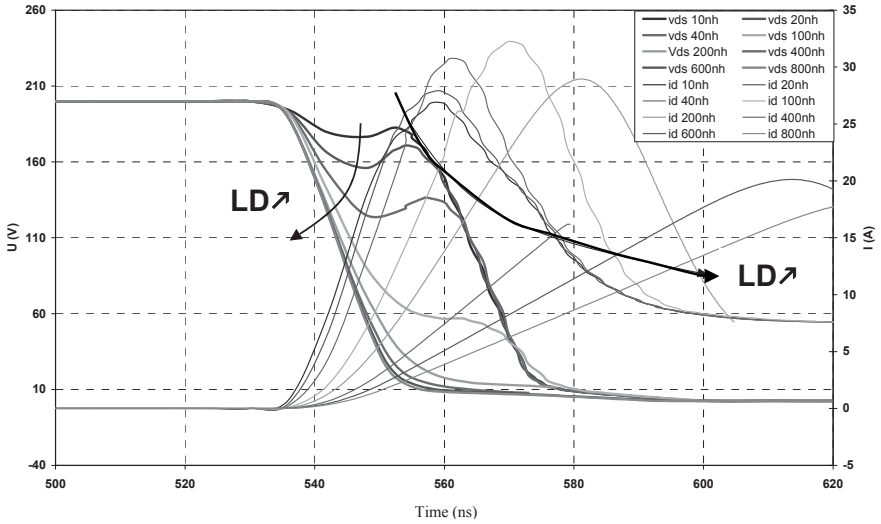


Figure 7.10. *Effect of inductance L_D for a low R_G (2 Ω)*

A second series of simulations was then carried out with a greater grid resistance Rg = 10 Ω.

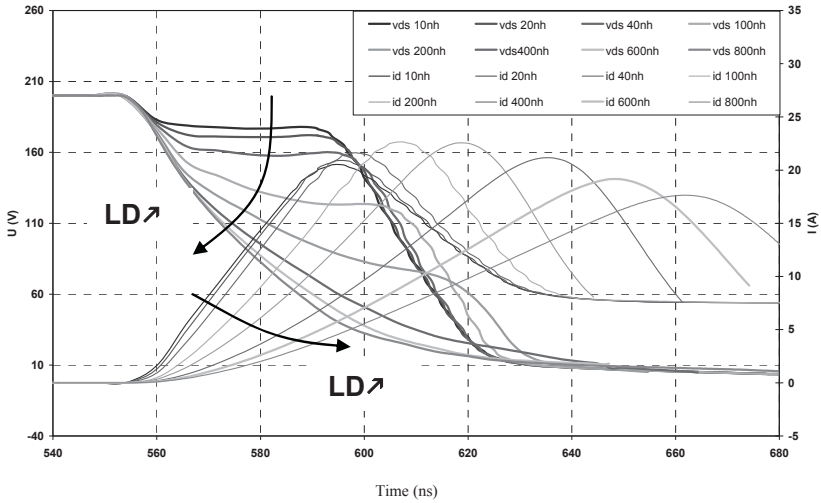


Figure 7.11. *Effect of inductance L_D for an average R_G (10 Ω)*

Finally a series of simulations was made with a more significant grid resistance (Rg = 50Ω).

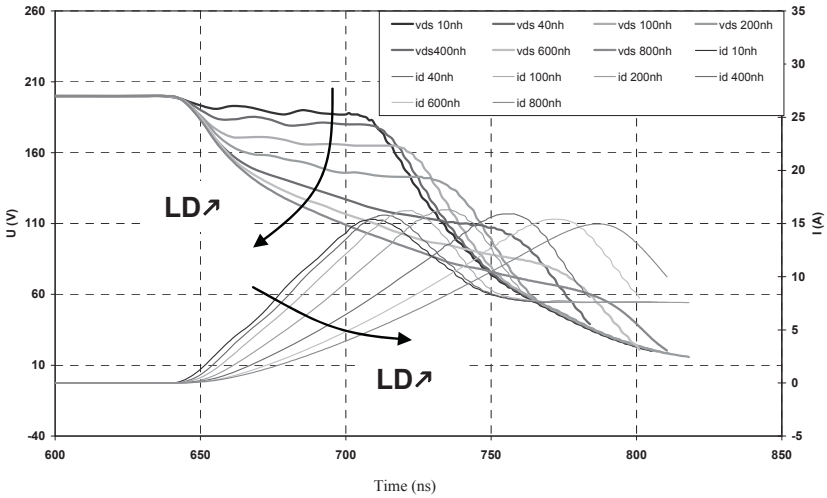


Figure 7.12. *Effect of inductance L_D for a large R_G (50 Ω)*

On the first series of simulations, we can observe that (when the value of inductance L_D increases) the inductive voltage drop equals the commutated voltage (E), and hence the value of dI_D/dt quickly reaches E/L_D. For more significant values of R_G, we find that the voltage drop never reaches the value E. This can be explained by the fact that the full discharge of capacity C_{ds} is required. $V_{GS} = V_{GD} + V_{DS}$, but during the commutation, V_{GS} # constant: to vary V_{DS}, it is required to vary V_{GD} by discharge of capacity C_{GD}. This discharge will be more rapid if the grid resistance R_G is lower.

From the previous curves, we can trace the evolution of dI_D/dt according to Ld (Figure 7.13), considering the area where the dI_D/dt is constant over time.

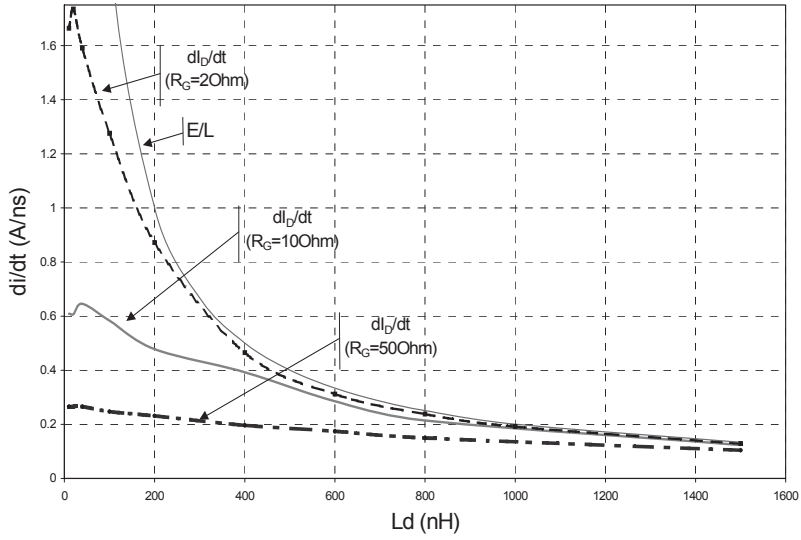


Figure 7.13. *Evolution of dI_D/d_t during the closure*

We note that for the large values of L_D and for low values of R_G, switching speed tends to E/LD: only the wiring then limits the commutation speed.

For large values of R_G, switching speed will be totally dependent on the circuit command and on MOSFET.

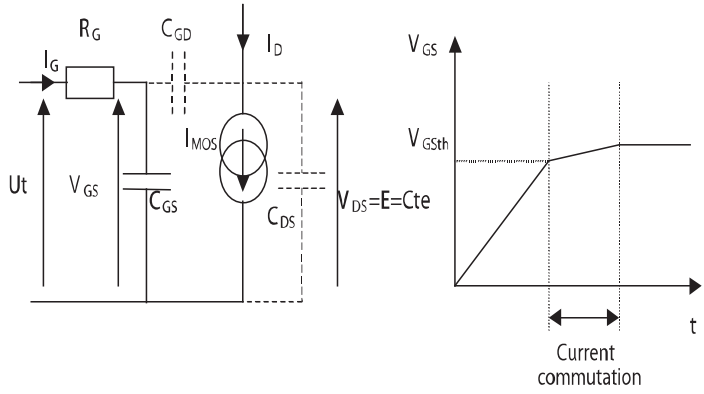


Figure 7.14. *Model of MOSFET for current switching when L_D is low and R_G is large*

During the current commutation, we assume that the voltage V_{GS} varies slightly and is almost V_{GSth}.

We consider that the current I_G is constant and is $I_G = (U_t - V_{GSth})/R_G$. As C_{GS} is much higher than C_{GD}, we consider that all current I_G flows in C_{GS}. Thus, we have:

$$V_{GS} = V_{GSth} + {I_G}/{C_{GS}} \cdot t$$

In addition, as L_D is low (in fact dI_D/dt low), the voltage V_{DS} will be regarded as constant and equal to E (no inductive voltage drop $L.dI_D/dt$). Thus, current through C_{DS} will be zero and therefore we obtain IMOS = I_D.

However, IMOS = $gm(V_{GS} - V_{GSth})$. Thus we have:

$$\frac{dI_D}{dt} = \frac{dI_{MOS}}{dt} = gm \cdot \left(\frac{Ut - V_{GSth}}{R_G \cdot C_{GS}} \right)$$

We note that for low values of L_D, dI_D/dt varies as $1/R_G$ by approximation gm ≈ constant, which is valid in the case of a sufficient level of switched current. The previous formulation will be valid only for large currents.

For larger values of L_D (or lower values of R_G), there is some competition between the two previous influences. [JEA 01, MER 96] then showed that the current switching speed is proportional to: $1/\sqrt{L_D \cdot R_G}$.

From there, we can break the evolution of dI_D/dt into three areas according to the mesh inductance L_D. The borders of these three areas are dependent on grid resistance R_G. They are summarized in the figure below.

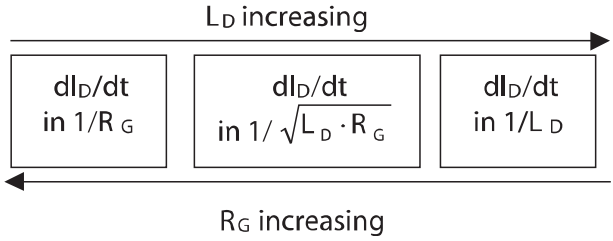


Figure 7.15. *Evolution of the switching speed of current according to R_G and L_D*

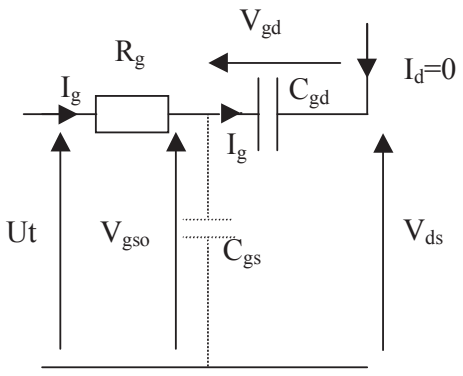
Influence on the voltage

[MER 96] proposed the following approach: we can consider that, at the first order, grid source voltage is maintained at a constant value noted:

V_{gso} ($V_{gso} = V_{th} + I_o/g_m$).

As a result the grid current ig is also constant and equals $ig = \dfrac{U_T - Vgso}{Rg}$.

This grid current charges (or discharges) capacity C_{gd}, causing the descent (or ascent) of voltage V_{ds}.



$$Vds + Vgd = Vgso$$

$$\Rightarrow \frac{dVds}{dt} + \frac{dVgd}{dt} = 0$$

$$ig = Cgd \cdot \frac{dVgd}{dt}$$

$$\boxed{\Rightarrow \frac{dVds}{dt} = \frac{Vgso - U_T}{Rg \cdot Cgd}}$$

Figure 7.16. *Equivalent schematic during the voltage commutation, and formula of the dV/dt*

The formula produced by this simple reasoning shows the role of grid resistance, and MOSFET parasitic capacitance.

7.3.1.2.2. Influence of MOSFET parameters

Parasitic capacities

We have just seen the influence of capacity C_{gd} (or "Miller" capacity) on the speed of evolution in voltage. We can easily show through simulations that if we keep the product $R_g.C_{gd}$ constant, the dV/dt is well preserved. The rest of this section is interested in the switching speed of current.

We will confirm the influence of this or that capacity. Starting from the reference values corresponding to the capacities identified on a MOSFET (IRF450FI), we have multiplied them by a coefficient. This method helps to keep developments consistent.

We can see that C_{GS} and C_{GD} have a strong influence on the moment of the beginning of the commutation. This is consistent with the model from Figure 7.14. Indeed, the first phase of the commutation, prior to the start of the evolution of current or voltage, is made up of the capacity charge C_{iss} ($C_{GS} + C_{GD}$). We note, however, that during the closure, the influence of C_{GD} (C_{rss}) on the moment of the beginning of the commutation, does not seems obvious here. This is because at the beginning of closure, the V_{DS} voltage is significant, and values of C_{rss} are low when V_{DS} is large, compared to those of C_{iss}.

We have identified in Table 7.1 the impact of these changes on the current commutation, including the evolution of (dId/dt) max (switching speed of current).

	Value of $\left(\frac{dI_D}{dt}\right)_{max}$ A/ns		Value of $\left(\frac{dI_D}{dt}\right)_{max}$ A/ns		Value of $\left(\frac{dI_D}{dt}\right)_{max}$ A/ns
Cgs*0.25	1.44	Cds*0.25	1.12	Cgd*0.25	2.12
Cgs*0.5	1.32	Cds*0.5	1.19	Cgd*0.5	1.71
Cgs*2	1.21	Cds*2	1.37	Cgd*2	1.14
Cgs*4	0.9	Cds*4	1.55	Cgd*4	0.88

Table 7.1. *Influence of CGS, CDS, CGD on the evolution of current ID (closure of the MOSFET)*

Regarding the current speed dI_D/dt, only C_{gd} seems to be predominant. This is because during these phases, command voltage (V_{GS}) and power voltage (V_{DS}) are almost constant. However, in full rigor V_{GS} and V_{DS} are not constant, it is therefore normal that the associated capacities (C_{GS} and C_{DS}) have an influence on the speed of change of the switched current.

Source current of the MOSFET

As in the case of capacities, we can confirm the importance of taking into account the non-constant gain *gm* (recall: $I_D = gm \cdot \left(V_{GS} - V_{GSth}\right)$ is not consistent with non-constant *gm*) of the current source according to VGS. We then looked at the importance of the value of *k* gain on the switching speed of current. In our case, the quadratic modeling $\left(I_D = k\left(V_{GS} - V_{GSth}\right)^2\right)$ is valid for I_D less than about 25 Amps, we have therefore taken care not to exceed this value during simulations using different values of *k*.

The influence of non-linearity in the modeling of the power source is highlighted in Figure 7.17. The gains $I_D = gm(VGS)$ used are shown below. The simulation conditions are as follows: rg = 10 Ω,LD = 40 nH, L_{dio} =10 nH, L_G =20 nH, E = 200 V and I commuted = 7.5 Amps.

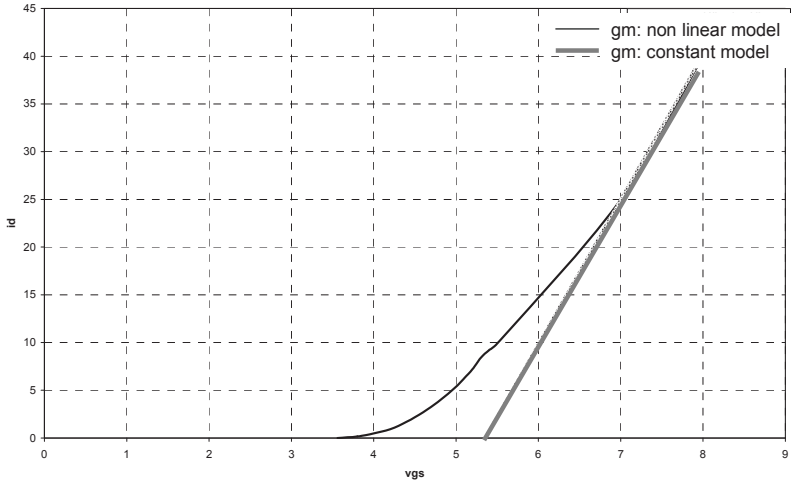


Figure 7.17. *Constant or non linear model for gm. Constant gm leads to linear variation of ID as a function of Vgs*

NOTE. – We note that for significant currents (beyond 25 Amps in this case), *gm* is constant.

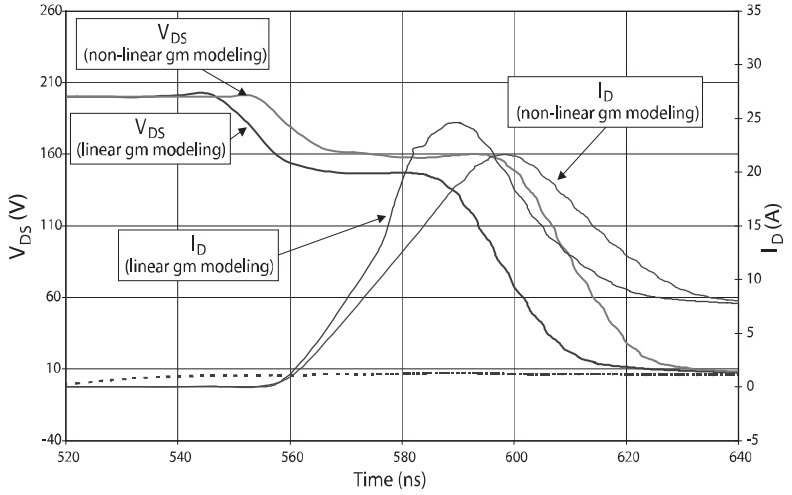


Figure 7.18. *Influence of modeling of the current source of MOSFET*

The non-linearity of the current source (variable gain *gm*) is naturally visible during the current commutation. Regarding the influence of the coefficient *k*, it is necessary to distinguish the closure from the opening of the MOSFET.

At the closing phase it can be seen that the current IMOS is almost equal to the current ID (neglecting the current passing through CDS as VDS is almost constant). Now IMOS depends on VGS, thus *k* gain has a strong influence. Note that this reasoning is valid only if the inductive voltage drop $L_D \cdot dI_D / dt$ is not too significant, i.e. if voltage VDS does not tend to 0: in this case the current would be imposed only by the mesh equation ($E = L_D \cdot dI_D / dt$).

The simulation results are available in the table below.

	Values of $\left(\frac{dI_D}{dt}\right)_{max}$ A/ns
k = 3.5	1.33
k = 5	1.47
k = 7.5	1.62
k = 10	1.74

Table 7.2. *Influence of gain k on current ID evolution (closing MOSFET)*

The gain *k* of the controlled current source is part of the parameters strongly influencing the switching speed of the current at the closure of the MOSFET. The static characteristic of the MOSFET (and its variation depending on the temperature) must be taken into account for associations of components, particularly for the balance of currents when setting in parallel.

7.3.1.2.3. Influence of the diode

We will see here the influence of parameters τ (carrier lifetime), W (thickness of the ν area with low doping) and Sa (active section of the diode).

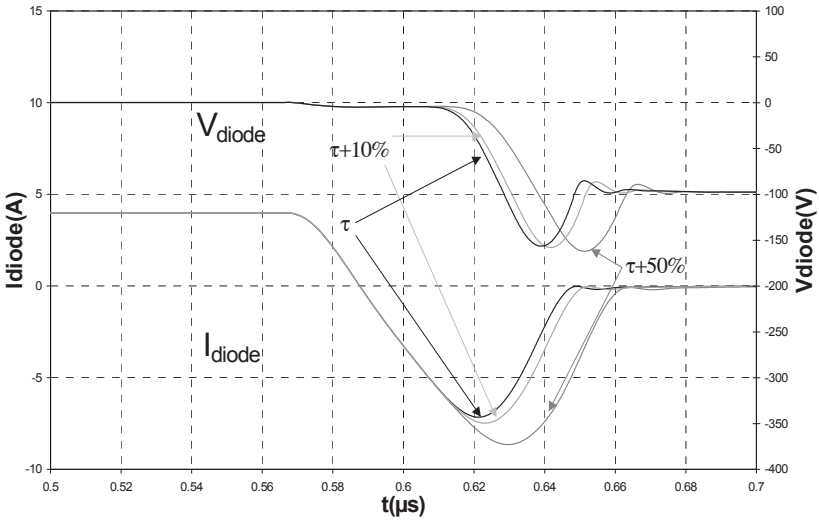


Figure 7.19. *Influence of parameter τ*

Figure 7.19 shows the evolution of currents and voltages depending on parameter τ. Compared to a reference value (corresponding to a real diode), we have increased it by 10% and 50%.

The switching losses increase of 4% (respectively 20%) and the value of the recovery current of 3% (respectively 13%) when the carrier lifetime increases by 10% (respectively 50%). We note that the carrier lifetime τ strongly influences the level of recovery current (Figure 7.19), and hence losses, but the influence on the switching speed of voltage remains negligible. Parameter τ is a parameter that is difficult to estimate (OCVD method [GHE 98]), but its influence on the recovery current is important. It will be relatively easy to determine this by superimposing experimental waveforms on simulated waveforms.

Using a similar procedure to the study of the influence of τ, we see that the thickness of the *W* zone with low doping (zone ν) specifically affects the voltage switching speed. According to Figure 7.20, an increase of *W* leads to increased switching speed. Note also that in our case, increasing *W* also creates a slight decrease in the recovery current, but this is not always the case. Indeed, depending on lifetime τ, the stored charge may increase or decrease with an increase of *W*. In the case of a long lifetime (recovery diode for example), an increase of *W* would

produce an increase in the stored charge, and therefore an increase of the recovery current.

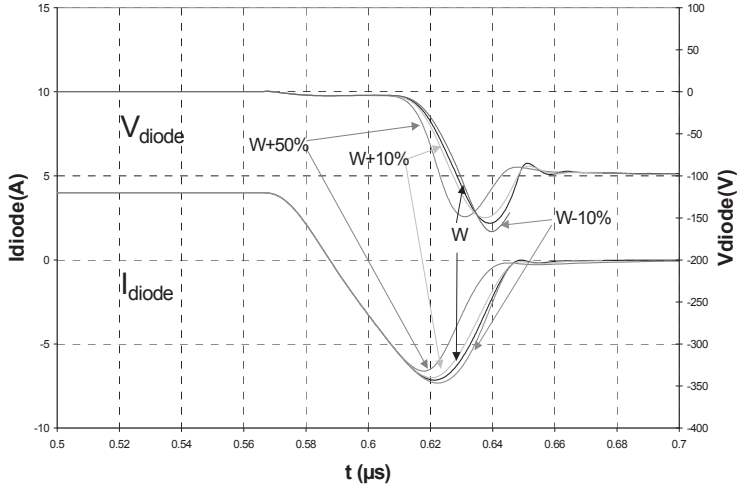


Figure 7.20. *Influence of W (width of the low doped zone)*

We then studied the influence of Sa, the active area of the diode. We note that its increase (Figure 7.21) has little influence on commutation waveforms.

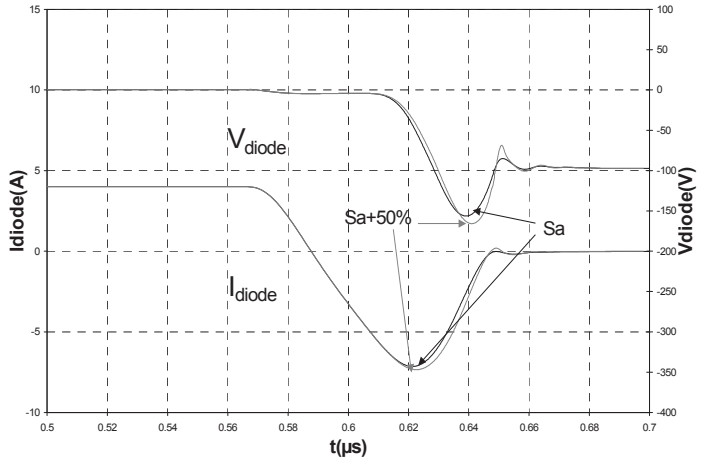


Figure 7.21. *Influence of Sa (active surface of the diode)*

Thus, we found a number of parameters involved in the closure of the diode. The mobility and the parameters of carrier recombination are little changed from one component to another; furthermore, commutation waveforms are not very sensitive to them. The geometric parameters (*W* and *Sa*) are relatively easy to identify using techniques such as spreading resistance (characteristic capacity – voltage c (v)) [GHE 98]. These identification techniques will also inform us on the doping profile of the ν area. In conclusion, we can use the waveforms at the closure of the MOSFET to identify the value of the carrier lifetime τ: this parameter, which is influential during the recovery phase, may be identified by comparing simulation to measurement.

7.3.2. *Opening of the MOSFET*

7.3.2.1. *Qualitative analysis*

Figure 7.22 shows idealized waveforms at the opening of a MOSFET. First, the grid circuit is discharged until the grid voltage reaches the source voltage Vth + Io/gm. At this point, the voltage is maintained at this threshold Vgs value, and the grid current, then roughly constant, ensures the development of voltage Vds via the discharge capacity Cgd. Note we assume here that the diode can change its space charge (hence its voltage) almost instantly or, in other words, it does not limit the rise of MOSFET voltage. Once the voltage Vds reaches the value of the continuous power bus, the diode is under zero voltage and becomes conductive. Then a current commutation occurs within the MOSFET, which will be governed by the component, its grid circuit and the wiring parameters. The commutation ends when the current and voltage oscillations caused by the MOSFET capacitors in the off state and wiring inductance LD + LC are damped. Hence the diode has little influence during this commutation phase (opening), insofar its over voltage during closing is neglected.

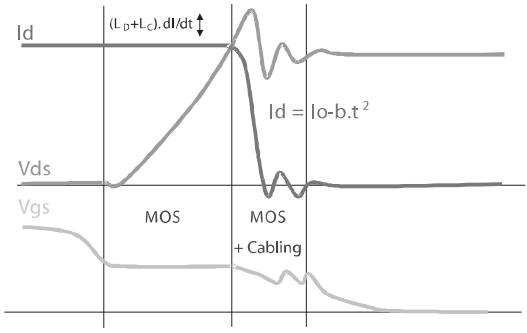


Figure 7.22. *Opening of MOSFET. Areas of dominance*

As for closing, the particular case of an aid circuit to the commutation may be mentioned, even if with hard commutation, no "spontaneous" scenario (without an aid capacitor for the opening) can be observed. In this case, the drain current falls sharply, the aid capacitor to the commutation is then charged by the load current. The voltage slope is then Io/Cds, and becomes independent of the component.

7.3.2.2. *Quantitative analysis*

7.3.2.2.1. Influence of wiring and grid resistance

Influence on the current

The phenomena are not very different from the case of closure: there is a new time competition between component speed (managed by its grid circuit) and the wiring. Figure 7.23 shows, for example, the influence of grid resistance on switching speed dI/dt, and Figure 7.24 that of the influence of inductance LD. It should be noted, as discussed for the closure, that large grid resistance or high mesh inductors slow down current switching speed. Figure 7.24 also shows that for "large" grid resistances, inductance LD has no more influence on the dI/dt.

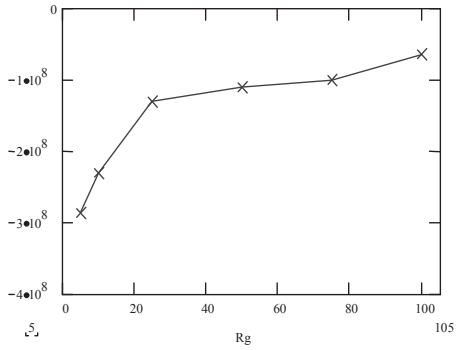


Figure 7.23. *Change in dI/dt depending on the grid resistance (fine simulation)*

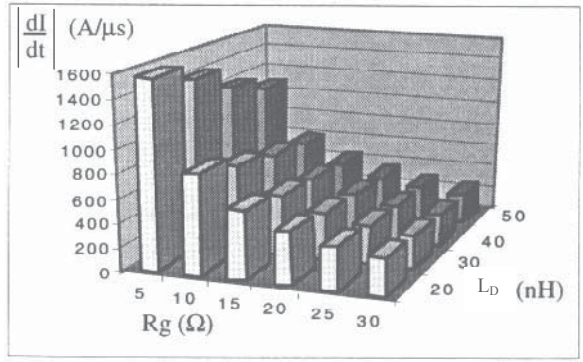


Figure 7.24. *Respective influences of grid resistance and mesh inductance on di/dt at the opening (Lk constant = 5 nH)*

Another example is the influence of the Lc common inductor (defined in Figure 7.7), which is able to make changes in the power current and re-inject on the grid circuit a voltage Lc.dI/dt, which amends the grid current and therefore the switching speed, and may even lead to the restoration of conduction of the component. This phenomenon, shown experimentally in Figure 7.25 may also occur at the closure.

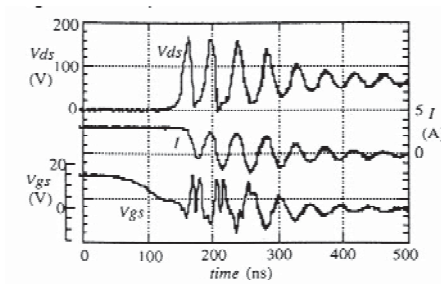


Figure 7.25. *Perturbation of a static converter by the common impedance at the opening of MOSFET (experimental waveforms from [MER 96])*

Figure 7.26 shows the influence of the common inductance of source Lc on the speed of evolution of the current at the opening, but also at the closure.

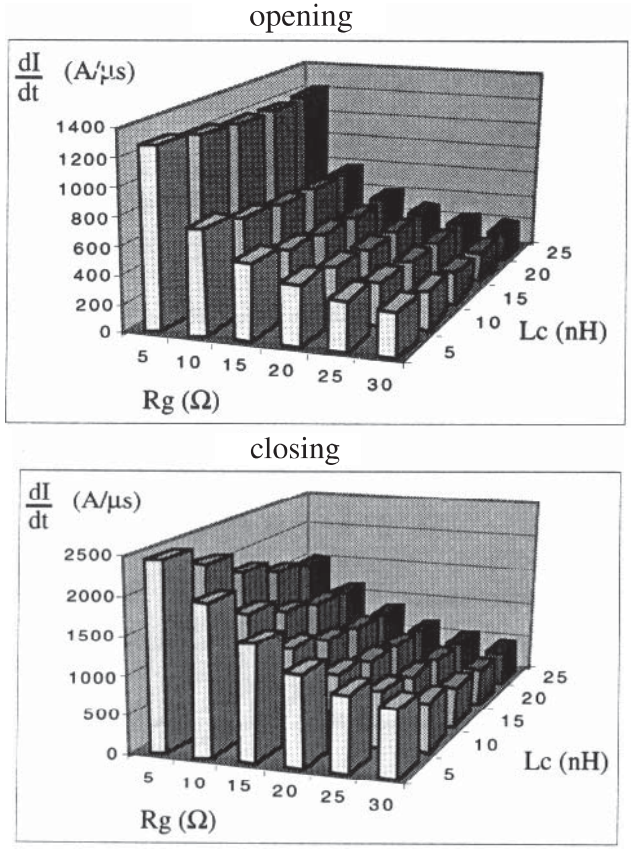


Figure 7.26. *Influence of common inductance L, for a mesh inductor LD + Lc constant, at the opening and closing [MER 96]*

The set of equations to calculate the speed of evolution of the current, to separate the respective influences of the total inductance of the switching mesh (LD + Lc) and of the common inductance Lc, is not particularly simple [JEA 01, LAU 99], and will not be repeated here. Note that [AKH 00] offers elegant wiring solutions to address this problem.

Influence on the voltage

The approach proposed earlier remains valid, as well as the proposed equations, which underlines the role of grid resistance Rg and "Miller" capacity Cgd.

7.3.2.2.2. Influence of MOSFET parameters

Influence of parasitic capacities

First, reiterate the need to take into account non-linearity of these capacities, particularly for low values of VDS [FAR 94]. We have made here two simulations, the first (Figure 7.37a) takes into account the phenomenon of variable capacities, the second does not. We note, in Figure 7.37a that voltage evolves in a non-constant way, whereas in Figure 7.37b, evolution is almost linear for most of the commutation.

This is particularly noticeable on the assessment of switching losses. There is a difference of almost 15% between the two approaches (45.7 μJoule in the case of taking into account the non-linearity, 39.8 μJoule in other cases).

Regarding now the rate of change in voltage (dVds/dt), the relatively simple approach proposed for closure (b) [MER 96], if it is still valid by changing the value of UT, does not take into account the capacity Cds. With such an analysis, we cannot see how an external aid capacitor to the commutation could intervene in the dV/dt. We can find in [JEA 01] a somewhat more detailed analysis in order to take into account a snubber capacitor Cds which aids the commutation.

Regarding the influence of parasitic capacities on the current, Table 7.3 (obtained in the same manner as for the closure) shows the influence of parasitic capacity on the evolution of (dId/dt) max (commutation speed of current).

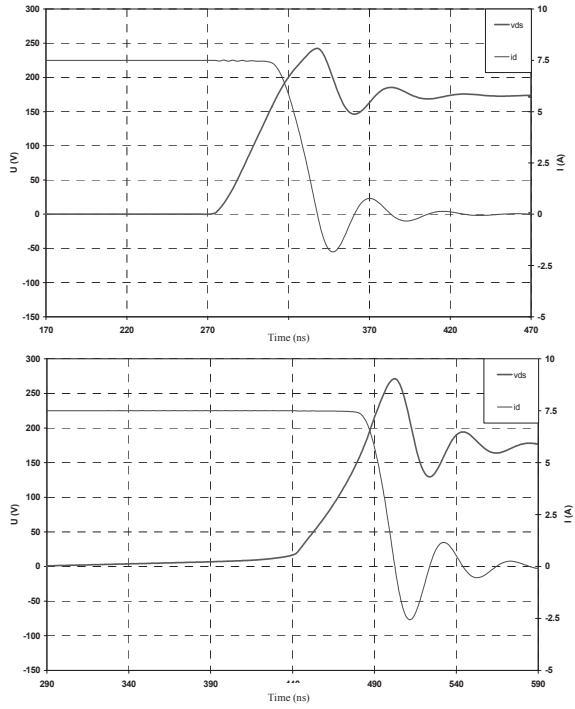


Figure 7.27. *Simulated waveforms at opening of a MOSFET*
(a) taking into account non-linearity of the parasitic capacities
(b) without taking into account non-linearity of the parasitic capacities

	Value of $\left(\frac{dI_D}{dt}\right)_{max}$ A/ns		Value of $\left(\frac{dI_D}{dt}\right)_{max}$ A/ns		Value of $\left(\frac{dI_D}{dt}\right)_{max}$ A/ns
Cgs*0.25	–17.8	Cds*0.25	–19.7	Cgd*0.25	–17.2
Cgs*0.5	–17.4	Cds*0.5	–19.3	Cgd*0.5	–16.9
Cgs*2	–15.8	Cds*2	–13.7	Cgd*2	–15.6
Cgs*4	–14	Cds*4	–9.56	Cgd*4	–14.7

Table 7.3. *Influence of CGS, CDS, CGD on the evolution of current ID (opening of MOSFET)*

As with the closing, the influence of Cgs capacity is very low, since it is under an almost constant voltage. The influence of Cgd is confirmed, as for the closure.

The strong influence of the increase of Cds is certainly justified here by a change of switching behavior ("snubber" effect).

Influence of the current source

In the case of opening, the situation is different from the closure: Table 7.4 shows the low influence of gain *k*. We can attribute this phenomenon to a competition between speed of grid circuit and speed of power circuit. Drive current IG flows through CGD and imposes voltage VDS, the current ID is then imposed by the law of meshes ($E = VDS + L_D \cdot dI_D / dt$). The speed of evolution of this current is the result of a compromise between the equation of the power mesh and the equation of the grid circuit.

	Value of $\left(\frac{dI_D}{dt}\right)_{max}$ A/ns
k = 3.5	–15.8
k = 5	–16.1
k = 7.5	–16.4
k = 10	–16.7

Table 7.4. *Influence of gain k on evolution of current ID (closing of MOSFET)*

7.3.2.2.3. Influence of the diode

The diode as little influence. Figure 7.28 shows the changes in waveforms of current and voltage for 50% variations of parameters τ, *Sa* and *W*.

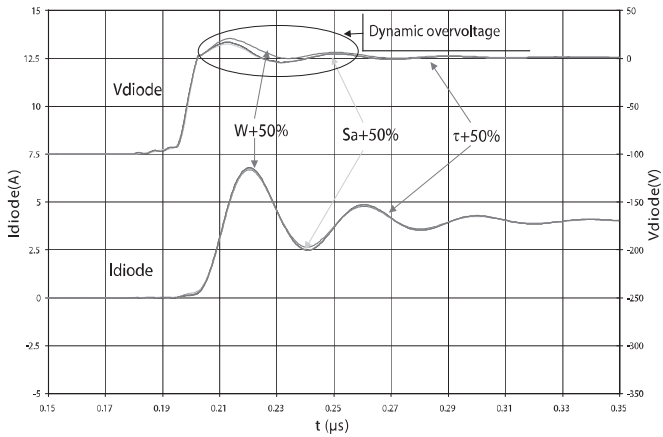


Figure 7.28. *Influence of the diode at the opening of MOSFET*

The above figure shows that changes in the physical parameters of the diode have little influence on commutation waveforms, except on the voltage surge when the diode is switched on [KOL 00]. In particular, we note that the dVDS/dt is controlled by the MOSFET alone.

7.3.3. *Summary*

Based on previous results, we can establish a table summarizing the relative influences of the different elements analyzed (0 = zero, + = little importance, ++ = important, +++ = very important). This table has been completed about dVDS/dt using the results of [MER 96], as well as those developed in the following section.

	CGD	CDS	CGS	LG	LD	k or gm	Iload
dID/dt	+++	++	++	0	+++	+++	0
dVDS/dt	+++	++	+	0	0	+	+

Table 7.5. *Summary of influences for the closure of MOSFET*

	CGD	CDS	CGS	LG	LD	k or gm
dID/dt	++	+++	+	0	+++	+
dVDS/dt	+++	++	+	0	0	+

Table 7.6. *Summary of influences for the opening of MOSFET*

Parameters Ut and VGSth drive the value of current IG through the grid resistance RG, these three parameters therefore influencing the charges and discharges of capacities CGD and CGS, and hence thereby both the early moments of commutation and switching speeds.

Note also that the capacities of the MOSFET influence the switching speeds of voltage. During these phases, the VGS voltage is almost constant, and the influence of capacity CGS will be low. The charge (or discharge) of the CGD capacity determines almost the entire evolution of voltage, its influence will be very important. In some cases, the CDS capacity limits dVDS/dt through the load current at the value Iload/CDS. Its influence may be significant.

7.4. References

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