Power Electronics Semiconductor Devices
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Chapter 6

Modeling Connections

6.1. Introduction

6.1.1. *Importance of interconnections in power electronics*

Interconnections or, more simply, wiring, have always played an important role in power electronics. The message has always been "cut wire length and decouple the closest semiconductor commutation". Times have not changed, but the era of laboratory converters gave way to series production, where we must now be able to integrate the presence of wiring or interconnections from the moment of conception. The modern components (IGBT) available today are characterized by higher and higher "di over dt". In the high power field (rail traction, naval propulsion, etc.), an area where we encounter probably the biggest constraints currently, current gradients di/dt increase to a few thousand amperes per microsecond, and apply strong constraints on wiring and on switching cell diodes. The existence of such constraints comes from the parallel implementation of several semiconductors, multiplying through this the di/dt in interconnections imposed by the number of chips involved. The phasing out of boxes such as "press-packs", involving wiring by massive conductors naturally very inductive, allows us to suppress more and more often snubber circuits which affect the simplicity and reliability of systems. As a result, the absence of passive components to properly tackle waveforms during the commutations requires new small inductive techniques for wiring. Examples include the development of bus bars regarding applications of medium to high power, or the

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development of isolated metal substrate (IMS) applications for lower power dedicated to large series production.

6.1.2. *The constraints imposed on the interconnections*

The increase in the required performances of converters always leads to more electrical requirements on the interconnections. We can discuss constraints linked to power electronics, electromagnetic compatibility, but also to the reliability of these new techniques.

Consider first the power electronics aspect: we can see that brutal transitions generate significant surge at the interconnection terminals endangering semiconductors. The performance increase of power converters requires putting in parallel and gradually setting a series of semi-conductors, while guaranteeing the compactness and simple solutions. We must therefore try to remove passive circuits necessary for balancing currents or voltages. We will therefore demand these new interconnections to ensure a supply of semiconductors more and more perfect.

Regarding the electromagnetic compatibility (EMC), the increase in switching frequency with the aim of improving the performance of converters (quality of the pulse-width modulation, reducing the size of the filters) and the increased compactness can lead to problems that are called EMC problems. Indeed, the increase in switching frequencies and, by extension, frequencies generated during the commutations, and the shrinking of distances inside devices, lead to increasingly significant acute couplings. We must take care of linkages between power conductors and wires carrying signals.

From a standard point of view, and since shieldings are cut off for cost reasons, it becomes important to be concerned about interconnection radiation and its impact on the spread of conducted noises.

Finally, regarding the reliability of these interconnections, we try to keep voltages ever higher through the dielectric constituents of bus bars or IMS. The operating temperature of these devices, which can reach several dozen degrees Celsius, limits the life time of the equipment. In addition, mechanical constraints are also taken into consideration for high power applications.. These constraints have different consequences. On the one hand, the connection itself may be destroyed in the case of a short circuit (tear, opening of pressed bus bars). However, on the other hand, the forces passed by the bus bars or the massive conductors on the components they supply may damage them.

We are therefore able, after this list, to see how a modern interconnection becomes a fully real component, the design of which results from complex

calculations and sometimes involves many disciplines such as electromagnetism, mechanics, thermal and power electronics (for interactions with semiconductors).

6.1.3. *The various interconnections used in power electronics*

The use of different interconnection technologies depends mainly on the level of power. From the highest level of power to the lowest, we encounter the achievements described below.

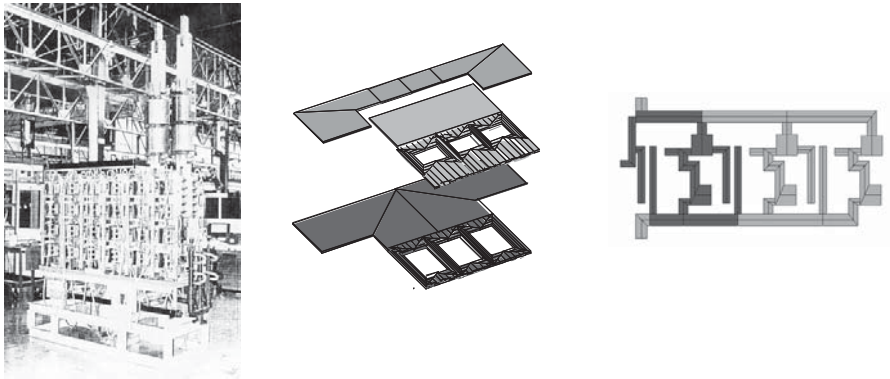
Electrochemistry or electrometallurgy applications involve currents of the order of hundreds of thousands of amperes. Although several converters are made in parallel for reasons of redundancy, currents are still extremely important (several dozen kiloamperes). Generally, the interconnections are made using massive aluminum conductors. We may also cite problems with current distribution between diodes in parallel induced by the dissymmetry of circuits (Figure 6.1a).

We must of course not forget induction heating, when powers and high frequencies make control of wiring inductances necessary. A strong knowledge has been gained in this field.

The railway applications or, more generally, traction applications, require rapid semiconductors (IGBT), but also smaller currents (typically 1,000 amps). This is the domain of bus bars composed of sheets of copper separated by sheets of dielectric (Figure 6.1b).

The automotive applications, requiring both a high reliability and important mass production, are mainly using isolated metallic substrate (IMS) techniques (Figure 6.1c). The wave weld and the heatsink ability of the substrate makes it highly attractive. Also note the achievements of hybrid power modules made on an alumina support. Although the electrical and thermal characteristics are different, they are strongly similar to the case of IMS in its concept.

Finally, the traditional power supplies, for general purposes, often use the classic printed circuit on an epoxy support.



a) b) c)

Figure 6.1. *Different types of connections: a) massive bars, b) erupted bus bar, c) IMS*

6.1.4. *The need to model the interconnections*

On the one hand, the willingness to develop products in an increasingly quick time and at the lowest cost tends to exclude more and more the use of prototypes, at least for applications other than those developed on printed circuit. On the other hand, as noted above, when the power density is greater, the number of constraints and their severity are increased. It is therefore easy to understand that meeting these constraints becomes increasingly difficult empirically or heuristically. It therefore becomes gradually essential to develop models of interconnections mainly reflecting electrical phenomena, but also thermal and mechanical.

If, for the moment, we merely want to know the behavior of electrical interconnections, we need models that can be applied in software commonly used in power electronics (SABER, SPICE, SIMPLORER, etc.).

In this chapter, we propose a method of modeling (PEEC), which seems well suited to the topology of power converters. This method is based on a program called InCa3D. It is possible that in the case of circuit boards, other methods borrowed from microwaves (transmission lines, moments method for calculating the parameters) appear to be more efficient. However, their scope is not as broad and the many examples that we were able to deal with, belonging to all categories of power, confirm us in this approach.

6.2. The method of modeling

6.2.1. *The required qualities*

To be used without restriction in the industry by engineers in power electronics, it was necessary to propose a method that will not require too much skill in electromagnetism or in the field of numerical methods. In particular, the finite element method, widely used for the design of electrical machines, requires a heavy investment which is not justifiable in power electronics, where the design of interconnections, even if it is a decisive phase in a project, has only a limited place in the whole design of a converter.

By the same logic, it is desirable to obtain a modeling of interconnections in the form of located elements easy to integrate in an analysis software of electrical circuits. At the moment, a model in the form of resistances, inductances and mutual inductance, possibly dependent on frequency, is valid for the frequency range extending from continuous to a few megahertz, or even a few dozen megahertz. This model is quite sufficient for the majority of interconnections from medium to high power. Now, in the field of printed circuit boards, or IMS, capacity between tracks and ground plane (radiator, chassis) must be added to take proper account of phenomena.

One of the results provided by the software must be an easy evaluation of the inductive weight of each section of the global interconnection. Considering the hunting down of nanohenry in power electronics, the engineer must know what is the most inductive portion and thus focus its efforts wisely, i.e. consider changes to geometry where it is actually possible to intervene and where the gain is substantial, and finally to know the financial implications. Regarding the interactions between conductors (power and control), the ability to directly edit the value of the mutual inductance is something appreciable.

In power electronics, although the switching frequency is still low, especially for high power (below 10 kHz), current commutations show contributions in frequency bands that are quite high. Even if the well known formula 0.35/tm, where tm is the rise time of the signal can be criticized, however it gives an idea of the frequency with which must be evaluated the parasitic elements of interconnections.

For a large majority of cases, the variation of interconnection parameters with the frequency is quite marginal. The impact of a change in the loop inductance of 50% for a commutation of semiconductors has no known impact both in terms of losses and in terms of spectra. Note that the change in inductance of an interconnection with the frequency depends on the change of distribution of current lines inside the conductor (Figure 6.2).

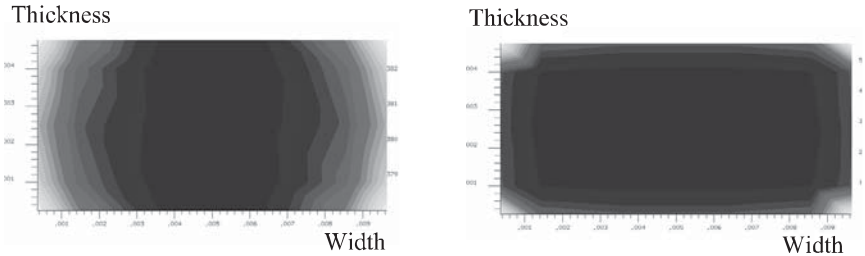


Figure 6.2. *Distribution of current lines for two different frequencies (100 Hz on left, 10 kHz on right) obtained with InCa3D*

The change in interconnection parameters with the frequency comes from two causes that are quite distinct from each other [DJO 94].

The first is what is commonly known as the skin effect, which is to concentrate currents on the edges of conductors and therefore increase the resistance of the conductor since the passage for the proposed current is lower. This effect occurs for a single conductor into the vacuum and submitted to a field created by its own current. The new distribution of current lines maintains the symmetries presented by the straight section of the conductor.

The second effect is the proximity effect, which occurs when the conductor is subject to an outfield that can be produced by a neighboring conductor. In particular, this effect often breaks the symmetry in the distribution of current lines mentioned previously.

6.2.2. *Which method of modeling?*

Having demonstrated the need to model the interconnections with an electric model, it remains to establish formulations to be used depending on the scope and especially the methods of resolution. For calculation of inductance or mutual inductances, Maxwell equations are required, perhaps simplified on the basis of assumptions.

One method of solving these equations, the most commonly used and that which first comes to mind is the numerical finite elements method. It achieves a partition of the problem (or mesh) to form 3D known elements (tetrahedron, brick, etc.) and assesses the unknown function at nodes of these elements. By interpolation throughout the area, the value of the function is then known everywhere. This method is very powerful when it is applied for mapping fields and fluxes (rotating

machines, transformers, etc.). However, it becomes less obvious when we must treat these data in order to obtain the values of global inductances and mutual inductances. Indeed, in the case of interconnections, for the mutual effect of a conductor on others, it will have to be fed by a current or voltage generator (boundary conditions of used formulations) and the various fluxes picked up by other conductors will have to be calculated. This involves as many resolutions as conductors in the problem (one less exactly) to fill in the matrix impedance. Moreover, the mesh size of the problem is closely linked to a particular frequency. Thus, the change in electrical parameters with the frequency requires as many resolutions as the number of values of frequencies. Finally, the structures studied here are mainly static converters for which it is necessary to have an estimate of the contribution of wiring in the air and in the absence of magnetic materials. The finite element method requires us, however, to mesh the entire field, including air, which increases the size of the problem to be solved. The mesh, on which ultimately rests a large part of the finite element method, poses a large problem when it comes to modeling conductors very thin and wide. The designer will be confronted with this when bus bars will be used to achieve the interconnections. Meshing this stacking of conductive plates very thin and very close, with finite elements of good quality, results in unacceptable resolution time. Using elements with potential drops is possible for a single layer, but impossible at present for a stack. For all these reasons, the local approach for solving Maxwell's equations is therefore excluded to model the interconnections [BOT 94].

When conductors become too long, another method exists. This is the TLM approach, which replaces the conductor by a transmission line. This approach is used in microwaves for which the geometry of conductors is simple. It can be adapted to power electronics for special wiring (PCB) as discussed further. The challenge is to correctly model side effects when conductors are short and wide. The complex 3D geometric structures are difficult to model. Finally, it requires the presence of a ground plane used as a reference for electromagnetic coupling. The latter is present in certain applications with medium power and high frequency. However, this is not the case in high power applications. Also, this method of resolution is rejected when it comes to modeling the interconnections of complex geometric shapes for medium frequencies and high powers.

We have just seen that using a local approach is not feasible, as well as a research approach with distributed elements. In addition, we will turn to a comprehensive approach to solving the problem whose result will be the values of localized electrical equivalent schematics of conductors.

This method of solving Maxwell equations exists. This is the PEEC (*Partial Element Equivalent Circuit)* method, which decomposes the vector potential and its circulation on each portion of the straight conductor, to evaluate the contribution of

each of them on the total inductance of the current loop. Thus, the immediate results are partial elements, inductances and mutual inductances between conductors. The side effects are automatically reflected in this approach.

6.2.3. *Brief description of the PEEC method*

This method comes from A.E. Ruehli, an engineer at IBM, who in the 1970s was instructed to model the interconnections of digital computer boards [RUE 72, RUE 74, RUE 79]. He noted that the transmission line method was not sufficient to correctly model all types of interconnections. In particular, the very short interconnections inside integrated circuits did not seem to be properly represented. This was mainly due to the invalidity of the basic assumption of the transmission line method: the existence of fields crossing the propagation direction of the current, mainly for short interconnections. At its origin, only an inductive and resistive modeling was carried out, then improvements were made on electrostatic phenomena, and then were taken into account delays related to propagation.

Our main contribution in adapting this method to power electronics focuses on techniques to represent the skin effect and proximity effect by meshing rectangular sections and all the analytical work that was undertaken to correctly represent 3D structures and very complex connections.

6.2.3.1. *Principle*

This method is based on the partial element concept: partial resistance, inductance and mutual inductances. More specifically, it is based on the fact that a current loop can be broken into straight components each contributing to the impedance of the total closed circuit. The vector potential and its circulation are decomposed on each element, which can determine their contribution. The total resistance of a current loop will be the sum of partial resistances of each element and its total inductance is the sum of all inductances and mutual between these inductances:

$$R_b = \sum_{n=1}^{N} R_{pn}$$

$$L_b = \sum_{m=1}^{N} \sum_{n=1}^{N} M_{pmn}$$

– Rpn: partial resistance of element *n*;

– Mpmn: partial mutual inductance of element *n* on element *m*;

– Mpnn: partial inductance of element *n*.

The value of the partial resistance of an element is given by:

$$R_s = \frac{\rho L}{S}$$

– ρ: resistivity of the material (Ω.m);

– L and S: length (m) and section (m^2) of the element.

In air and in the absence of magnetic material, the partial mutual between two massive parallel conductors is calculated, also from an analytical expression after successive integrations of vector potential. By assuming a uniform current density in the straight section of the two conductors, this value depends only on geometric characteristics of these elements (Figure 6.3) [HOE 65]. The partial inductance is then a mutual element on itself (E = P = l3 = 0, l1 = l2, a = c, b = d).

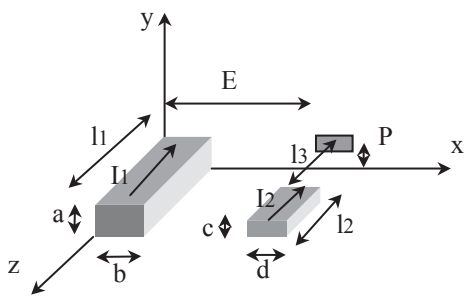


Figure 6.3. *Definitions for the calculation of the partial elements with the PEEC method*

We give below the exact formula (equation E) because it is the basis of calculations of inductances and it is important to know the different elements it comprises. The value of M is obtained in μH with a definition of the sides in cm.

To implement these formulations in case of power electronic interconnections, we must dissociate the geometry of connections into elements of straight conductors for which the assumption of uniform current density is valid.

$$M=\frac{0.001}{abcd}\left[\left[\left[\left(\frac{y^2z^2}{4}-\frac{y^4}{24}-\frac{z^4}{24}\right)x\ln\frac{x+\sqrt{x^2+y^2+z^2}}{\sqrt{y^2+z^2}}+\right.\right.\right.$$

$$\left(\frac{x^2z^2}{4}-\frac{x^4}{24}-\frac{z^4}{24}\right)y\ln\frac{y+\sqrt{x^2+y^2+z^2}}{\sqrt{x^2+z^2}}+$$

$$\left(\frac{y^2x^2}{4}-\frac{y^4}{24}-\frac{x^4}{24}\right)z\ln\frac{z+\sqrt{x^2+y^2+z^2}}{\sqrt{y^2+x^2}}+$$

$$\frac{1}{60}\left(x^4+y^4+z^4-3y^2x^2-3y^2z^2-3x^2z^2\right)\sqrt{x^2+y^2+z^2}-$$

$$\frac{xyz^3}{6}Arctg\frac{xy}{z\sqrt{x^2+y^2+z^2}}-\frac{xy^3z}{6}Arctg\frac{xz}{y\sqrt{x^2+y^2+z^2}}-$$

$$\left.\left.\frac{x^3yz}{6}Arctg\frac{zy}{x\sqrt{x^2+y^2+z^2}}\right]_{E+d-b,E}^{E-b,E+d}(x)\right]_{P+c-a,P}^{P-a,P+c}(y)\Bigg]_{l3+l2-l1,l3}^{l3-l1,l3+l2}$$

(equation E), with:

$$\left[\left[\left[f(x,y,z)\right]_{q2,q4}^{q1,q3}(x)\right]_{r2,r4}^{r1,r3}(y)\right]_{s2,24}^{s1,s3}(z)=\sum_{i=1}^{4}\sum_{j=1}^{4}\sum_{k=1}^{4}(-1)^{i+j+k+1}f(qi,rj,sk)$$

6.2.3.2. *1D, 2D… assumptions*

The geometric shape of conductors encountered in power electronics will, in most cases, make possible the assumption of unidirectional lines of current. This is the case with massive bars and conductors for which the length is large compared to the width and thickness. The conductor model will be a LR series circuit (Figure 6.4a).

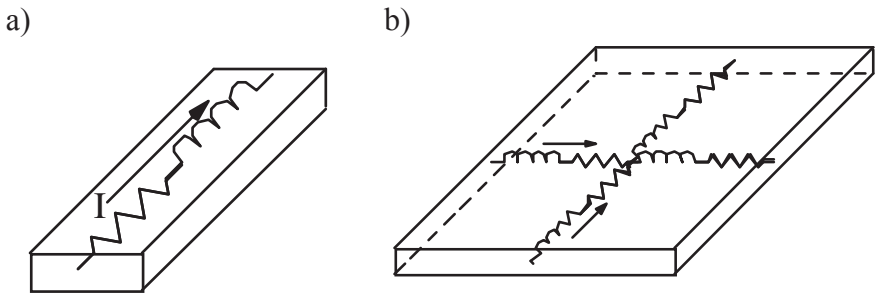


Figure 6.4. *(a) 1D and (b) 2D model*

Considering bus bars, interconnections for which the current often comes from a point to be distributed later, this 1D assumption is no longer valid. A 2D model is then developed (Figure 6.4b), which allows current lines to go in two perpendicular directions.

Then in this case only circulating currents in the thickness of the bus bar plates are neglected. Given the frequency range, this assumption is justified. It is therefore not necessary at this time to develop a 3D model.

6.2.3.3. *Ground plane*

The structures in power electronics are often located on a radiator or a chassis which acts as a ground plane. Hence currents flow inside it and their influence will modify the electrical characteristics of interconnections located above.

The easiest way of modeling is the image method [PED 91]. It replaces a conductor above a perfect ground plane (infinite and infinitely conductive) with the same conductor and its image fed by opposed currents if it is parallel to the plane (Figure 6.5a) and currents of same direction if it is perpendicular to the plane (Figure 6.5b). In the first case, the equivalent inductance is $L'_1 = L_1 - M_{1i}$ and in the second case $L'_1 = L_1 + M_{1i}$ (partial resistance is unchanged because the ground plane is considered ideal).

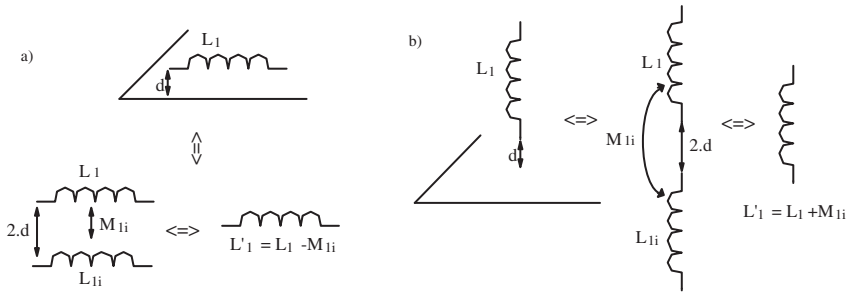


Figure 6.5. *Different positions of the conductor located above the ground plane*

The assumption of a perfect ground plane is in most cases valid: it is sufficient to have a material being either very good conductor (copper or aluminum) and with transverse dimensions relatively large compared to dimensions of the circuit located above [SCH 94].

Another problem exists when the structure is surrounded by a box, then you are in the presence of several ground planes. In this case, the images method is very difficult to apply because it can lead to a large number of images.

If it is not possible to assume a perfect ground plane, it must be seen as a conductor and meshed in the same way as other elements of the circuit. In this case, take a lot of care with the meshing, which will require the use of, in most cases, 2D elements.

6.2.3.4. *Mesh*

The underlying assumption used is that the current density is uniform in the straight section of conductors. We have already seen that for large plates, the current direction was not known, which led to 2D mesh-types (section 6.2.3.2). Another issue that may require a mesh is the frequency. Indeed, with increasing frequency, a redistribution of current lines occurs (skin effect): this is not symmetric if there are other conductors close to the one under consideration (proximity effect).

For a straight conductor, for which current lines have a preferred direction, the section will be only meshed into elements of smaller section and of the same length (Figure 6.6). In this latter case, the length of conductors will not be discretized assuming that frequency is not too high (length of the conductor compared to the wavelength). This reduces the number of elements, as compared to a finite element method.

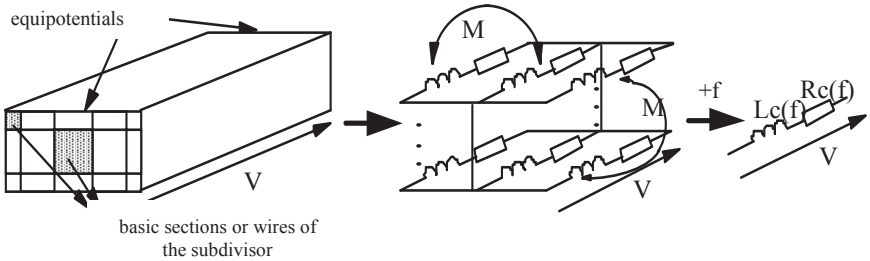


Figure 6.6. *Obtaining electrical characteristics of a conductor depending on the frequency with a subdivision of its section*

In the case of a 2D model, the mesh will be finer depending on the frequency. This methodology has been implemented in a simulator called InCa3D®, consisting of a 3D geometric descriptor, a mesh assistant, a calculation module and a post treatment.

6.3. The printed circuit board

The method described above obviously applies in the case of printed circuit board. Analytical formulations are similar to equation E: they are even intermediate results obtained in the course of integration. However, with generic software, they add no particular advantage:

– the printed circuit board is used in many fields other than power electronics, many works have been completed, including high-frequency electronics;

– modeling them is based on the transmission line theory, possibly multiconductors. Then the parameters of these lines are calculated: resistances, inductances, capacitances and couplings, all these quantities are per unit length parameters;

– the use of these methods is allowed in the case of printed circuit boards, because the plane structure offers simple geometries, unlike static power converters, which include 3D wiring.

6.3.1. *Introduction*

Printed wiring is commonly used in high frequency and average power converters. Also, modeling must be able to simultaneously take into account all electromagnetic phenomena:

– self- and mutual inductance between tracks;

– capacitive effect in relation to a plane and between tracks;

– resistive effect, function of frequency: skin effect and proximity effect;

– existence of a conductor near the wiring (chassis or heatsink).

In order to achieve a simulation tool for printed wiring dedicated to computer-aided design, the analytical method must be inexpensive considering computing time. If we further consider that the electric field in a print conductor has only one direction, that of its greatest length, the problem becomes 1D, facilitating further formulations. Thus, the proposed method uses line theory. It allows assuming some adaptations to answer the imposed criteria. The principle used is to share a printed wiring in rectangular segments, oriented in the direction of the current, themselves divided into thin conductors placed in parallel (Figure 6.7). On this decomposition line theory can thus apply. Indeed, the analytical expressions of the per unit length inductances, capacitances and mutual couplings for this type of row form conductors are known [LEE 86]. The calculation of row currents allows us, knowing the voltage conditions at the ends, to determine an overall equivalent impedance and finally its representation by a "circuit" model. Thus, a conductor is represented by a four pole impedance referenced to a ground plane, which can take into account both the differential mode and common mode effects.

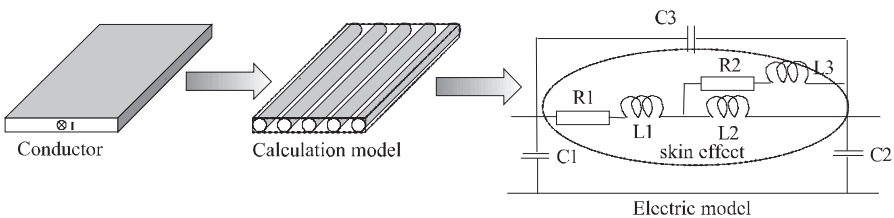


Figure 6.7. *Principle of modeling*

6.3.2. *Thin wire method*

6.3.2.1. *Principle of the method*

Studies cited in [MAC 93, PET 96] showed equivalence between a micro strip line and a bundle of *N* thin conductors parallel between them (Figure 6.8), insofar as a minimal distribution of thin conductors per centimeter is respected.

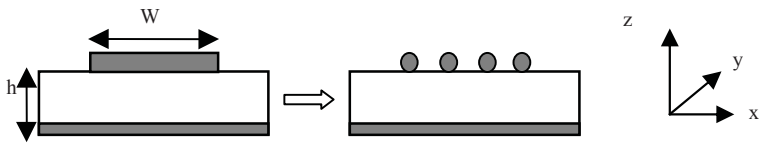


Figure 6.8. *Equivalence to a set of thin conductors*

These *N* thin conductors are immersed in an environment which characterizes an equivalent dielectric substrate. The principle is to calculate the electrical parameters of the line from geometry and material. The frequency resolution method is based on the transmission line theory for multiconductors. This model requires the resolution of the system:

$$\frac{d^2[I]}{dz^2} = [Y].[Z].[I]$$

$$\frac{d^2[V]}{dz^2} = [Z].[Y].[V]$$

The matrices of linear impedance and admittance [Z] and [Y] are defined from:

$$[Z] = [R] + j\omega[L]$$

$$[Y] = [G] + j\omega[C]$$

[L] and [R] represent matrices of linear inductance and resistance; [C] and [G] symbolize matrices of linear capacity and conductance. The latter is supposed to be zero as we consider no losses in the dielectric: [G] = 0.

Depending on the operating frequency, a quasi-TEM mode is assumed to propagate throughout the micro strip line. It equates to a pure TEM mode. Although the propagation environment is inhomogenous, the structure may be treated as an homogenous environment of effective permittivity ε_{eff}. This value is calculated from expressions of by Wheeler, Schneider and Hammerstad [SCH 69, WHE 77]. It can also be calculated by the finite element method in 2D. The capacitance matrix is deducted from the inductance matrix by a simple inversion.

$$[C] = \mu_0 . \varepsilon_{eff} . [L]^{-1}$$

6.3.2.2. *Solving equations*

The resolution of a system requires us to reduce the product (Y)(Z) to diagonal to move in the modal basis. In fact, the product (Y)(Z) is not diagonal since losses in the lines are taken into account. The matrices of passage (Ti), respectively (Tv) are determined, they allow the reduction to diagonal of (Y)(Z), respectively (Z)(Y):

$$(I) = (Ti)\ (i)$$

$$(V) = (Tv)\ (v)$$

where (i) and (v) are matrices of the current and voltage in the modal basis. The differential equation of the second order of the matrix system is then written:

$$\left(\frac{d^2 i}{dz^2}\right) - (\gamma_p)^2(i) = 0$$

$(\gamma_p)^2$=(Ti) – 1(Y)(Z)(Ti) is the diagonal matrix for propagation in the modal basis. The solution of the system is given by:

$$[i(z)] = e^{[\gamma_p]z}[A] + e^{-[\gamma_p]z}[B]$$

where [A] and [B] are determined using the boundary conditions. The matrices of the current and voltage in the original basis are obtained by the relationship above.

6.3.3. *Expressions of per unit length parameters*

The analytical formulation of per unit length parameters is the focal point of this method. This should help take into account all the effects you want to represent, whatever the geometries and disposition of thin conductors (not parallel, non-coplanar, etc.) even in non necessarily homogeneous media. We present two families of formulation: the first assumes that the conductor is very long compared to its width (ratio greater than 4). In this case we use simple formulations since we assume infinite conductors. In a second case, we take into account the finished length of thin conductors. The formulation is more complex and we use the PEEC method applied to cylindrical conductors of finished length. Finally, the computing time is linked to the meshing of printed conductor. Two types of meshing are proposed:

– a linear distribution which has the disadvantage of computational cost increasing with the width of the track;

– a geometric distribution which allows a constant number of thin wires regardless of the width of the track, and is therefore more interesting for calculation time, but needs to be adapted according to the operating frequency range.

6.3.3.1. *Linear distribution of thin wires*

The determination of per unit length parameters reduces to the calculations of inductance and resistance matrices. Consider a set of *N* thin wires coupled over a ground plane (Figure 6.9).

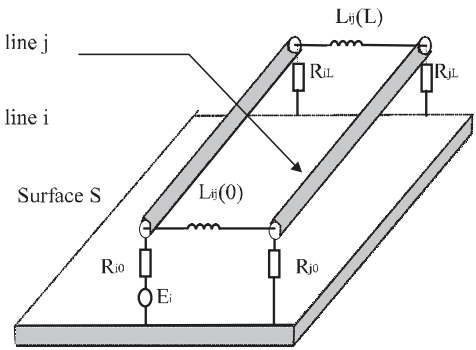


Figure 6.9. *Electric representation*

The elements of the inductance matrix (Lij) are calculated by the traditional analytical formulations of cylindrical conductors, assuming the thin wires of infinite length and interwire distance d_0 much higher than their diameter ϕ. This is equal to the thickness of the micro strip line.

$$L_{ii} = \frac{\mu_0}{2\pi}.\ln\left(\frac{4.h}{\phi}\right) + L_{\text{int}\,erne}$$

$$L_{ij} = \frac{\mu_0}{4\pi}.\ln\left(1 + \frac{4.h^2}{d_{ij}^2}\right)$$

where dij means the interwire distance.

Skin effect and proximity effect phenomena are also taken into account as well as the change in internal inductance of thin wires. Recent work [GAU 00] gives an analytical expression of the internal per unit length inductance using Kelvin

functions. However, the contribution of internal inductance has little influence on the accuracy of the "thin wire" model made up of conductors of small cylindrical diameter. It is nevertheless important for conductors of large section. The resistive effect is important in the frequency band studied in power electronics. Also, the conductor model introduced the per unit length resistance matrix [R] which depends directly on the frequency. In the case of the linear distribution of conductors, the per unit length equivalent resistance of a thin wire is expressed by:

$$R_{fil} = N.\frac{\gamma}{\sqrt{2}.\sigma.(w+\phi)}.F_R_{Bessel}\left(2\gamma.\frac{w.\phi}{w+\phi}\right)$$

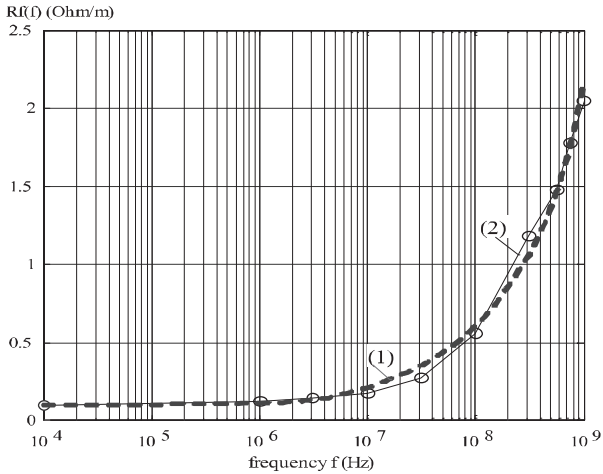
N: number of thin wires describing the printed conductor.

F_RBessel is defined by:

$$F_R_{Bessel}(x) = \frac{Ber_0(x)Bei_1(x) - Ber_0(x)Ber_1(x) - Bei_0(x)Bei_1(x) - Bei_0(x)Ber_1(x)}{Ber_1^2(x) + Bei_1^2(x)}$$

with: $\gamma = \sqrt{\omega\mu\sigma}$ Ω/m

Figure 6.10 shows that this analytical function properly reflects the evolution of resistance with frequency. The reference values are derived by calculating with finite elements. The example is a track 5mm wide and 35 µm thick.



Curve (1) (dotted) corresponds directly to the evolution of this function.

Curve (2) is the result obtained by calculating the resistance by finite elements

Figure 6.10. *Evolution of linear resistance for a 5 mm wide track: comparison between thin wire method and finite element method*

It is therefore possible to obtain a total impedance of a printed track with a good accuracy, as shown in Figure 6.11. However, one of the disadvantages of this method results from increasing the size of matrices with the width of the tracks. Accordingly, the computing time can become prohibitive. Also one change is to adopt a non-linear distribution of thin wires.

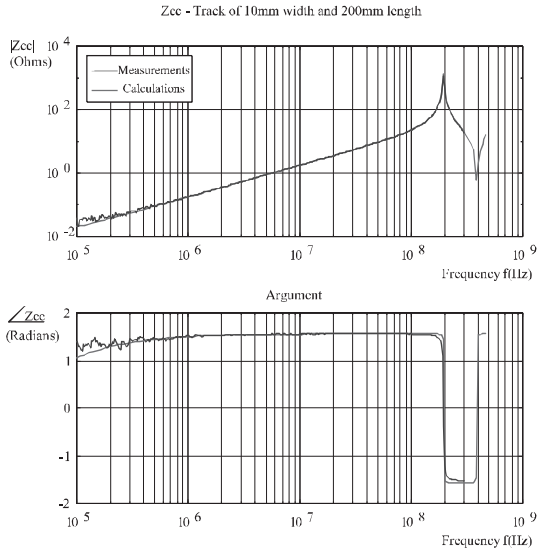


Figure 6.11. *Example of track impedance calculated by the thin wire method*

6.3.3.2. *Non-linear distribution of thin wires*

The observation of the distribution of current density in a track led to develop a new distribution of wires in order to reduce the computing time. To this effect, thin conductors are concentrated on the edges of the track (Figure 6.12). The calculation of the interwire distance achieved through an arithmetic reason r:

$$d_n = d_0 + n.r$$

n represents the number of wires in the first half of the track. Given the symmetry of the system, the distribution of wires is made solely for the first half of the track. The total number of wires is equal to:

$$n_{\text{wire}} = 2\ (\text{n} + 1) + 1$$

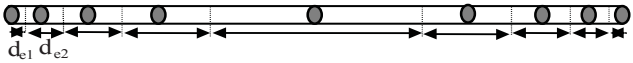


Figure 6.12. *Non-linear distribution of thin wires*

The vector = [de1 de2 ... de*n*] can represent the position of thin wires.

with: $d_{e1} = \frac{d_0}{2}$ and $d_{en} = \frac{1}{2}.\left(d_{n-2} + d_{n-1}\right)$

We then obtain the expressions of inductance and resistance matrices:

$$\left[L_{ij}\right] = \frac{\mu_0}{4\pi}.\ln\left(1 + 4.h^2.\left[d_{ij}\right]^{-1}\right)$$

$$\left[R\right] = \frac{F_R_{Bessel}\left(\phi,\delta\right)}{\sigma.\phi}.\left[d_e\right]^{-1}$$

[dij] is the distribution matrix of non-linear thin wires and δ the skin thickness.

Figure 6.13 shows a comparison between the two meshing modes of a printed track for calculating the current density in the section. Both methods converge satisfactorily; the gain in computing time is very significant.

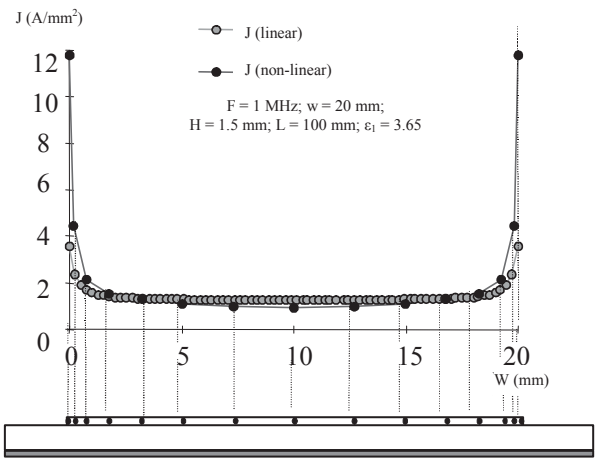


Figure 6.13. *Comparison of current densities depending on the meshing of the track*

This method reduces the CPU time. It maintains a constant calculation time whatever the width of the track. However, the distribution of conductors is optimized for a certain frequency range. The distribution must be adapted according to this criterion. For example, some values of computing time are given in Table 6.1, depending on the method. The calculation concerns the impedance of a line for 60 values of frequencies compatible with the chosen distribution.

Width of the line studied (mm)	Number of wires in the linear case	CPU time (s)	Number of wires in the non-linear case	CPU time (s)
5	20	71.73	15	15.44
10	40	307.75	15	15.22
20	80	1540	15	15.16

Table 6.1. *CPU time depending on discretization of thin wires*

6.3.3.3. *General formulation of per unit length inductances*

In the previous sections, the per unit length parameters are independent of the length, which introduces errors in the case of short tracks. To solve this issue, the principle is to use the PEEC method to calculate equivalent linear parameters for cylindrical thin wires of finished length.

The calculation of the terms of matrix [L] requires taking into account the neighboring conductors denoted wire 2 and its respective image wire 3 (Figure 6.14).

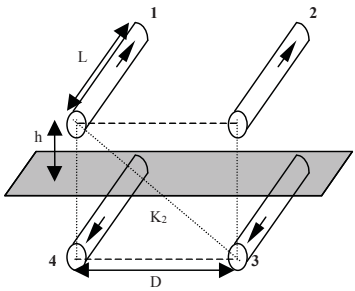


Figure 6.14. *Coupling thin wires above ground plane*

By definition: Lij = Lp12 – Lp13 (H/m)

This concludes formulations given by:

$$L_{p12} = \frac{\mu_0}{2\pi}.\left\{\ln\left[\frac{L}{D} + \sqrt{1+\left(\frac{L}{D}\right)^2}\right] - \sqrt{1+\left(\frac{D}{L}\right)^2} + \frac{D}{L}\right\}$$

$$L_{p13} = \frac{\mu_0}{2\pi}.\left\{\ln\left[\frac{L}{K_2} + \sqrt{1+\left(\frac{L}{K_2}\right)^2}\right] - \sqrt{1+\left(\frac{K_2}{L}\right)^2} + \frac{K_2}{L}\right\}$$

where: $K_2 = \sqrt{D^2 + 4h^2}$.

If the length is large compared to the width of the line, we find the analytical expressions above. Figure 6.15 shows the change in the per unit length mutual inductance for two thin wires distant from 175 µm, located in a conductor having a width of 5 mm, a thickness of 35 µm and placed at 1.5 mm above the ground plane.

Depending on the length of the track, we can choose a formulation independent of the length or that takes into account, this is to optimize the CPU time.

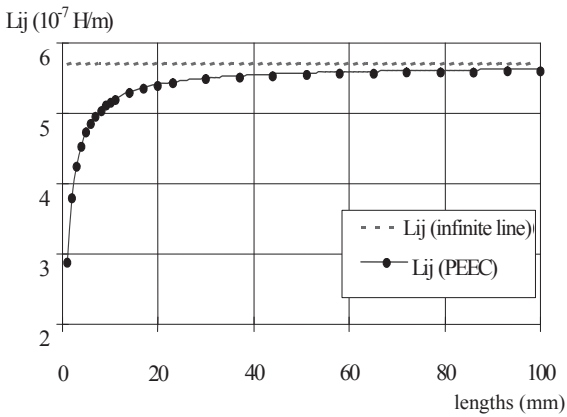
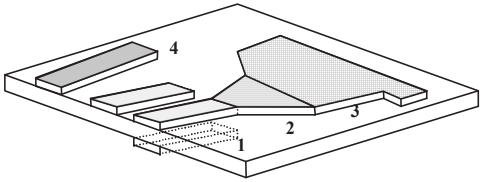


Figure 6.15. *Change in linear mutual inductance with the length*

6.3.3.4. *Extension of the method to non-parallel lines and multilayer lines*

It is possible to generalize the previous formulation to cases of non-parallel and non-coplanar conductors. This extension allows us to treat all types of conductors, including multilayer circuits (Figure 6.16).



1: double face tracks

2: enlarged tracks

3: massive tracks

4: coupled tracks, parallel or not

Figure 6.16. *Examples of topologies that can be managed by the thin wire method*

The difficulty in this case concerns areas whose permittivities are different. Line theory applies well in an isotropic environment. Different methods exist for determining an equivalent permittivity [BAT 89]. To illustrate case 2 (enlarged tracks) an example of formulation is given in the case of coplanar conductors.

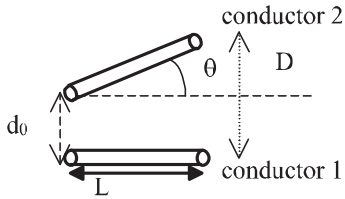


Figure 6.17. *Non-parallel conductors*

$$L_{ij} = \frac{\mu_0 \cos\theta}{4\pi.\sqrt{1+\tan^2\theta}}.\ln\left\{\frac{\left(\frac{L}{2}+A+\sqrt{\left(\frac{L}{2}+A\right)^2+B^2}\right).\left(-\frac{L}{2}+A+\sqrt{\left(-\frac{L}{2}+A\right)^2+C}\right)}{\left(-\frac{L}{2}+A+\sqrt{\left(-\frac{L}{2}+A\right)^2+B^2}\right).\left(\frac{L}{2}+A+\sqrt{\left(\frac{L}{2}+A\right)^2+C}\right)}\right\}$$

The constants A, B and C are determined by the length L and the distance d_0. The curve of Figure 6.18 illustrates the evolution of per unit length mutual inductance L_{ij} depending on the angle θ. It should be noted that mutual inductance between the two orthogonal conductors is quasi-zero.

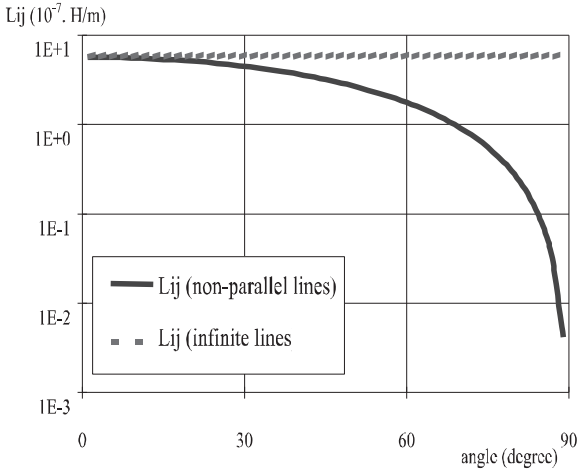


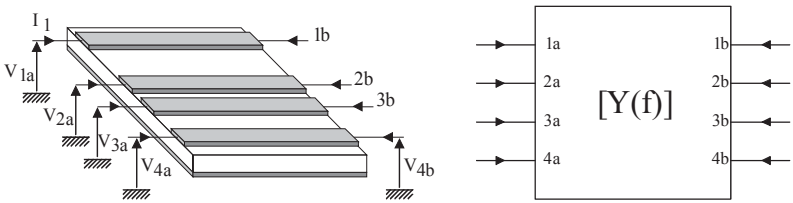
Figure 6.18. *Change in mutual depending on the angle*

The previous formulation is generally applied to non-coplanar conductors, which can solve the case of a multi-layer printed circuit board.

6.3.4. *Representation by multi-poles, "circuit" modeling*

6.3.4.1. *Couplings between tracks*

The thin wires method allows us to calculate the coupling between different segments of parallel tracks. We must then consider all these segments of the track as a multi-pole, characterized by an overall matrix of admittance [Y]. In the case of N segments of coupled tracks, the multi-pole is connected to $2N$ ports and the corresponding matrix of admittance has a dimension $2N \times 2N$.



4 tracks ⇔ 8 ports: matrix Y(f) 8 × 8

Figure 6.19. *8 port multi-pole*

Because of symmetries, the number of different primary admittances defined in the matrix Y(f) is less than the total number of elements of the matrix. Thus, for a 8 × 8 matrix (4 coupled tracks), there are actually 20 different admittances defined. If a complete model of electrical coupling between the four tracks is sought, these 20 admittances must be correctly reproduced, which implies a complex electric model and complex calculation of parameters, and therefore a high CPU time. A possible simplification is to only take into account linkages between adjacent tracks. The former problem was thus reduced to the study of three couplings between two tracks, which is the calculation of three 4 x 4 matrices.

To limit the number of couplings to be taken into account in the printed circuit model, a criterion has been defined in [PET 96]. The criterion allows determining the significant couplings considering the geometrical characteristics of segments of track, and maximum current that can cross each segment.

6.3.4.2. *"Circuit" modeling*

The ultimate goal of the multi-polar formalization is then to build an electric model of circuit type of *N* coupled tracks to be easily simulated by SPICE type software. The "circuit" model will then include only R, L, C and inductive couplings terms. Having calculated the electrical characteristics of different segments of tracks using the thin wire method, it is necessary to determine the circuit models to use, as well as the parameters of these models to accurately simulate the behavior of printed circuit boards. This process is represented in Figure 6.20.

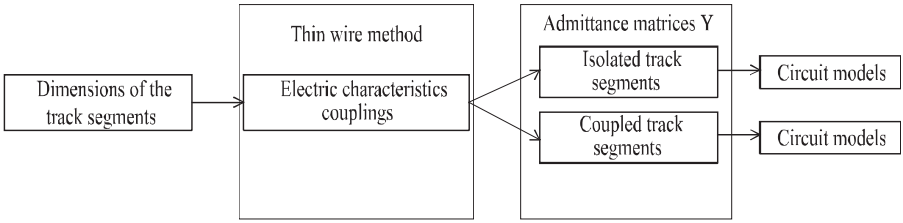


Figure 6.20. *Approach to obtain circuit models*

The parameters of the "circuit" model are determined automatically by an identification software from admittance matrices. In a first phase, the frequency range is shared into three zones, which correspond to different dominant behaviors of the segment of the track (resistive, inductive and with propagation). The model parameters are determined by frequency range where each effect is dominant.

6.3.4.3. *Example of application on the case of two coupled tracks*

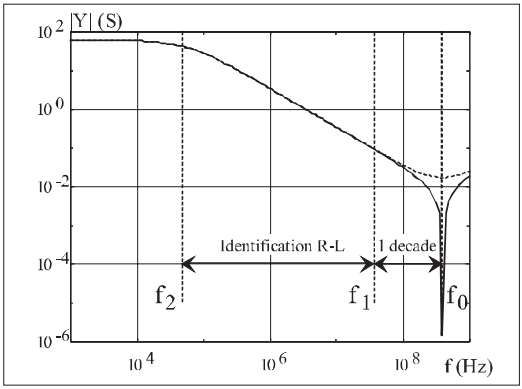


Figure 6.21. *The different areas of frequencies*

In the example below, we present the method of identification of the circuit model. The thin wire method enables us to obtain the admittance matrix [Y] of the system of two coupled tracks. The matrix is size 4 x 4. An example of parameters Y_{ij} is shown in Figure 6.21.

We can see several areas of frequencies in which the behavior of admittances are characteristics:

– $f < f_2$, impedance behavior is resistive;

– $f_2 < f < f_1$, impedance behavior is inductive;

– $f > f_0$, impedance presents a capacitive behavior.

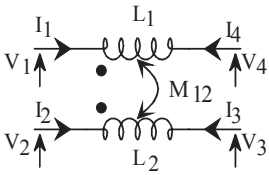
The frequency f_0 corresponds to the resonance of the track. This is the same for all parameters Y of the system and depends only on the length of the track and the permittivity of the environment

$$\left(f_0 = \frac{1}{2\ell \cdot \sqrt{\varepsilon\mu_0}} \right)$$

This is used to identify the different terms of the “circuit” model according the frequency band.

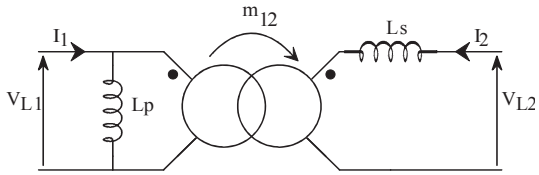
6.3.4.3.1. Inductive coupling

The first step is to represent the inductive coupling between segments of tracks. A simple model is depicted in Figures 6.22 and 6.23 with the corresponding formulations.



$$\begin{cases} V_{L1} = L_1 \dfrac{dI_1}{dt} + M_{12} \dfrac{dI_2}{dt} \\ V_{L2} = M_{12} \dfrac{dI_1}{dt} + L_2 \dfrac{dI_2}{dt} \end{cases}$$

Figure 6.22. *Equivalence between segments of tracks and coupled inductors*



$$L_p = L_1 \qquad L_s = \frac{L_2}{1 + \dfrac{M_{12}^2}{L_1^2}} \qquad m_{12} = \frac{M_{12}}{L_1}$$

Figure 6.23. *Equivalent representation of inductive coupling*

The electrical parameters of the model are then identified under the matrix [Y] (calculated using the thin wire method) using a numerical identification method. It concerns the resistive and inductive terms.

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{12} & Y_{22} \end{bmatrix} \cdot \begin{bmatrix} (V_1 - V_4) \\ (V_2 - V_3) \end{bmatrix}$$

By identification on the domain [f2, f1], we obtain:

$$L_1 \cdot \omega = \frac{Y_{22}}{Y_{11}Y_{22} - Y_{12}^2} \qquad L_2 \cdot \omega = \frac{Y_{11}}{Y_{11}Y_{22} - Y_{12}^2} \; ; \qquad M_{12} \cdot \omega = \frac{-Y_{12}}{Y_{11}Y_{22} - Y_{12}^2}$$

The skin and proximity effects that result in a variation of resistance with frequency are represented by R-L networks, as shown in Figure 76.24.

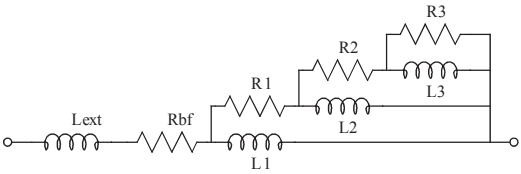


Figure 6.24. *R-L network – equivalent schematic to model the skin effect*

The number of cells depends on the frequency range on which we wish to represent the phenomenon. The parameters of the model are identified using the matrix [Y] for f <f2.

6.3.4.3.2. Multiple capacitive coupling

From capacitive model of tracks represented on Figure 6.25, the second step is to identify capacitances of each segment and capacitive couplings between adjacent segments of track.

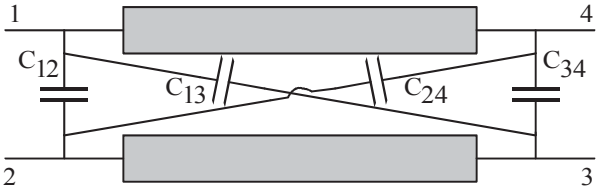


Figure 6.25. *Coupling capacities between two segments of track*

The capacitances are identified using the matrix [Y] calculated by the thin wires method. The following relationships are established for the model of Figure 6.25:

$$\begin{cases} I_{1capa} = (C_{11} + C_{12} + C_{13} + C_{14}) \cdot \frac{dV_1}{dt} - C_{12} \cdot \frac{dV_2}{dt} - C_{13} \cdot \frac{dV_3}{dt} - C_{14} \cdot \frac{dV_4}{dt} \\ I_{2capa} = -C_{12} \cdot \frac{dV_1}{dt} + (C_{12} + C_{22} + C_{23} + C_{24}) \cdot \frac{dV_2}{dt} - C_{23} \cdot \frac{dV_3}{dt} - C_{24} \cdot \frac{dV_4}{dt} \\ I_{3capa} = -C_{13} \cdot \frac{dV_1}{dt} - C_{23} \cdot \frac{dV_2}{dt} + (C_{13} + C_{23} + C_{33} + C_{34}) \cdot \frac{dV_3}{dt} - C_{34} \cdot \frac{dV_4}{dt} \\ I_{4capa} = -C_{14} \cdot \frac{dV_1}{dt} - C_{24} \cdot \frac{dV_2}{dt} - C_{34} \cdot \frac{dV_3}{dt} + (C_{14} + C_{24} + C_{34} + C_{44}) \cdot \frac{dV_4}{dt} \end{cases}$$

The symmetries of the system can reduce the number of independent terms Y_{ij} and therefore the number of capacitances to be determined noting that:

$$\begin{cases} C_{11} = C_{44} \\ C_{22} = C_{33} \\ C_{12} = C_{34} \\ C_{13} = C_{24} \end{cases} \quad \text{and} \quad \begin{cases} Y_{11C} = Y_{44C} = (C_{11} + C_{12} + C_{13} + C_{14}) \cdot s \\ Y_{22C} = Y_{33C} = (C_{12} + C_{22} + C_{23} + C_{13}) \cdot s \\ Y_{12C} = Y_{21C} = Y_{34C} = Y_{43C} = -C_{12} \cdot s \\ Y_{13C} = Y_{31C} = Y_{24C} = Y_{42C} = -C_{13} \cdot s \\ Y_{14C} = Y_{41C} = -C_{14} \cdot s \\ Y_{23C} = Y_{32C} = -C_{23} \cdot s \end{cases}$$

The values of capacitances are identified from the knowledge of the previously calculated inductance matrix and the resonant frequency f_0 of each term Y_{ij}. We can write that:

$$[Y] = [Y_L] + [Y_C]$$

The terms Y_{11}, Y_{22} and Y_{12} have the same anti-resonance frequency, whereas the terms Y_{13}, Y_{14} and Y_{23} have a minimum for this frequency. It follows that, at this particular frequency, capacitances can be determined from the following relationships:

$$Y_{11} = \frac{L_2}{(L_1 L_2 - M_{12}^2) \cdot p} + (C_{11} + C_{12} + C_{13} + C_{14}) \cdot p$$

$$Y_{22} = \frac{L_1}{(L_1 L_2 - M_{12}^2) \cdot p} + (C_{12} + C_{22} + C_{23} + C_{13}) \cdot p$$

$$Y_{12} = \frac{-M_{12}}{(L_1 L_2 - M_{12}^2) \cdot p} - C_{12} \cdot p \qquad Y_{13} = \frac{M_{12}}{(L_1 L_2 - M_{12}^2) \cdot p} - C_{13} \cdot p$$

$$Y_{14} = \frac{-L_2}{(L_1 L_2 - M_{12}^2) \cdot p} - C_{14} \cdot p \qquad Y_{23} = \frac{-L_1}{(L_1 L_2 - M_{12}^2) \cdot p} - C_{23} \cdot p$$

The complete model of the two coupled tracks is shown in Figure 6.26. Its interest lies in the modularity. Indeed, according to the dynamic applied, the model can be very simple and gradually becomes more complex when all the effects must be taken into account.

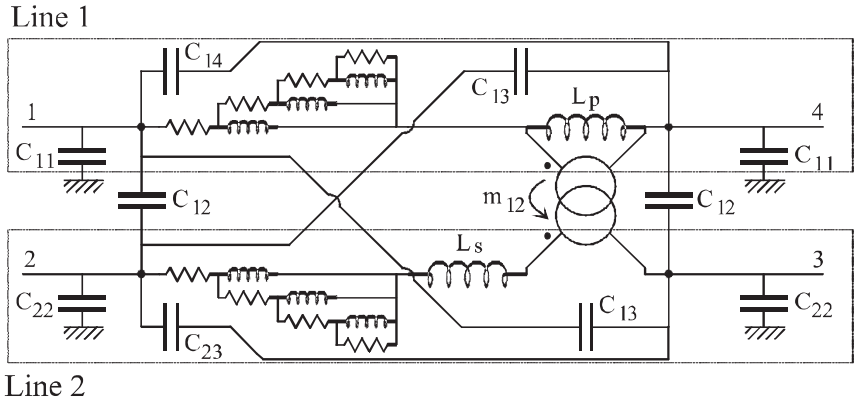


Figure 6.26. *Complete equivalent electrical schematic for two segments of coupled tracks*

However, when the model becomes more complex, the simulating time increases. The method presented for two coupled tracks is generalized to any number of tracks. This generalization is presented in [GAU 00].

6.3.5. *Topological analysis of printed circuit*

The objective of having a CAD tool for the power printed circuit board imposes to automate the tasks to share the design into elementary elements, to verify the existence of couplings between tracks, to identify the parameters of the "circuit" model and finally to make a net list interpretable by the simulator. A software of automatic sharing and analysis of printed circuit is necessary for these tasks. This software must generate, from the geometric description of the tracks on the circuit board, the information necessary for its characterization by the method of thin wires. It also allows the user to specify different levels of modeling for each element obtained during sharing. Finally, it conducts an initial analysis on possible couplings between the various segments of track. Figure 6.27 clarifies this software stage (dotted line) in the overall modeling process.

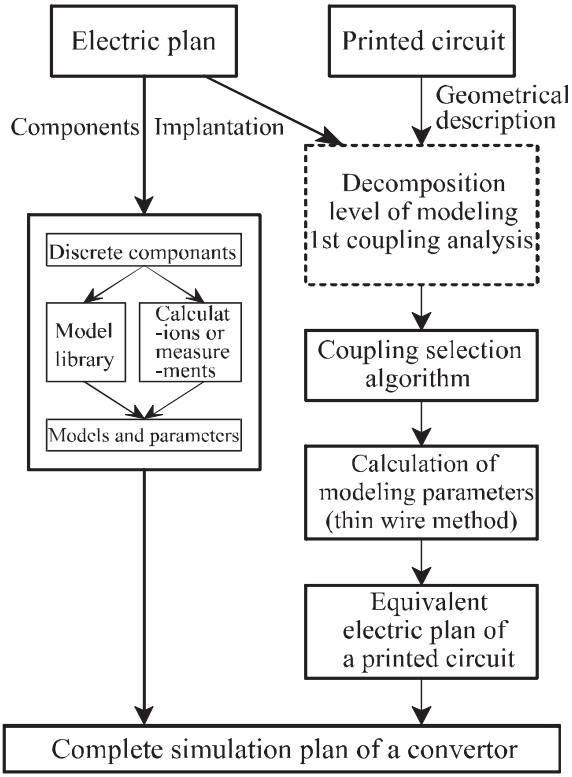


Figure 6.27. *Modeling process*

This algorithm enables the sharing of tracks of a printed circuit for modeling by the thin wire method, as shown in Figure 6.28. The segments of track obtained during the decomposition correspond to the elements of printed circuit board that can be modeled using this method. The nodes correspond to the linking elements between the various segments of track or the junction points with components. The thin track method is not well adapted to model these particular areas which are characterized by low lengths and large surfaces. The geometry of these nodes and parts of linkage with segments of track, however, are fully identified, which allow us to consider their modeling and characterization using a 2D numerical method (finite differences or transmission line matrix) without changing this algorithm. An initial identification of nodes is carried out to allow a simplified characterization (analytical formulations [GAU 00]) in the case of some well-defined configurations.

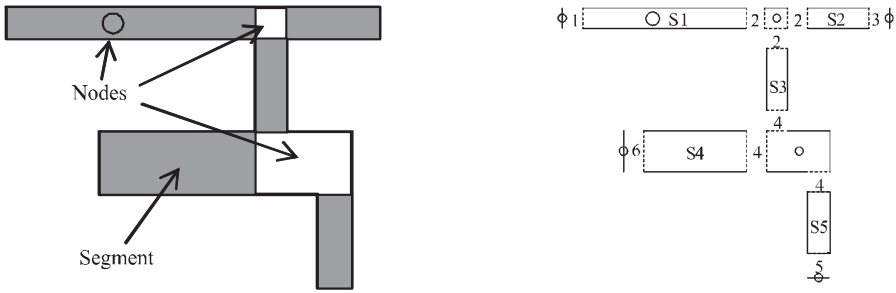


Figure 6.28. *Decomposition of a design in elements treatable by the thin wire method*

Once the stage of decomposition into segments and nodes is completed, the user can perform an initial analysis of the couplings between different segments of track. This analysis allows identifying all segments of track that are parallel with parts face to face (in Figure 6.28 S4 and S1 but not S4 and S2 even if they are parallel). By default, all segments of track are treated in this analysis, but the designer can specify the segments in which we should not use the standard modeling. The determination of significant linkages in turn helps to reduce the total number of linkages to be represented.

Finally, the third and final step is to automatically create a specific library for the printed circuit analyzed, comprising the parameters of models for all segments of track. Using a library can make the link between generic components, used in the electrical diagram, and the degree of complexity of models, as shown in Figure 6.29.

Some generic components have been created under SPICE to model:

– a single track segment (track_1m);

– two coupled track segments (track_2m);

– three coupled track segments (track_3m).

Different libraries are generated automatically depending on the degree of complexity required:

– level 1: R-L model with inductive coupling;

– level 2: R-L-C model with inductive and capacitive coupling;

– level 3: R-L-C model with inductive and capacitive coupling, and skin effect (4 cells).

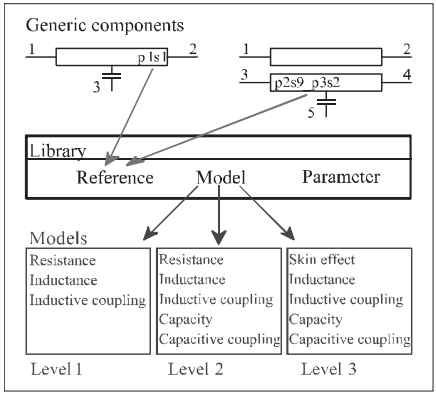


Figure 6.29. *Links between components, models and parameters*

We can consider an extension of this approach to a multi-layer printed circuit: successively applying the previous method to the different layers, which can allow identifying segments of rectangular track. The couplings are treated the same way as for a simple face circuit, parallel segments of track with part face to face are identified during an initial topology analysis.

6.3.6. *Experimental applications*

6.3.6.1. *Analysis of printed wiring*

This section illustrates, using an example, the principles and methods of modeling printed circuit developed here. The device under study is a half bridge of an inverter with MOSFET transistors, powered by 150 V and with switching at 20 kHz. It is represented in Figure 6.30 with its mono-layer printed circuit wiring.

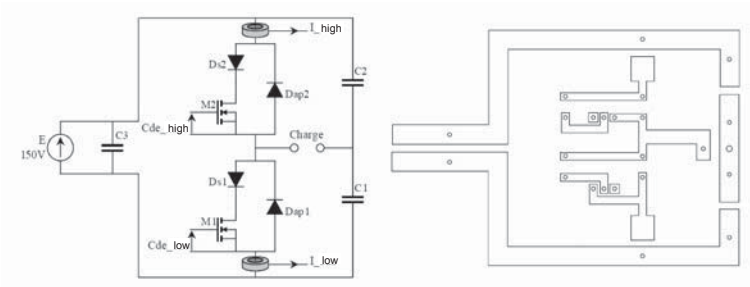


Figure 6.30. *Converter and its printed circuit board*

The analysis of a printed circuit takes place in 5 stages.

	Step	Result
1	Decomposition of printed circuit	All track segments and nodes
2	Study of couplings	list of couplings
3	Calculation of electric characteristics	Admittance matrices Y
4	Calculation of equivalent models	Model parameters
5	Generation of the SPICE library	Library for all elements of the printed circuit board

After applying the method, an impedance measure of the design is performed to validate the simulation. Figure 6.31 presents these results in an indicated wiring configuration.

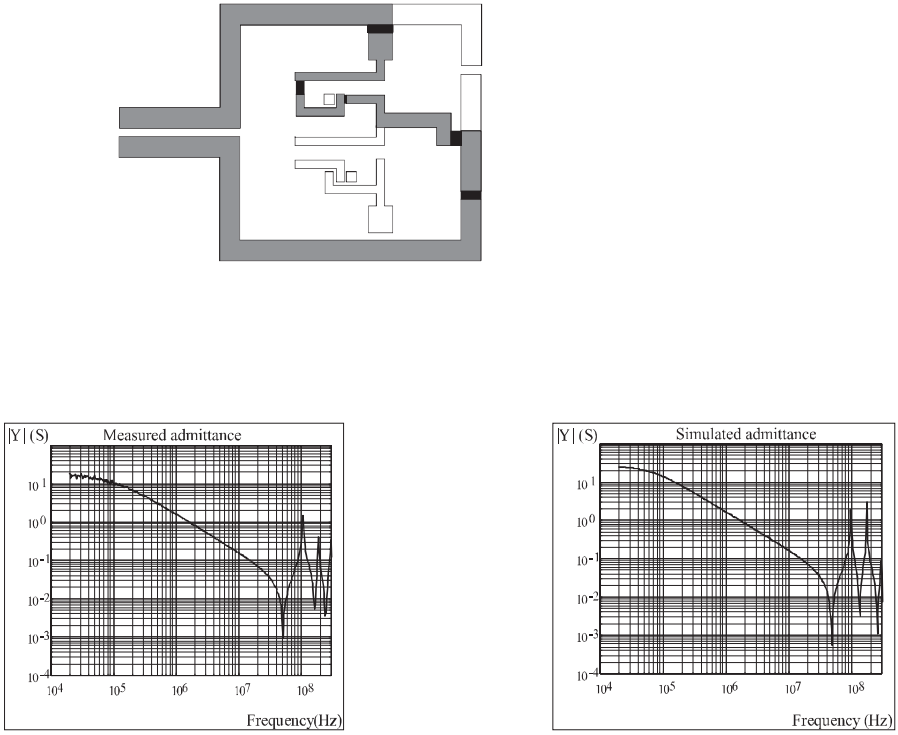


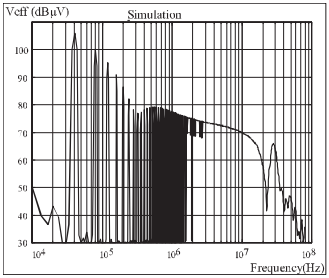
Figure 6.31. *Printed circuit board located 11.5 mm from the ground plane*

You can find a correct representation of the impedance of the circuit up to several hundred MHz. The interest of this analytical method is to easily vary a parameter, for example, the height of a printed circuit compared to the ground plane. The simulation shows in this case a decrease of inductances and an increase in parasitic capacitances with the ground plane. The designer may assume the consequences in terms of EMC (current leakages by common mode capacitance) or operation of converter (voltage surge), compared to a specification. It is thus possible to quickly optimize the wiring using some simulations.

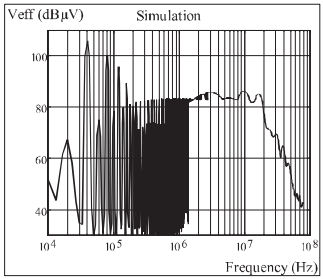
6.3.6.2. *Influence of wiring on conducted disturbances*

Having the complete wiring model, it is then possible to simulate its influence in terms of electromagnetic compatibility by comparing an ideal situation (wiring with no impedance) and the actual situation induced by different types of wiring. The study was conducted in Figure 6.32 where the influence of printed wiring is represented on the spectrum of conducted disturbances. These are measured on the Line Impedance Stabilizer Network (LISN) connected at the input of the converter. The simulation reproduces the measurement configuration.

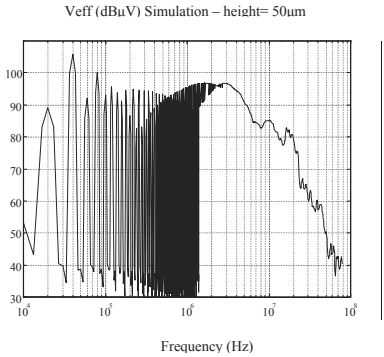
In the simulation corresponding to Figure 6.32a, only the imperfections of semiconductors and passive components were taken into account. In Figure 6.32b the wiring model was added. It is located 11.5 mm above the ground plane, a classic value for printed circuit boards. The case of Figure 6.32c corresponds to a type of IMS wiring where the height compared to the ground plane is 50 µm. There is a marked increase over the ideal case and over the case of a printed circuit board. The comparison of simulations clearly shows the influence of wiring on the electromagnetic signature of the converter. It is dominant in the range of 1-30 MHz and already sensitive a decade before. Finally, Figure 6.33 presents measurements on the actual converter in the configuration of simulation b. There is a good fit with the simulation results, which validate the methodology. We should note that, according to the level of detail used for simulation, the time to calculate can be long, especially if we introduce skin effect models and multiple couplings. Also, in a CAD oriented simulation, the time to calculate can be long, especially if we introduce skin effect models and multiple linkages. Also, in a CAD oriented simulation, the designer must begin the simulation by using low-level models to determine the weight of any particular parameter on EMC or electrical performance of his device. The complex model is then reserved for the final stage of the calculation.



a) ideal wiring, real components



b) height in relation to ground plane: 11.5 mm



c) height in relation to ground plane: 50 µm

Figure 6.32. *Study of the influence of wiring on the spectrum of conducted disturbances by simulation*

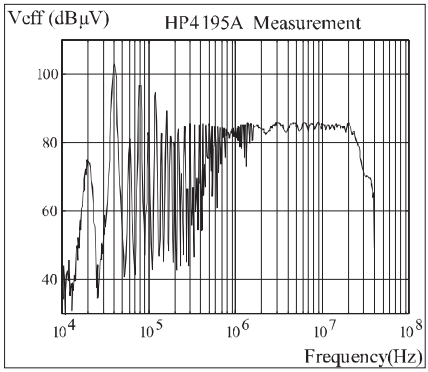


Figure 6.33. *Spectrum of conducted disturbances*

6.3.7. *Conclusion on the simulation of printed circuit*

These sections have shown that the printed wiring used for power electronics, whether traditional (epoxy) or on substrates of IMS type or DCB type for hybrid modules, can be simulated with a satisfactory accuracy and calculation time for a CAD design by a mono-dimensional transmission line method.

All types of printed conductors (multi-layer, variable width, etc.) can be simulated using this method with a sufficient accuracy up to 100 MHz. Some configurations, however, require a 2D modeling, this work is currently underway.

6.4. Towards a better understanding of massive interconnections

In this chapter, we will try to show some examples of power interconnection with their own specificities. We will focus in this section on the design of interconnections according to the criteria of power electronics, that we have already highlighted in the previous sections. Of course, these models can then be completed for EMC. Our intention here is to give examples that can be used in a certain way as guide lines for design. Of course, some proposed solutions are not necessarily original, and have already been developed by engineers of strong powers in the field of induction heating. We will try to illustrate the particularities of each family of interconnections showing orders of magnitude to be expected, and the simplifying assumptions that can be made according to the specificity of each and according to the accuracy that is expected. This accuracy is not always easy to determine, as we will show in section 6.5.

The interconnections in power electronics, except bonding, are mostly and quite exclusively, made of rectangular cross-section conductors. In the same way, but less systematically, conductors are parallel to each other or perpendicular, which greatly simplifies the representation of models of a complete structure (zero coupling between perpendicular conductors). Thus, first studies of quite general scope can be made, and only after this will we see the impact of the specificities of each type of interconnection according the geometrical dimensions and geometrical shapes encountered.

6.4.1. *General considerations*

In this section, we first of all want to illustrate the general trends regarding the evolution of the inductive impact of conductors, based on their geometric dimensions. Most connections used (printed circuit board, IMS, bus bars, massive

bars, etc.) have rectangular cross-sections that make possible to apply the following general trends.

6.4.1.1. *Change in partial inductance depending on the geometry of the straight section of the conductor*

Figure 6.34 highlights the change in inductive impact of a conductor according to its section. In this example, the length of the conductor is 50 cm and the cross-section of the conductor is changed, taking as constant the surface equal to 4 cm^2.

It should be noted that more the conductor is thin and large, the less inductive it is. This makes it very obvious which geometric shape of sections must be chosen to minimize the inductance of a path. The square section gives an idea of the inductance of a round wire whose transverse section is an equivalent surface.

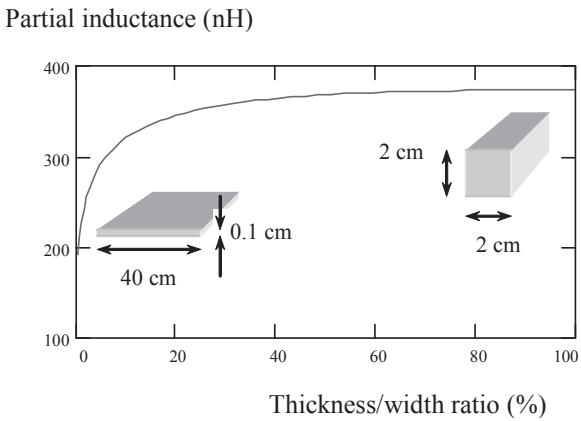


Figure 6.34. *Evolution of the partial inductance with the geometry of the section*

6.4.1.2. *Change in partial inductance depending on the surface of the straight section of the conductor*

The second concept that is as important as the previous one is to have an idea of the change of partial inductance of a conductor depending on the surface of its cross-section.

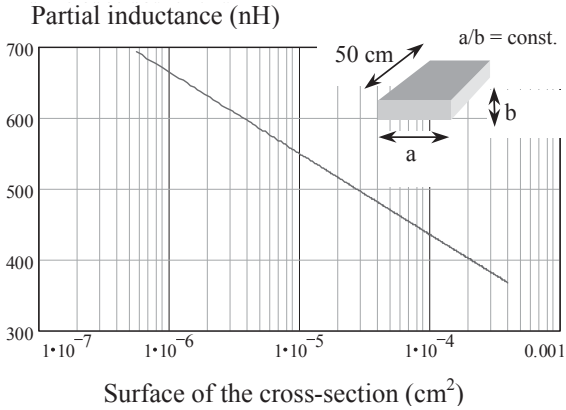


Figure 6.35. *Evolution of the partial inductance depending on the surface of the cross-section keeping constant ratio width over thickness*

Even if the first criterion for choosing a cross-section is thermal, the chart contained in Figure 6.35 shows that the partial inductance of a conductor is very much reduced when the amount of copper used increases.

More specifically, we can observe on the curve in Figure 6.35 that the evolution is linear if a logarithmic scale is used for the surface value. It may be recalled that the expression of the partial inductance shows on denominator the surface of the conductor. It is therefore normal to find this type of variation. The user can then easily extrapolate the curve to solve his problem.

6.4.1.3. *Change in partial inductance depending on the length and section of conductor*

In the following illustration, we want to overcome stereotypes which consider it is sufficient to say that one meter of conductor has an inductance of 1 μH (order of magnitude is however useful in some simple cases). Given the expected performance of interconnections in power electronics (often less than 100 nH), there was no question of use of such magnitudes, legitimate only in the case of wiring several tens of meters separating electrical assemblies. We take this opportunity to recall that the partial inductance is not a linear concept and that, therefore, inductance of a 2 meter conductor is not twice the inductance of one meter. The partial inductance takes into account the fact that the length of the conductor is finite and this concept does not, therefore, makes the assumption of TEM mode (transverse electro-magnetic field).

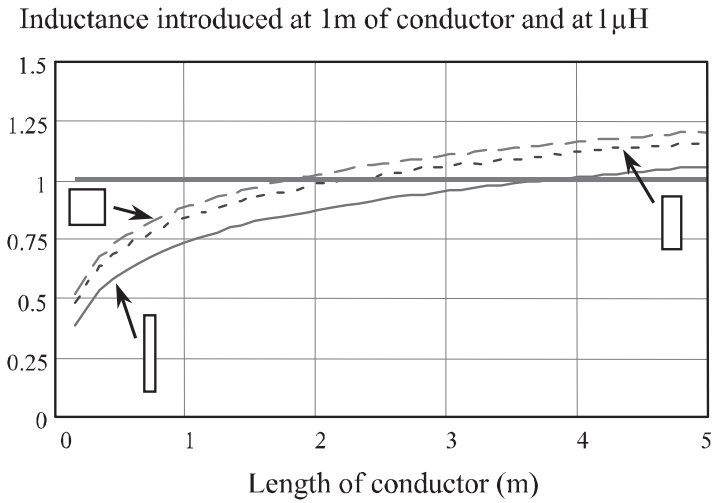


Figure 6.36. *Dependency of inductance of a conductor with the length and the section*

The graph in Figure 6.36 shows this considering conductors whose cross-sections are different (from the flatter to the extreme case of a square or cylindrical conductor). The partial inductance of a conductor has been calculated taking into account its length, then divided by its length to obtain a per unit length value. This result was then compared to 1 μH to show errors that can be made with this kind of approximation.

As for longitudinal dimensions of less than 3 m, the "magic" value of designers of 1 μH/m overstates the inductance, while for dimensions greater than 3 m, it underestimates. Moreover, this distance depends on the section of conductors. The thinner and wider this section, the more this changeover distance increases.

6.4.1.4. *Change in partial inductance depending on the frequency*

Traditionally, we consider that the inductance of a circuit can be broken into two parts. One is the magnetic energy contained in the volume of the conductor. This is called internal inductance and depends on its geometry. The other part is called external inductance, which is defined by the flow embraced by the current loop. It depends on the shape of the loop but also that of conductors. The total inductance of a circuit is the sum of these two inductances. In high frequency, current tends to spread to the periphery of the conductor (skin effect); internal inductance therefore tends to zero when the frequency tends towards infinity.

We can illustrate these remarks by the school case which consists of a cylindrical wire infinitely long with radius a. The internal low-frequency inductance expressed per unit of length is: $\frac{Li}{l} = \frac{\mu_o}{8 \cdot \pi}$.

For any wire, whatever its diameter, this is a low frequency internal inductance of 50 nH/m.

High frequency redistribution of current in the conductor is performed with the same cylindrical symmetry as with low frequency (Figure 6.37), if the conductor is not subject to any external influence; external inductance of the circuit made by cylindrical conductors does not vary.

Figure 6.37. *Current density of a cylindrical conductor far away from other conductor:. a) low frequency; b) high frequency*

In cases where another wire (back of the loop for example) is considered close to the conductor, high frequency redistribution of current looses its symmetry and external inductor is amended (Figure 6.38).

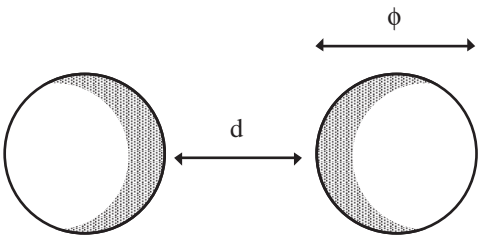


Figure 6.38. *Current density of a cylindrical conductor: influence of the back conductor in high frequency (d of same order of magnitude than Φ)*

Figure 6.39 shows in the case of a loop of rectangular shape (perimeter 50 cm) made of round wire that the change of inductance with frequency is indeed 50 nH/m, because there is no significant proximity effect (10 cm - 15 cm) between conductors.

Where two conductors of the loop are close (24.5 cm - 0.5 cm), the decrease of inductance with frequency is higher.

The external inductor has therefore been amended by the presence of the return conductor.

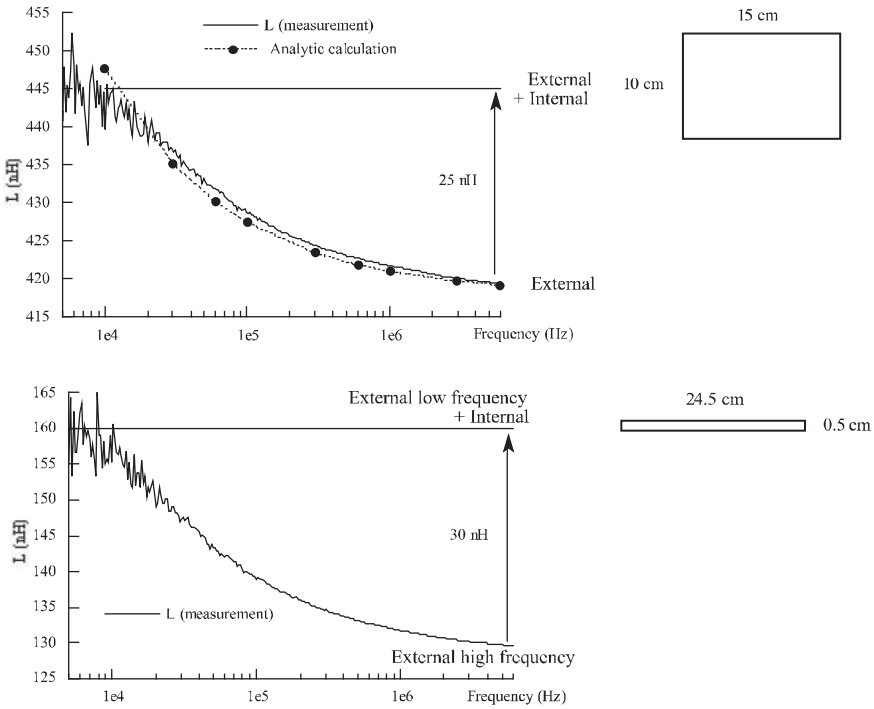


Figure 6.39. *Change of internal and external inductances depending on the frequency*

For conductors of rectangular section, internal inductance becomes negligible if one dimension is very low compared to the other, as shown in Table 6.2. The variation of inductance with frequency in the case of thin ribbons (printed circuit or plates) must therefore be attributed to the external inductance.

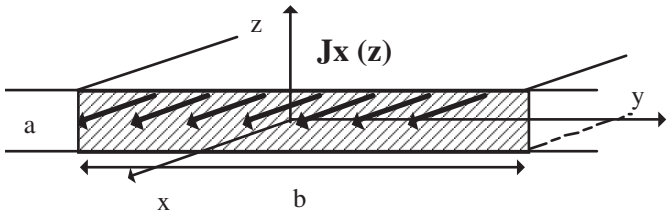


Figure 6.40. *Flat current in a conductor of very low thickness*

a (mm)	b (mm)	a/b	R (mΩ/m) 1 MHz	Li (nH/m) 1 Hz	Li (nH/m) 1 MHz
0.0035	12.5	0.0028	61.2	0.6	0.6
0.0661	6.61	0.0100	63.4	2.0	2.0
0.15	2.9	0.0520	74.6	9.3	7.1
0.21	2.1	0.1000	86.6	16.3	10.4
0.33	1.32	0.2500	111.5	31.0	14.2
0.47	0.94	0.5000	123.4	43.0	15.7
0.66	0.66	1.0000	128.4	48.3	16.3
r = 0.373		–	120.8	50.0	17.5

Table 6.2. *Simulations with "finite elements" for a constant surface ab (R low frequency = 39 mΩ). Also case of wire with given radius r*

It is interesting to note that for the printed circuit board traditionally used in power electronics, 210 µm thick, where it is common to encounter tracks of 1 cm wide, the value of the internal inductance will be lower than 4.4 nH/m. For power boards, where the total length of connections does not exceed 20 cm, internal inductance does not exceed the nanohenry. The wires of circular or square sections have a neighbor behavior.

6.4.2. *The printed circuit board or the isolated metal substrate (IMS)*

The effect of a ground plane located below a track is well known to reduce the inductance of a loop of electrical circuit, whether the plane is electrically connected or not to the rest of the assembly.

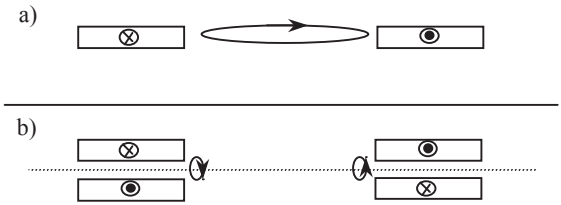


Figure 6.41. *Change of the inductance of a loop by introducing a ground plane*

Indeed, if we consider a loop (Figure 6.41a), composed of a conductor and return back, the embraced surface can therefore become consistent, inductance that results is therefore high. Now (Figure 6.41b), put a ground plane below the conductors. The theorem of images leads us to replace the ground plane by a loop travelled by the same currents in the opposite direction. Soon, it appears that there are compensation flows between a conductor and its image. This way, there is no longer a big loop which radiates but two extremely flat loops (twice the spacing between the conductor and the ground plane), which constitute inductance of the original loop. It is therefore easy to see that the inductance is greatly reduced (Figure 6.42).

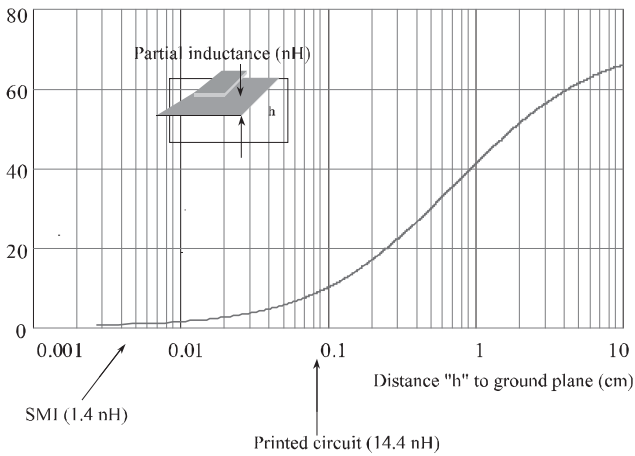


Figure 6.42. *Increase of partial inductance of a conductor with the remoteness of the ground plane*

In terms of application in power electronics, the IMS uses this feature perfectly which leads us to obtain tracks whose partial inductance rarely exceeds 10 nH. The

voltage surge at the opening of semiconductor components are therefore not to be feared with this type of technology, provided the appropriate packages are used.

6.4.3. *Massive conductors*

In the applications of very high power (more than a few megawatts), or more exactly when the current reaches very large values (more than 1,000 Amps), connections with massive conductors are used. It is necessary to be able to connect in parallel converters, and several constraints of mechanical congestion lead us to use such interconnections. It is faster and more convenient to make the connection between two pieces using massive conductors than studying a bus bar which has to answer very specific criteria for partial discharge, etc. This method of connection is widely used in power electronics at industrial frequency (bridge rectifiers for electrolysis, manufacture of aluminum, etc.) or simply in electrical engineering (bars for transformer supply, etc.). In these cases, the intrinsic value of loop inductance is not important but the perfect knowledge of inductance wiring is predominant in the correct distribution of currents between devices in parallel.

The way to reduce inductance of the loop is to maximize face to face surfaces and increase the conductor section (Figure 6.43). However, we must be aware that we cannot change this inductance significantly.

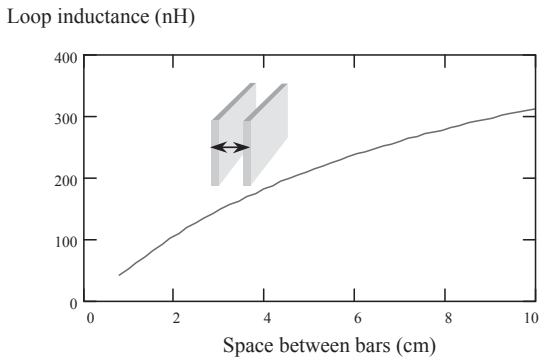


Figure 6.43. *Evolution of the partial inductance of a loop made of go and return massive conductors, depending on their distance*

6.4.4. *Bus bars*

The bus bars are sandwiches of copper and insulating materials pressed and glued. The extreme proximity of conductors increases the partial mutual inductance

which comes to subtract the partial inductance of each bar. This explains perfectly how we can obtain through this process little inductive wiring.

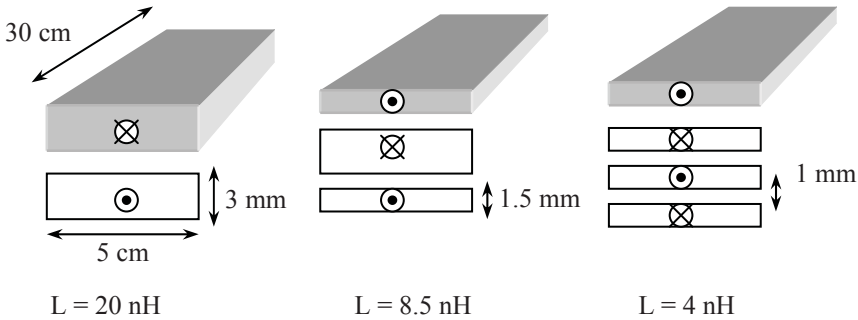


Figure 6.44. *Some ideas to win more nH! (at constant copper volume)*

Nevertheless, the idea to compensate the magnetic flux created in copper at the closest by interspersing plates of way and return flow, as shown in Figure 6.44, shows that it is possible to earn a few nanohenrys but this stacking increases slightly the sizes of the device and especially leads to a much more expensive component. It should be noted that the dielectric layers are all of the same thickness and that the current densities are the same in all conductors.

The weakness of the bus bars lies in the problems of partial discharges which often take place in the corners that can present this type of interconnection.

6.5. Experimental validations

The more frequent use of modeling as an "*a priori*" design tool, requires many validations on realistic configurations. In the case where the device exists, it is sometimes possible to make characterizations of interconnections in the actual operating configuration of the device or, at least, in a configuration extremely close. However, in general, the measure of interconnections remains delicate, mainly because the measured values are, fortunately, particularly low. It is not always easy to close the loop to be measured by a foreign connection to the device and with less impedance than it.

Two large families of measurements are possible in a practical way to achieve the evaluation of interconnections [CLA 96]. The offline measures, themselves separated into several categories, are:

– Measures of impedances with specific devices (impedance measurement bridge for example). This technique is interesting because it gives the value of the impedance according to the frequency. In order to form a loop, the connection under test may be closed either by a short circuit (not always easy to achieve and sometimes with significant impedance) or by decoupling capacitors, which themselves, if they can be exactly of the same value, exist in the final assembly.

– Measures by reflectometry (time or frequency), for example, vector analyzers or temporal reflectometry (TdR). The main drawback of these methods is the low accuracy when the impedance to be measured is far away form characteristic impedance of measuring apparatus (50 Ω most often). As a result, very low impedances due to the connections will not be determined with precision, except at very high frequency. Now, this is the inductive behavior, visible at rather low frequency, which is important for a power electronics designer (forecast of voltage surges).

– Measures by resonance: either with the decoupling capacitors used in the application or possibly with others. We must of course know exactly their values. It determines the tuning frequency of the system (actual impedance at that frequency), which leads to the value of inductance sought.

– Measures making the ratio V/(di/dt). In an "off line" approach, di/dt is injected by an external generator. Note that it is sometimes possible to move the voltage sensor throughout the connection to assess the inductive contribution of each piece. Take care at this stage that the voltage which is measured is expressed by $V = L\frac{di}{dt} + \sum_{i \neq j}^{j} M_{ij}\frac{di_j}{dt}$. Thus, in the general case, we will not have access to the value of inductance unless we can effectively ignore the mutual couplings Mij.

– "Online" measures, fairly close to the actual operating conditions of the device or even in operation, can also be used.

The ratio V/(di/dt), during commutation, can of course give useful information on inductances, concerning mutual inductances some precautions can be taken as previously said. One of the important applications is the determination of housing inductance of a controlled IGBT-type semiconductor.

We can also think of an oscillatory discharge. Decoupling capacitors are charged generally under a reduced voltage and the short circuit is realized using the semiconductors of the power structure. Given the orders of magnitude, it is not always easy to obtain an oscillating wave discharge which remains easy to identify.

The identification results are not always very accurate and can present an error by the fact that the short circuit created by semiconductors is not instantaneous.

The necessary conclusion is that none of these measures is really better than the others. Our preference is still for measures on impedances bridge which has the advantage of allowing a display of the impedance depending on the frequency. In addition, some of the mistakes are more easily quantifiable in terms of abacuses provided by the manufacturer. The only large inaccuracies are due to the possible short circuits used to close the loop.

Figure 6.45 shows the comparison between model and measurement, on inductance between the emitter and collector of an IGBT in its package. This validation of the overall modeling of inductive package confirms the interest of the approach.

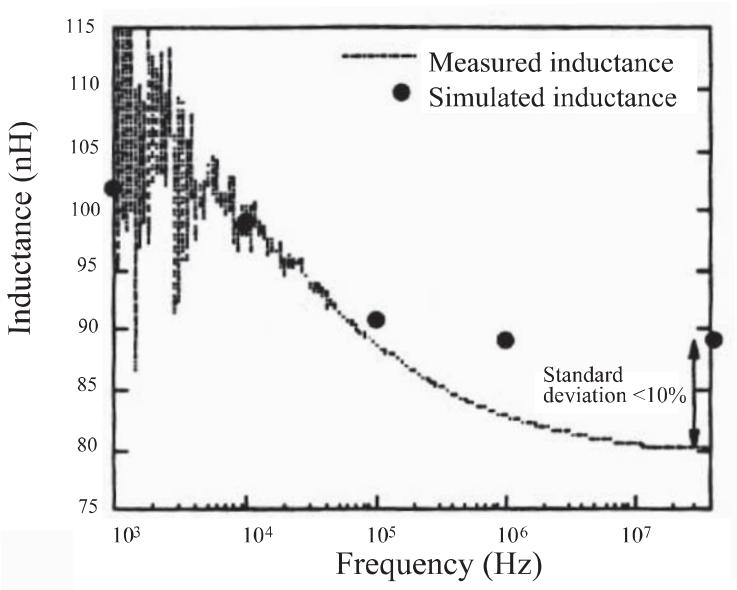


Figure 6.45. *Comparison simulation – measure on an IGBT package (old generation)*

For more complex connections requiring a 2D approach, the example of Figure 6.46 is that of a three-phase UPS installed to supply AC machines. In addition to InCa3D modeling, we conducted several measurements using different methods that we summarized in Table 6.4. It may be noted that it is also necessary to model any piece belonging to the switching cell which is also involved in the measurement. In particular, it was necessary to characterize internal inductances of semiconductor packages. The measurement does not allow us to differentiate the

inductive importance of the bus bar in the total loop. We had to remove the simulation results of the package from the measure to obtain the results presented.

	Resonance	Short circuit Impedance bridge	Oscillating Discharge	Simulation
Inductance	20.5 nH	13.5 nH	9 nH	9 nH

Table 6.3. *Values of inductance of the commutation cell: measures and simulation*

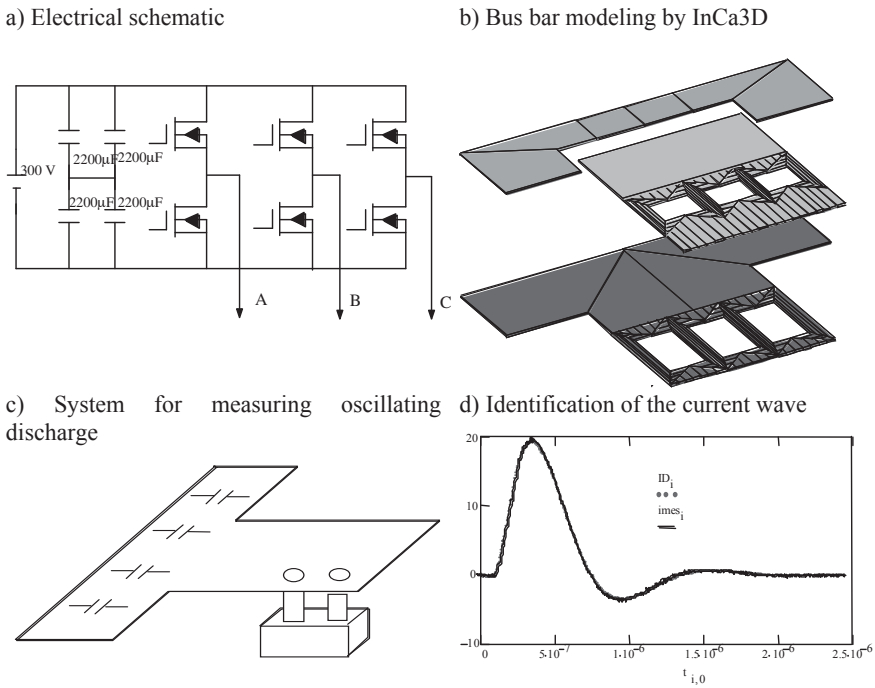


Figure 6.46. *Example of measurement for characterization of a bus bar*

As a conclusion, we can see that there is already a great dispersion of results depending on methods of measurement and it would be very hasty to conclude that oscillatory discharge is the best method because it gives the nearest result from simulation, itself subject to errors.

6.6. Using these models

In this section, we will show how to use electrical equivalent schematics provided by modeling. Indeed, it is possible to obtain global values and/or local values according to the post-treatment involved. Of course, depending on the studied structure, the analyses will be more or less easy and will lead to more or less data processing.

6.6.1. *Determination of equivalent impedance*

As modeling provides an electrical equivalent schematic including localized constants made of resistances, inductances and mutual inductances, then it is logical to try to reduce this figure to determine the impedance of all or part of the structure. This impedance then serves to make a study of waveforms of the power electronics structure. However sometimes the complexity of the structure is such that one impedance is not enough to show all the connections of the device. The scale model is then more complicated and we will see in the following section that the calculation methods are not the same as for the simple case of a single impedance (section 6.5.1.1).

6.6.1.1. *Between two points*

In this section, we will give two examples illustrating the approach to determine the impedance of the commutation loop. The 1D assumption was used in the first instance and the 2D assumption for the second (for the connections grid).

Here is a brief recap of the different steps of the approach [CLA 97]:

1. entering the geometry of the device from plans by the graphic pre-processor InCa3D;

2. evaluation with InCa3D of all parasitic elements, inductances and mutual couplings;

3. post-treatment with InCa3D to possibly reduce the equivalent electrical diagram;

4. simulation of the electric model thus obtained. The system which now needs to be simulated is of reasonable complexity (at least the switching cell composed of a voltage source, an inductance, a diode and a switch). We can of course simulate more complex systems that are more complete and thus allow any change in geometry.

6.6.1.1.1. First example

The first example that we present is modeling a switching cell in the form of a Power Block package.

Figure 6.47 shows the modeling process of the switch function:

– capture of geometry (Figure 6.47c);

– modeling with an electrical equivalent schematic with localized constants (Figure 6.47d). Here, as conductors are mostly linear and, more important, as it is possible to make assumptions on the path of current lines, a 1D mesh was adopted;

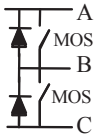
– – reducing the electrical equivalent circuit given by PEEC modeling. This is to determine the equivalent impedance from two points of the switching cell (Figure 6.47e). Note that this impedance results in the serial and parallel combination of different portions which, remember, are all linked to each other, which requires some developments of matrix calculus [ROU 94] and the introduction of the frequency;

– simulation and obtaining global waveforms of module (Figure 6.47f). In the final simulation schematic, mesh inductance includes therefore the case that we just evaluated through InCa3D, the inductance of voltage source (decoupling capacitors) and the one of the bus bar between the capacitors and the Power Block.

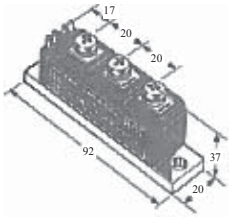
6.6.1.1.2. Second example

Now let us take a much more complex example in the form of an interconnection bus bar with a large and flat geometry, which needs to make a 2D mesh (Figure 6.48) as described in section 6.3.2. As a result of the InCa3D modeling, a network of resistors and inductances are all coupled, but difficult to use directly by the power electronics engineer.

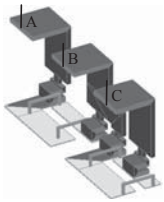
a) Electric function of the studied Power Block



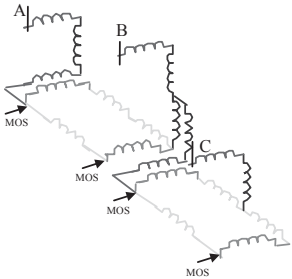
b) External aspect of the Power Block



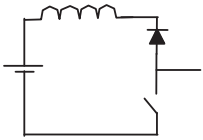
c) Geometry of internal connexions described on InCa3D



d) Electric schematic from modeling on InCa3D (all are coupled inductors)



e) Generic diagram for simulation



f) Accurate simulation obtained from accurate model of connection and component: opening a MOSFET

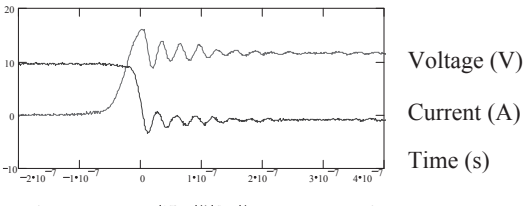


Figure 6.47. *Approach for extracting a cell switching: from capture of geometry to simulation*

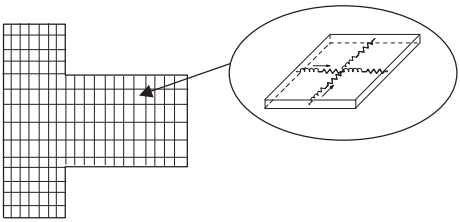


Figure 6.48. *2D mesh of plates of the bus bar*

The application of a network theory is not justified in this example. We are looking only for the impedance between two points, input and output, of the bus bar.

A simple harmonic analysis with SPICE, for example (Figure 6.48), gives the evolution of the electrical characteristics of the bus bar depending on the frequency (Figure 6.49).

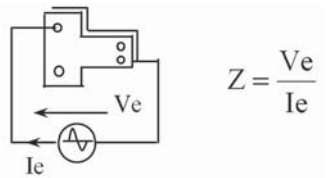


Figure 6.49. *Impedance of bus bar depending on the frequency*

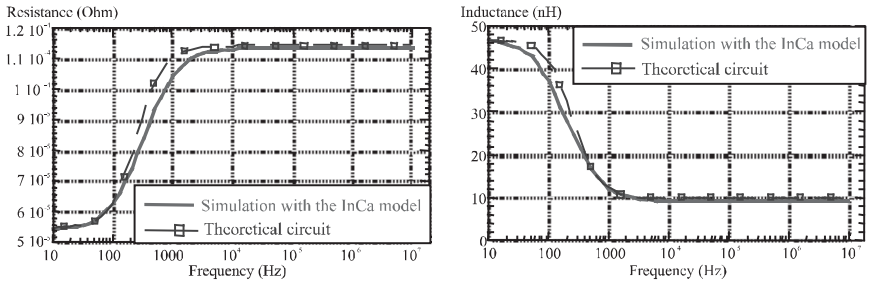


Figure 6.50. *Frequency characteristics by using a SPICE simulation, device measurement*

More specifically, Figure 6.50 shows the evolution of resistance and inductance depending on the frequency. These values are only valid for a limited range of frequencies, in agreement with the spatial meshing of the bus bar (Figure 6.48). This phenomenon appears especially on the resistance whose value reached a limit around 10 kHz, while in practice it continues to grow with frequency. Variations of inductance are much smaller amplitudes, which does not allow us to distinguish the limit of correct digitization, and enables us to accept good values of inductance obtained for frequencies above 10 kHz.

From these impedance curves, it is possible to deduce a simplified electrical equivalent circuit involving only two resistances and two non-coupled inductances (Figure 6.51). Clearly, it is easier to make a temporal simulation with this last model than with the one obtained by InCa3D simulation which contains several hundred coupled LR series circuits. A finer model, but also more costly in simulation time, can be made by adding parallel LR cells in series.

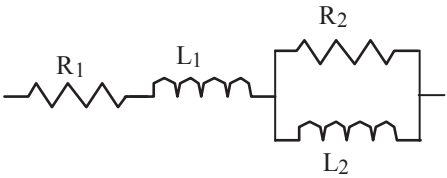


Figure 6.51. *Simplified electrical equivalent schematic whose characteristics are independent of the frequency*

In the case of 2D modeled structures, post-treatment can be very long and costly in terms of memory space, because the electrical pattern that has to be reduced to a simple impedance can be very dense.

In many cases, a power electronics designer will be tempted to use an approach to solving circuit equations based on the method of potential nodes, as proposed by the SPICE software. However, the latter is not well suited to many inductors, and analysis of the circuit related to the current is better suited as we will show in what follows.

6.6.1.1.3. Analysis of electrical circuit [PIE 99]

After applying the PEEC method, we obtain a matrix system $\mathbf{U} = \mathbf{Z} \cdot \mathbf{I}$ which dimension equals the number of subdivisions. At the end of this circuit analysis a reduced relationship $u = z \cdot i$ must be obtained, where z is the equivalent impedance between two points of the structure, which will allow us to study the overall behavior of the system.

We have chosen a systematic topological analysis, which uses Kirchhoff's laws (law of nodes and law of mesh). These laws do not depend on the type of components (active or passive, linear or non-linear), but only on the directed graph of the circuit. For example, Figure 6.52 shows an electric circuit and its associated graph.

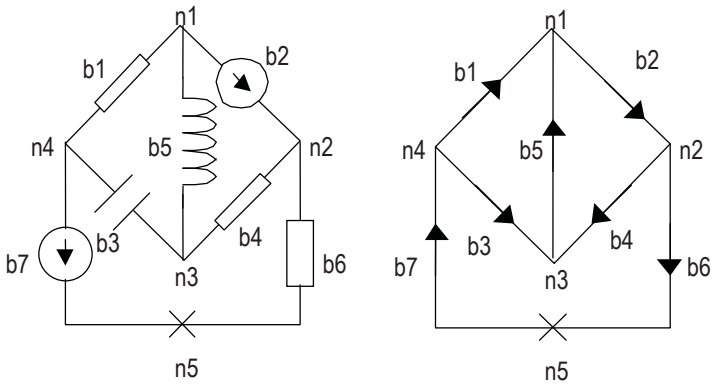


Figure 6.52. *Electrical circuit and its associated graph*

The electrical circuit is composed of 7 components that are represented in the associated graph with directed segments. The points of connections, 5 on this example, which are terminals of components, are topological nodes. Oriented segments in the direction of reference are called branches.

The mesh concept is also defined. It is a closed loop, oriented in a reference direction, which follows the branches, such a way the branches are travelled at least once. For our example, there are 6 meshes as we can see in Figure 6.53. However, it appears that these meshes are redundant and do not form an independent system. It will therefore be required to find the number of independent meshes for describing the system.

Broadly speaking, if we consider the graph of an electrical circuit with b branches and n nodes, the system of independent integral and differential equations for the calculation of voltages and currents in components includes $n - 1$ equations for nodes and $b - n + 1$ equations for meshes. It should be noted that the number of branches b is greater than the number n of nodes, which may be a factor in the choice of the calculation algorithm.

In the previous case, we must find 3 independent meshes (because b = 7 and n = 5). For the following development, our independent 3 will be meshes m1, m2 and m3.

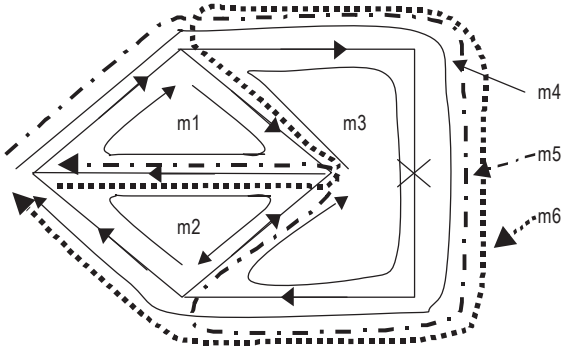


Figure 6.53. *Electrical meshes*

To implement the system of equations to be solved, several well-known values must be introduced. The incidence matrix N, also called the nodes to branches matrix, is defined as follows:

$$\mathbf{N} = \begin{bmatrix} \alpha_{11} & \alpha_{12} & \cdots & \alpha_{1b} \\ \alpha_{21} & \alpha_{22} & \cdots & \alpha_{2b} \\ \vdots & \vdots & \ddots & \vdots \\ \alpha_{n1} & \alpha_{n2} & \cdots & \alpha_{nb} \end{bmatrix} \quad avec \quad \alpha_{ij} = \begin{cases} 1 & \text{, if branch j leaves node i} \\ -1 & \text{, if branch j arrives at node i} \\ 0 & \text{, if branch j is not connected to node i} \end{cases}$$

With this matrix N, we can write the law of nodes: $\mathbf{N} \cdot \mathbf{I} = \mathbf{0}$, with I the vector of branch current, with dimension b.

Matrix N is not regular. To transform it, we need to delete a line and we obtain the reduced incidence matrix N' which is regular. This operation corresponds to the choice of a reference node.

We can always write the relationship: $\mathbf{N}' \cdot \mathbf{I} = \mathbf{0}$

Consider the matrix $\mathbf{M} = \begin{bmatrix} \beta_{11} & \beta_{12} & \cdots & \beta_{1b} \\ \beta_{21} & \beta_{22} & \cdots & \beta_{2b} \\ \vdots & \vdots & \ddots & \vdots \\ \beta_{m1} & \beta_{m2} & \cdots & \beta_{mb} \end{bmatrix}$, with m = b – n +1

and:

$$\beta_{ij} = \left| \begin{array}{l} 1 \quad \text{, if branch j belongs to mesh i and they are oriented in the same direction} \\ -1 \quad \text{, if branch j belongs to mesh i and they are oriented in the opposite direction} \\ 0 \quad \text{, if branch j does not belong to mesh i} \end{array} \right.$$

The matrix M will be called in the following matrix mesh-branch.

We can write the mesh law: $\mathbf{M} \cdot \mathbf{U} = \mathbf{0}$ with U the vector of branch voltages of dimension b.

In the above presentation, we have ignored the components of the circuit. We will take them into account in expressing Ohm's law on each branch. Two dual methods exist.

The branch currents are a function of branch voltages. In systems that we describe, it is always possible to write Ohm's Law:

$$\mathbf{I} = \mathbf{Y} \cdot \mathbf{U}$$

with:

– I: branch currents vector;

– U: branch voltages vector;

– Y: admittances matrix related to the branches.

Vectors I and U are not completely composed of unknown variables. Some ii and uj may be determined by the structure: they are current and voltage sources. In this approach, the unknown is vector U. The current sources will be isolated in a vector I_g. The previous law becomes:

$$\mathbf{I} = \mathbf{Y} \cdot \mathbf{U} + \mathbf{I_g}$$

with I_g the vector of current generators.

To illustrate this, we take the example of Figure 6.53 and we assume that the generators are current generators. Then we have the following terms:

$$\mathbf{I_g} = \begin{bmatrix} 0 & I_1 & 0 & 0 & 0 & 0 & I_2 \end{bmatrix}^t$$

and:

$$\mathbf{Y} = \begin{bmatrix} \frac{1}{R_1} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & jC\omega & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{R_2} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{jL\omega} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{R_3} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

The branch voltages are a function of branch currents.

For this approach, we express Ohm's Law $\mathbf{U} = \mathbf{Z} \cdot \mathbf{I}$, with:

– U: vector of voltage branches;

– I: vector of current branches;

– Z: impedance matrix relative to each branch.

As in the previous case, there may be voltage and current sources.

The unknown here is the current vector I. The voltage sources are encountered in the vector U_g.

We obtain: $\mathbf{U} = \mathbf{Z} \cdot \mathbf{I} + \mathbf{U}_g$

with U_g the vector of voltage generators.

This time, we assume that the generators are voltage generators. Then we have the following terms:

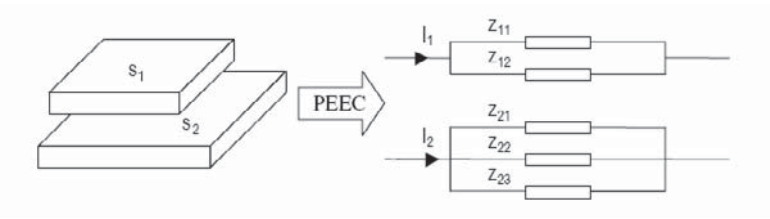
$$\mathbf{U}_g = \begin{bmatrix} 0 & E_1 & 0 & 0 & 0 & 0 & E_2 \end{bmatrix}^t$$

and:

$$\mathbf{Z} = \begin{bmatrix} R_1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{jC\omega} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & R_2 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & jL\omega & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & R_3 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}$$

Once the different values are defined, we will explain later the impact of the two previous approaches. We will explain the reasons of our choice.

To show the principle of the two methods, we will take a simple example: 2 straight bars, which we model in 1D, respectively in 2 and 3 elements in Figure 6.54. Here, the bars were isolated from the converter



with $z_i = r_i + j\ \omega\ l_i$

Figure 6.54. *PEEC modeling*

In this case, we want to assess the electrical equivalent pattern of each bar and the inductive coupling between them. To this end, two fictitious components are added. These can be considered as impedance sensors (Figure 6.55), i.e. devices that measure the equivalent impedance of connections: for the specific case of an impedance only resistive, this is an ohmmeter.

We try to identify elements of the impedance matrix defined as follows:

$$\begin{bmatrix} U_1 \\ U_2 \end{bmatrix} = \begin{bmatrix} Z_1^1 & Z_1^2 \\ Z_2^1 & Z_2^2 \end{bmatrix} \cdot \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}, \text{ with } Z_2^1 = Z_1^2 .$$

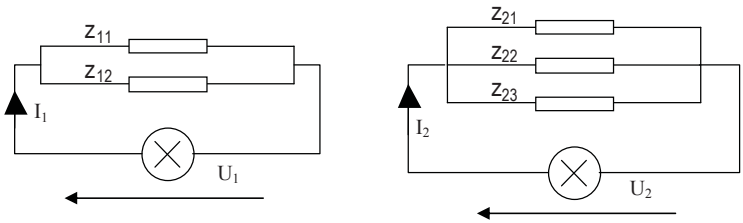


Figure 6.55. *Adopted model*

The associated graph with this electric system is presented in Figure 6.56.

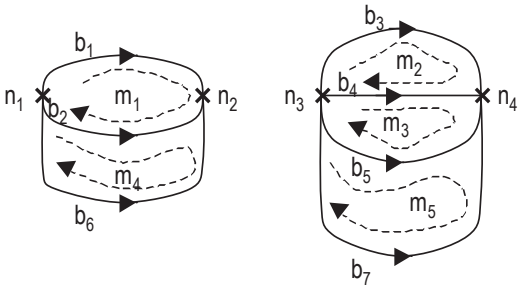


Figure 6.56. *Associated graph*

Starting from this graph, we can define nodes Ni $\left(i \in \{1 \ldots n\}\right)$, branches Bi $\left(i \in \{1 \ldots b\}\right)$ and independent meshes Mi$\left(i \in \{1 \ldots m\}\right)$. The number s of impedance sensors is also defined (here, s = 2). For our example we have n = 4, m = 5 and b = 7.

Note Z the matrix of impedance obtained by modeling with the PEEC method.

$$\mathbf{Z} = \left[\begin{array}{cc|ccc} R_{1_1} + j\omega L_{1_1} & j\omega M_{1_1}^{1_2} & j\omega M_{1_1}^{2_1} & j\omega M_{1_1}^{2_2} & j\omega M_{1_1}^{2_3} \\ j\omega M_{1_1}^{1_2} & R_{1_2} + j\omega L_{1_2} & j\omega M_{1_2}^{2_1} & j\omega M_{1_2}^{2_2} & j\omega M_{1_2}^{2_3} \\ \hline j\omega M_{1_1}^{2_1} & j\omega M_{1_2}^{2_1} & R_{2_1} + j\omega L_{2_1} & j\omega M_{2_1}^{2_2} & j\omega M_{2_1}^{2_3} \\ j\omega M_{1_1}^{2_2} & j\omega M_{1_2}^{2_2} & j\omega M_{2_1}^{2_2} & R_{2_2} + j\omega L_{2_2} & j\omega M_{2_2}^{2_3} \\ j\omega M_{1_1}^{2_3} & j\omega M_{12}^{2_3} & j\omega M_{2_1}^{2_3} & j\omega M_{2_2}^{2_3} & R_{2_3} + j\omega L_{2_3} \end{array}\right]$$

The notation is as follows:

– $M_{A_i}^{B_j}$ which is the mutual coupling between element i of bar A and element j of bar B;

– R_{A_i} which is the proper resistance of element i of bar A;

– L_{A_i} which is the self inductance of element i of bar A.

Note that $M_{A_i}^{B_j} = M_{B_j}^{A_i}$.

Analysis related to voltages: in this approach, the unknown will be the vector of branch voltages U. We will use the laws concerning the matrix N' of incidences of branches at nodes and Ohm's Law expressed through admittances. The impedance sensors are, for this method, current generators. We have:

$$\mathbf{I}_g = [0 \quad 0 \quad 0 \quad 0 \quad 0 \quad I_1 \quad I_2]^t \quad \text{and} \quad \mathbf{Y} = \begin{array}{c} \left[\begin{array}{c|c} \mathbf{Z}^{-1} & \begin{matrix} 0 \\ \vdots \\ \vdots \end{matrix} \\ \hline 0 & 0 \end{array}\right] \begin{array}{l} \updownarrow b-s \\ \updownarrow s \end{array} \\ \begin{array}{cc} \longleftrightarrow b-s & \longleftrightarrow s \end{array} \end{array}$$

The combination of the previous equations gives: $\mathbf{N}' \cdot \mathbf{Y} \cdot \mathbf{U} + \mathbf{N}' \cdot \mathbf{I}_g = \mathbf{0}$.

If we choose a node reference by independent system, we can define the vector V of potential differences between each node and its associated reference node. V is size (n - s) and is linked to the vector U of voltage with the equation: $\mathbf{U} = \mathbf{N}'^t \cdot \mathbf{V}$.

In our case, we took nodes n_2 and n_4 as nodes of reference.

We obtain equality as follows:

$$\mathbf{N}' \cdot \mathbf{Y} \cdot \mathbf{N}'^t \cdot \mathbf{V} + \mathbf{N}' \cdot \mathbf{I}_g = \mathbf{0}$$

To simplify the equation, we note: $\mathbf{Y}_n = \mathbf{N}' \cdot \mathbf{Y} \cdot \mathbf{N}'^t$.

For the example studied, we have:

$$\mathbf{Y}_n = \begin{bmatrix} Y_{1_1}^{1_1} + Y_{1_2}^{1_2} + 2Y_{1_2}^{1_1} & Y_{1_2}^{1_1} + Y_{2_2}^{1_1} + Y_{2_3}^{1_1} + Y_{2_1}^{1_2} + Y_{2_2}^{1_2} + Y_{2_3}^{1_2} \\ Y_{2_1}^{1_1} + Y_{2_2}^{1_1} + Y_{2_3}^{1_1} + Y_{2_1}^{1_2} + Y_{2_2}^{1_2} + Y_{2_3}^{1_2} & Y_{2_1}^{2_1} + Y_{2_2}^{2_2} + Y_{2_3}^{2_3} + 2Y_{2_2}^{2_1} + 2Y_{2_3}^{2_2} + 2Y_{2_3}^{2_1} \end{bmatrix}$$

with $Y_{A_i}^{B_j}$ the admittance between element i of the bar A and element j of the bar B.

The equation becomes: $\mathbf{Y}_n \cdot \mathbf{V} + \mathbf{N}' \cdot \mathbf{I}_g = \mathbf{0}$.

In order to obtain the potential of current generators, and hence find the equivalent impedance of each system, as well as mutual between two systems, we must reverse Yn.

Thus, we express V as follows: $\mathbf{V} = -\mathbf{Y}_n^{-1} \cdot \mathbf{N}' \cdot \mathbf{I}_g$.

For mesh voltages, we obtain the equation:

$$\mathbf{U} = -\mathbf{N}'^t \cdot \mathbf{Y}_n^{-1} \cdot \mathbf{N}' \cdot \mathbf{I}_g$$

We call Zb the matrix $-\mathbf{N}'^t \cdot \mathbf{Y}_n^{-1} \cdot \mathbf{N}'$.

Recall that the vector Ig is a vector composed mainly of 0, except s last terms that are equal to the currents set by the impedance sensors. The matrix Z_b can be broken down as follows:

$$\mathbf{Z_b} = \begin{array}{c} \left[\begin{array}{c|c} & \\ \hline & \mathbf{Z_c} \end{array}\right] \begin{array}{l} \updownarrow b-s \\ \updownarrow s \end{array} \\ \begin{array}{cc} b-s & s \end{array} \end{array}$$

Written in expanded form:

$$\begin{bmatrix} u_{1_1} \\ u_{12} \\ u_{2_1} \\ u_{2_2} \\ u_{2_3} \\ \hline U_1 \\ U_2 \end{bmatrix} = \left[\begin{array}{c|c} & \\ \hline & \mathbf{Z}_c \end{array}\right] \cdot \begin{bmatrix} i_{1_1} \\ i_{12} \\ i_{2_1} \\ i_{2_2} \\ i_{2_3} \\ \hline I_1 \\ I_2 \end{bmatrix}$$

Z_c is the matrix of impedances sought in the case of a reduction.

In summary, Z_c is obtained as a result of several operations:

– inversion of the matrix Z (dimension (b - s) x (b - s));

– inversion of the matrix Y_n (dimension (n - s) x (n - s)).

Before discussing the advantages and disadvantages of this method, we will first present its dual analysis.

Analysis related to currents: for this analysis, the unknowns are the mesh currents. Thus, we will use the laws associated with the mesh-branch matrix M and Ohm's law expressed with the impedance matrix. This time, impedance sensors are voltage generators.

U_g and Z involved in this case are as follows:

$$\mathbf{U}_g = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & E_1 & E_2 \end{bmatrix} \quad \text{and} \quad \mathbf{Z} = \begin{array}{c} \left[\begin{array}{c|c} \mathbf{Z} & \begin{matrix} 0 \\ \vdots \\ \vdots \\ 0 \end{matrix} \\ \hline 0 & 0 \end{array}\right] \begin{matrix} b-s \\ s \end{matrix} \\ \begin{matrix} b-s & s \end{matrix} \end{array}$$

The mesh-branch matrix M is defined so that it is regular. Recall the dimensions of the matrix are m × b.

$$\mathbf{M} = \begin{bmatrix} 1 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & -1 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & -1 \end{bmatrix}$$

Similarly, we define the vector composed of Im mesh currents (dimension m × 1).

This was for our example: $U = \begin{bmatrix} u_{1_1} & u_{1_2} & u_{2_1} & u_{2_2} & u_{2_3} & U_1 & U_2 \end{bmatrix}^t$.

$$\mathbf{I} = \begin{bmatrix} i_{1_1} & i_{1_2} & i_{2_1} & i_{2_2} & i_{2_3} & I_1 & I_2 \end{bmatrix}^t$$

$$\mathbf{I}_m = \begin{bmatrix} i_{m_1} & i_{m_2} & i_{m_3} & i_{m_4} & i_{m_5} \end{bmatrix}^t$$

Vector Im is calculated from vector I expressing the law of meshes, using the matrix M, which gives the equation: $\mathbf{I} = \mathbf{M}^t \cdot \mathbf{I}_m$.

The combination of the previous equations gives:

$$\mathbf{M} \cdot \mathbf{Z} \cdot \mathbf{M}^t \cdot \mathbf{I}_m + \mathbf{M} \cdot \mathbf{U}_g = \mathbf{0}$$

For simplicity, we note: $\mathbf{Z}_m = \mathbf{M} \cdot \mathbf{Z} \cdot \mathbf{M}^t$ and $\mathbf{U}_m = \mathbf{M} \cdot \mathbf{U}_g$.

Here,

$$\mathbf{Z}_m = \begin{bmatrix} Z_{1_1} - 2Z_{1_1}^{1_2} + Z_{1_2} & Z_{1_1}^{2_1} - Z_{1_2}^{2_1} - Z_{1_1}^{2_2} + Z_{1_2}^{2_2} & Z_{1_1}^{2_2} - Z_{1_2}^{2_2} - Z_{1_1}^{2_3} + Z_{1_2}^{2_3} & Z_{1_1}^{1_2} - Z_{1_2} & Z_{1_1}^{2_3} - Z_{1_2}^{2_3} \\ Z_{1_1}^{2_1} - Z_{1_2}^{2_1} - Z_{1_1}^{2_2} + Z_{1_2}^{2_2} & Z_{2_1} + Z_{2_2} - 2Z_{2_1}^{2_2} & Z_{2_1}^{2_2} + Z_{2_2}^{2_3} - Z_{2_1}^{2_3} - Z_{1_1} & Z_{1_2}^{2_1} - Z_{1_2}^{2_2} & Z_{2_1}^{2_3} - Z_{2_2}^{2_3} \\ Z_{1_1}^{2_2} - Z_{1_2}^{2_2} - Z_{1_1}^{2_3} + Z_{1_2}^{2_3} & Z_{2_1}^{2_2} + Z_{2_2}^{2_3} - Z_{2_1}^{2_3} - Z_{1_1} & Z_{2_2} - 2Z_{2_2}^{2_2} + Z_{2_3} & Z_{1_2}^{2_2} - Z_{1_1}^{2_3} & Z_{2_2}^{2_3} - Z_{2_3} \\ Z_{1_1}^{1_2} - Z_{1_2} & Z_{1_2}^{2_1} - Z_{1_2}^{2_2} & Z_{1_2}^{2_2} - Z_{1_1}^{2_3} & Z_{1_2} & Z_{1_2}^{2_3} \\ Z_{1_1}^{2_3} - Z_{1_2}^{2_3} & Z_{2_1}^{2_3} - Z_{2_2}^{2_3} & Z_{2_2}^{2_3} - Z_{2_3} & Z_{1_2}^{2_3} & Z_{2_3} \end{bmatrix}$$

and $\mathbf{U}_m = \begin{bmatrix} 0 & 0 & 0 & -E_1 & -E_2 \end{bmatrix}$.

The introduction of the two previous equations leads to:

$$\mathbf{Z}_m \cdot \mathbf{I}_m + \mathbf{U}_m = \mathbf{0}$$

Calculations allow us to write both following equalities:

$$i_{m_4} = i_{1_1} + i_{1_2} = I_1$$

$$i_{m_5} = i_{2_1} + i_{2_2} + i_{2_3} = I_2$$

As we wish to express equivalent impedances between two points, we have to find out Z_c such that:

$$\mathbf{Z}_c \cdot \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} E_1 \\ E_2 \end{bmatrix}$$

Obtaining Z_c will be carried out using a method able to make partially triangular the matrix Z_m, for example, the Pivot Gauss method. This allows the equality:

$$\begin{bmatrix} 1 & x & x & x & x \\ 0 & 1 & x & x & x \\ 0 & 0 & 1 & x & x \\ 0 & 0 & 0 & Z_{c11} & Z_{c12} \\ 0 & 0 & 0 & Z_{c21} & Z_{c22} \end{bmatrix} \cdot \begin{bmatrix} i_{m1} \\ i_{m2} \\ i_{m3} \\ i_{m4} \\ i_{m5} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 0 \\ E_1 \\ E_2 \end{bmatrix}$$

We can extract the matrix Z_c and therefore equivalent impedances of each independent system.

In summary, the result is obtained using a partial triangular matrix Z_m (dimension $m \times n$).

Comparison of the two analyses: at the beginning of the analysis in relation to the voltages, the analytical aspect is lost while we keep it up until we make the triangular matrix operation in the analysis related to the currents.

To compare the two types of analysis previously exposed, we will recall in a summary table the characteristics of each method.

analysis in relation to the voltages	**analysis in relation to the currents**
Inversion of two matrices: $(b-s)\times(b-s)$ $(n-s)\times(n-s)$	Triangular operation on a matrix $m\times m$

Table 6.4. *Operations for current and voltage methods*

We can conclude that in terms of calculation cost, the analysis related to voltages is much more expensive than that related to currents and the two inversions as the

voltage method looses the advantage of analytical formulae used by the PEEC modeling.

For these two main reasons, the method of analysis related to the currents seems the most appropriate. We keep together as far as possible analytical formulae, which will be an advantage during a phase of structural optimization of converters of power electronics. We can now present the complete modeling synopsis (Figure 6.57).

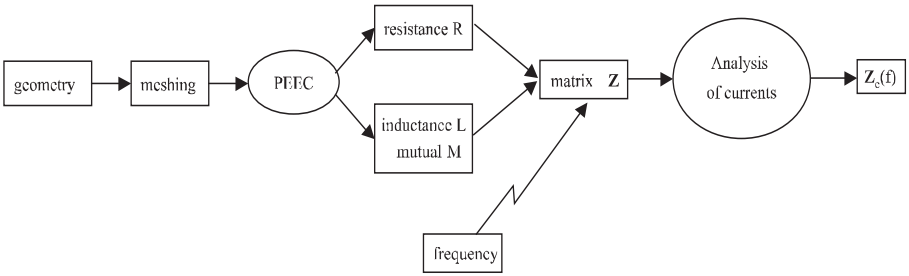


Figure 6.57. *Overview of modeling*

Until the construction of matrix Z, the frequency is not involved in modeling. Now, for the reduction of the schematic, we cannot avoid the influence of frequency. Thus, if we want to perform a frequency analysis, it will require as many partial triangular operations as number of calculation points desired.

If we take the example above, the obtained matrix Z_c includes extra-diagonal terms whose real part is low compared to the real part of the diagonal terms. This is often negligible, so that we can easily translate this result as an electric schematic with localized constants, able to be introduced in a simulation software to obtain the electrical waveforms over all the studied structure.

However in some cases, the real part will not be neglected. We will not be able then to find a representation with located elements in this impedance matrix. In fact, there are no simple components to translate a resistive coupling.

This justifies the following section in which a particular method for dealing with this problem and therefore which generalizes the translation of the equivalent impedance into an electric schematic is detailed.

6.6.1.2. *Between several points*

To be able to model these connections, two problems must be solved: a 2D meshing must be available to treat plates more or less complex, including notches, holes… At the moment, the two softwares, InCa3D – developed by G2elab – [CLA 96] and Fasthenry, software from MIT [KAM 94], are based on a uniform discretization of plates, which generates a large number of components. It must therefore be able to reduce equivalent schematics from this 2D approach, what has been explained in the preceding section.

The connections such as "plates" are not used between two points only. Therefore, an electrical equivalent schematic must be proposed to reflect these multiple accesses. This is the second aspect that will be discussed during this section.

Let us imagine a bus bar simply defined by Figure 6.58, with 8 connection points (4 per plate). According to the mode of presentation of the PEEC method, the most natural schematic will consist of 6 coupled impedances; indeed, on each plate, a point can be chosen as an arbitrary reference, and it radiates from this point to the others. It was therefore required to determine each of these impedances, using InCa. The problem occurs on the terms of couplings between these impedances: terms of resistive couplings appear in addition to conventional mutual inductances.

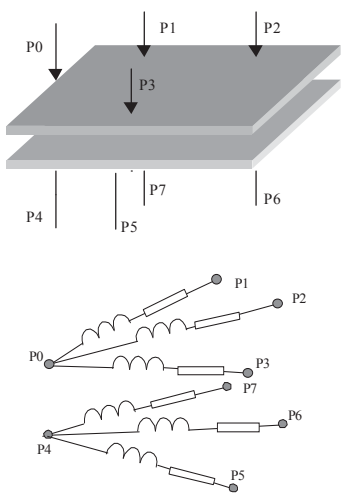


Figure 6.58. *Simple bus bar illustrating the problem of multiple accesses. A possible representation involving resistive coupling (for clarity, no coupling is represented)*

The physical interpretation within a single plate is rather direct: if a supply is applied between two points, a voltage will be induced between two others, which will be both inductive and resistive (current lines may go between these two points and cause a voltage drop). Regarding the case of two separate plates, the explanation lies in the eddy currents induced in the other plate when two points of the first one are supplied. Then there is indeed a common, and therefore resistive, voltage drop.

The "mutual resistance" does not exist in the electrical simulators, any more than the complex elements (complex mutual inductance to represent the resistive linkages): another representation must be adopted if we want to reflect all the phenomena involved in the bus bar.

Using a standard "transformer" approach (because it is here a transformer with n windings), it is possible to move from this "star of branches" representation to another type of "polygonal" representation, using decoupled elements. The method is described below.

We detail the approach on the example in Figure 6.58 using a formalism close to that of the preceding section.

Let us call ni the number of nodes on the plate number i. Here there are two plates; they will be $(n_1 - 1 + n_2 - 1)$ coupled inductances, i.e. $n_L = n_1 - 1 + n_2 - 1$ self-inductances $(n_L = 6)$ and $n_M = \sum_{i=1}^{n_L - 1} i = \frac{n_L(n_L - 1)}{2}$ mutual inductances $(nM = 15)$. The PEEC approach is to establish an impedance matrix Z, complex square matrix of dimension $(n_1 - 1 + n_2 - 1)$ and thus symmetric with $n_L + n_M$ complex elements. Z connects branch currents to branch voltages referenced in points P0 to plate 1 and P4 to plate 2.

$$\begin{bmatrix} V_1 \\ V_2 \\ \\ \\ V_{n_1-1+n_2-1} \end{bmatrix} = [Z] \begin{bmatrix} I_1 \\ I_2 \\ \\ \\ I_{n_1-1+n_2-1} \end{bmatrix}$$

To ensure the change of base and go to "polygonal" representation we need a single reference linking these two points. We find then $n_L = 6$ branch voltages, referenced to the common node "P0P4".

The chosen representation is then to replace the problem of n_L coupled inductances by a system of $n_L + n_M$ decoupled inductances.

The total number of nodes of the problem is then $n = n_1 + n_2 - 1$ ($n = 7$). In addition, we then connect all the nodes 2 by 2 by a non-coupled inductance. We obtain b branches with $b = \sum_{i=1}^{n-1} i = \frac{n(n-1)}{2}$ (b = 21 branches).

Ohm's Law is then written:

$$\begin{bmatrix} U_1 \\ U_2 \\ \\ \\ U_b \end{bmatrix} = \left[Z_{diag}\right] \begin{bmatrix} J_1 \\ J_2 \\ \\ \\ J_b \end{bmatrix}$$

where Z_{diag} is the diagonal matrix of dimension b × b containing the items sought.

The only problem is that we have connected the two plates. To find again the necessary galvanic isolation, three perfect couplers of unit ratio are then inserted at terminal points P0P4, P1, P2 and P3, to provide isolated accesses to the equivalent schematic (Figure 6.59).

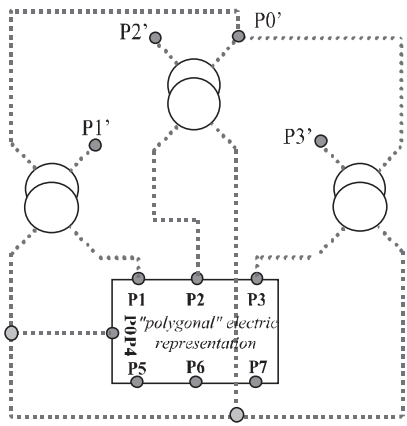


Figure 6.59. *Passage to "polygonal" representation, for example in Figure 6.58 with insulation of the two plates. The access to the model are points P0' to P3', and P5 to P7*

The representation assured, it remains to determine the values of decoupled impedances. The passage is not easy, insofar as we must identify $n_L + n_M$ terms of a matrix $(n_1 - 1 + n_2 - 1) \times (n_1 - 1 + n_2 - 1)$ with b diagonal elements from the "polygonal" matrix processed this way.

Anyone who has already made the passage, for a two windings transformer, from a two coupled inductance representation to the classic "leakage inductance, magnetizing inductance and ratio of transformation" version knows that these calculations, without being complicated, are not immediate as it is to identify term to term two matrices of different sizes. It is easy to find by matrix projection the coupled impedances from the decoupled elements, but the reverse is a little trickier, and it is precisely this sense of passage that we are attempting [SUA 99].

We are actually looking for a formula for transition from Z to Z_{diag}.

For that we are going to intervene in 2 matrices.

Call P_i the matrix which is linking the outgoing currents I_i $\left(i \in [1\ ;\ n_1 - 1 + n_2 - 1]\right)$ to branch currents J_j $\left(j \in [1\ ;\ b]\right)$ of dimension $((n_1 - 1 + n_2 - 1) \times b)$ and P_v the matrix which is linking branch voltages U_j $\left(j \in [1\ ;\ b]\right)$ to simple voltages V_i $\left(i \in [1\ ;\ n_1 - 1 + n_2 - 1]\right)$ of dimension $(b \times (n_1 - 1 + n_2 - 1))$.

This is:

$$\begin{bmatrix} I_1 \\ I_2 \\ \\ \\ I_{n_1-1+n_2-1} \end{bmatrix} = [P_i] \begin{bmatrix} J_1 \\ J_2 \\ \\ \\ J_b \end{bmatrix} \quad \text{and} \quad \begin{bmatrix} U_1 \\ U_2 \\ \\ \\ U_b \end{bmatrix} = [P_v] \begin{bmatrix} V_1 \\ V_2 \\ \\ \\ V_{n_1-1+n_2-1} \end{bmatrix}$$

If we call $Y = Z^{-1}$ the admittance matrix of the schematic with coupled inductances, then we obtain the following relationship: $Y = P_i\, Y_{diag}\, P_v$.

As Y is symmetric, then $tP_v = P_i$.

In addition, by reversing Y_{diag}, we obtain the matrix Z_{diag} desired. The problem is that we have to identify Y_{diag} term by term.

The matrix P_i will be completed using the node law. The matrix P_v is derived from the law of meshes or from the relationship linking it to P_i.

If there is yj $\left(j \in [1\ ;\ b]\right)$ the terms of Y_{diag}, then it is easy to obtain an expression of the terms of Y, with certain conventions to take when describing the two schematics (coupled inductances or polygon).

Conventions:

– the common node is noted 0 and output points are noted 1 to $(n_1 - 1 + n_2 - 1)$;

– currents I_i correspond to the currents flowing from these points;

– branches and hence branch currents will be numbered as follows:

- branch 1 from node 0 to node 1, branch 2 from node 0 to node 2… , branch $(n_1 - 1 + n_2 - 1)$ from node 0 to node $(n_1 - 1 + n_2 - 1)$,

- branch $(n_1 - 1 + n_2)$ from node 1 to node 2…

With these conventions, we can fill in Y as follows:

Upon its diagonal, we put the terms y_1 to $yn_1 - 1 + n_2 - 1$. They then complete the superior triangular part line by line with the following terms (from $yn_1 - 1 + n_2 - 1$ to y_b) by adding a minus sign. Then we complete the diagonal by subtracting from the already written term the sum of other terms of the line.

$$[Y] = \begin{bmatrix} y_1 + \sum_{j=n}^{2n-3} y_j & -y_n & \cdots & \cdots & -y_{2n-3} \\ -y_n & y_2 + y_n + \sum_{j=2n-2}^{3n-6} y_j & & & -y_{3n-6} \\ . & & & & \\ . & & & & \\ . & & & & -y_b \\ -y_{2n-3} & -y_{3n-6} & & -y_b & y_{n-1} + \sum_{j=0}^{n-2} y_{2n-2-(2j+1)} \end{bmatrix}$$

Identification is then easy between Y obtained by reversing Z and Y_{diag}. It is sufficient to begin with the extra-diagonal terms of Y (terms of Y_{diag} directly with reverse sign) and then, by simple addition, complete by using the diagonal terms of Y. A simple inversion of Y_{diag} gives us the matrix Z_{diag} sought.

Note that certain terms may be negative. This is not a problem: any impedance measured between each of the outside access points is always positive, which is the only physical constraint.

There follows an example of processing for a schematic with 3 coupled inductances.

Let us see what this approach gives in the case of a schematic with 3 coupled inductances. This gives a polygon schematic with 6 branches (Figure 6.60).

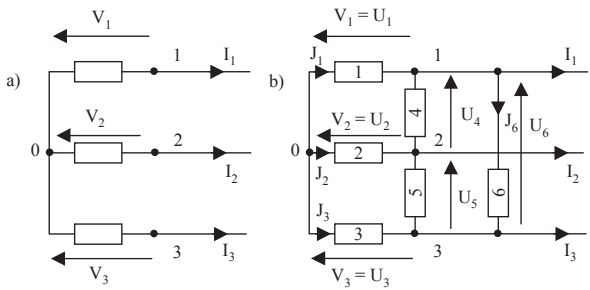


Figure 6.60. *a) Schematic with 3 coupled inductances, b) "polygonal" representation*

We obtain:

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & -1 & -1 & 0 \\ 0 & 1 & 0 & 1 & 0 & -1 \\ 0 & 0 & 1 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} J_1 \\ J_2 \\ J_3 \\ J_4 \\ J_5 \\ J_6 \end{bmatrix} \text{ and } \begin{bmatrix} U_1 \\ U_2 \\ U_3 \\ U_4 \\ U_5 \\ U_6 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \\ -1 & 1 & 0 \\ -1 & 0 & 1 \\ 0 & -1 & 1 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix}$$

let us write:

$$[Y_{diag}] = \begin{bmatrix} a & 0 & 0 & 0 & 0 & 0 \\ 0 & b & 0 & 0 & 0 & 0 \\ 0 & 0 & c & 0 & 0 & 0 \\ 0 & 0 & 0 & d & 0 & 0 \\ 0 & 0 & 0 & 0 & e & 0 \\ 0 & 0 & 0 & 0 & 0 & f \end{bmatrix}$$

then:

$$[Y] = \begin{bmatrix} a+d+e & -d & -e \\ -d & b+d+f & -f \\ -e & -f & c+e+f \end{bmatrix}$$

Then we identify the terms of Y with the result of the inversion of Z to know the 6 unknown variables of the polygon schematic.

As a conclusion, if we know how to model the plates, the method described above provides an equivalent schematic able to be simulated by a circuit software of the PSPICE type. Figure 6.61 shows the result of this approach on a relatively complex industrial example: a bus bar connecting 5 IGBT and 6 decoupling capacitors. The bus bar presents 24 accesses (with plus and minus entries of continuous bus). The result thus includes 506 impedances (506 R and 506 L) $\left(C_{23}^{2}\right)$ and 12 couplers, and may be represented as an hyper block in the PSPICE simulator. Note that an approach neglecting resistive coupling leads to a schematic including 22 coupled inductances (which corresponds to a description that would win 506 – 22 = 484 resistances, since mutual inductances remain).

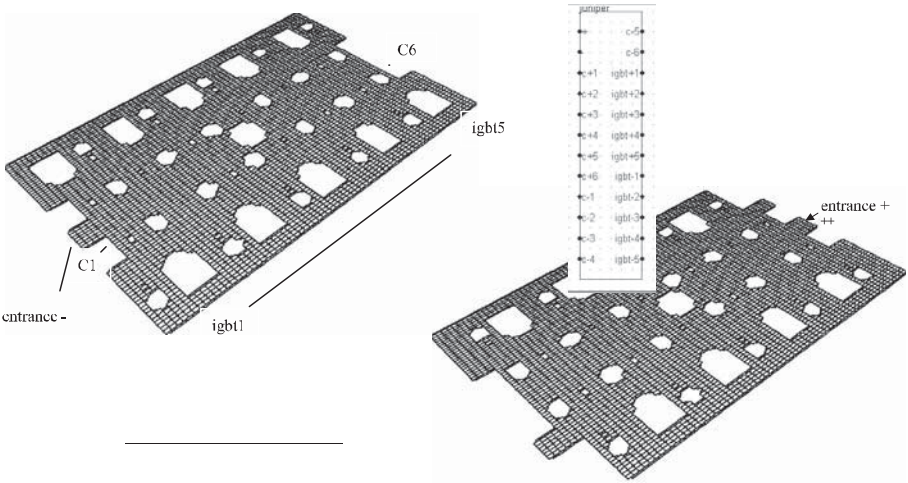


Figure 6.61. *Industrial bus bar involving 5 IGBT and 6 decoupling capacitors, and corresponding PSPICE hyper block*

6.6.2. *Other applications: towards thermal analysis and electrodynamic efforts computation*

The exploitation of equivalent schematics from a PEEC modeling is not the "simple" research of equivalent impedances. Even if these are very useful in order to later carry out an analysis of waveforms of the overall structure, they are not sufficient in the context of a more comprehensive analysis i.e. taking into account other parts of physics.

Indeed, if we refer to the equations in section 6.6.1.2, a simple resolution of the linear system using a direct method such as Choleski gives us access to different currents of meshes. Remember that these currents are actually currents in subdivisions of the mesh device. This resolution is certainly costly in computing time if the mesh is dense but if it is well defined, i.e. adapted to the frequency range of operation of the structure, it must be performed only one time. Thus, if we obtain the current in each of the subdivisions then the current density is immediate with the modeling approach we have adopted.

If we take the example of the bus bar of the Figure 6.61, it is also possible to obtain the distribution of current in each cell after the subdivision of plates (Figure 6.62) when a sine wave generator of voltage with variable frequency is

connected to some ends. It is perhaps interesting to note the current evolution in different parts of the conductor depending on the frequency.

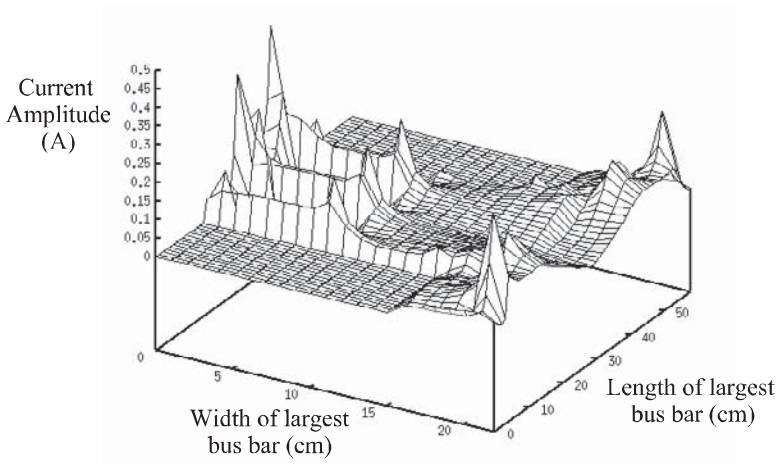


Figure 6.62. *Distribution of current in one of the plates of the bus bar at 10 kHz*

This analysis can be very interesting when we do not know *a priori* the path of current plates lines in a bus bar. Thus we can make geometrical changes (holes, notches, etc.) in conductors to change the routes of power currents and access a more satisfactory operation in terms of power electronics. Gradually, we see the emergence of qualitative design rules that will improve designs which are so far based on essentially empirical approaches.

Moreover, in the case of three-phase structures, the magnitude of the current in each phase is not enough, we must also take into account the phase shift to really evaluate the distribution of current in connections.

The following example shows a three-phase bus bar, each phase consisting of six parallel bars (Figure 6.63), and distribution of the current density in each of them for a given frequency (Figure 6.64) [GUI 00a].

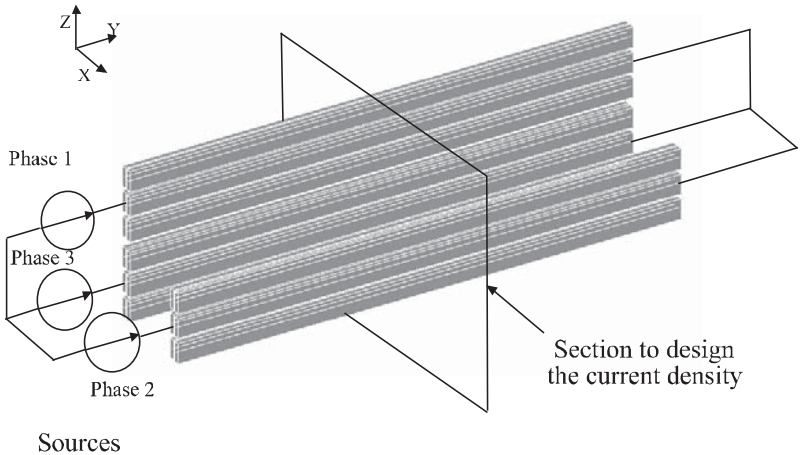


Figure 6.63. *Three-phase structure: set of bars*

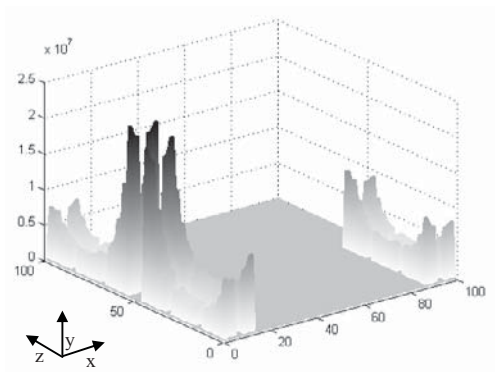


Figure 6.64. *Distribution of current densities in the bars (A/m^2)*

Knowing the current density in conductors is also very useful when we come to other areas of physics which were not previously taken into account in the design phase of the power structures by computer.

6.6.2.1. *Evaluation of losses*

Thus, we can deduce the power dissipated, then it informs us about the thermal aspects of the structure. Already, the display of current densities tells us about the potential hot spots. But now, in order to know the losses, when a three-phase structure is modeled, some currents can be cancelled, making results different from the case of DC operation.

The calculation of the power dissipation is immediate, since we know the current in each mesh subdivision:

$$P_{subdivision} = R_{subdivision} . I_{subdivision}^{2} .$$

with:

– $P_{subdivision}$: power dissipated in a subdivision (W);

– $R_{subdivision}$: resistance of a subdivision (Ω);

– $I_{subdivision}$: effective current through a subdivision (A).

Then the sum of all subdivisions gives the total losses of the device.

Note: if the problem is not meshed or inadequately meshed, there will be some mistake on the current, and as the current is high squared, the error is high squared too. It is therefore necessary to treat the mesh correctly, using geometric subdivisions for example, to obtain dissipated powers close to reality.

When losses are calculated using the method previously indicated, it is sufficient to apply the heat equation to determine temperatures at several points. Note that the conduction is easily assessable throughout electrical equivalent models. The convection and radiation are still based on empirical formulations to determine the different constants of the device (coefficients of convection and radiation).

6.6.2.2. *Evaluation of electrodynamic efforts*

6.6.2.2.1. Calculating the induction

Knowing the current in each of the subdivisions, we can calculate the magnetic field B at any point of the device, applying one of the fundamental principles of electromagnetism: the Biot–Savart law. The elementary dB field created by an element d flown by a current I2 at a point M in space (Figure 6.65) is given by the following equation:

$$d\mathbf{B} = \frac{\mu_0 . I_2 . d\ell \times \mathbf{r}}{4.\pi.R^2}$$

with:

– μ_0 permeability of vacuum (= $4\pi 10^{-7}$ H/m);
– r: unitary vector.

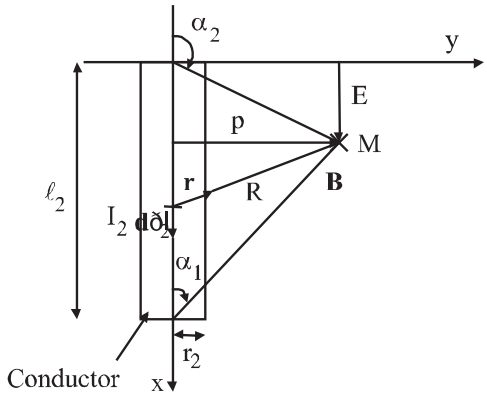


Figure 6.65. *Convention for the calculation of the magnetic field at any point*

This expression gives induction created at M by current element $I_2 d\ell$. This method allows us to calculate the induction created by one or more conductors at all points of space. However, it is possible to observe that when the distance R decreases and tends to 0, induction will move towards infinity. To circumvent this divergence, two cases will be distinguished. The first is obtained when the induction is sought outside of the conductor (for example Figure 6.66, $|p| > r$), the second is obtained when the induction is being sought inside the conductor $|p| \leq r_2$.

In the first case, the expression of B is: $B = \frac{\mu_0 . I_2}{4.\pi.p}\left(\cos(\alpha_1) - \cos(\alpha_2)\right)$.

In the second case, where the induction is being sought inside the conductor, it is necessary not to reflect the entire current flowing through the conductor to avoid the divergence of B which is directly linked to the linear modeling of the wire. For this,

we assume that the current is distributed uniformly in the section of the conductor and that it is circular. It replaces a conductor section most often by a rectangular conductor of the same circular cross-section. After integration, we obtain:

$$B_2 = \frac{\mu_0 . I'_2}{4.\pi.r_2^{\,2}}.p.(\cos(\alpha_1) - \cos(\alpha_2))$$

with $I'_2 = J_2.\pi.p^2$ and $J_2 = \dfrac{I_2}{\pi.r_2^{\,2}}$.

This calculation, immediate when automated, can then obtain the field for the entire device. This may then be useful to take into account the presence of magnetic materials (for example with a finite elements tool) and deduct their impact by superposition.

Validation with a fully digital calculation (finite elements with the Flux3D software) have provided confidence in the previous expressions. An example of such validation is presented Figure 6.66.

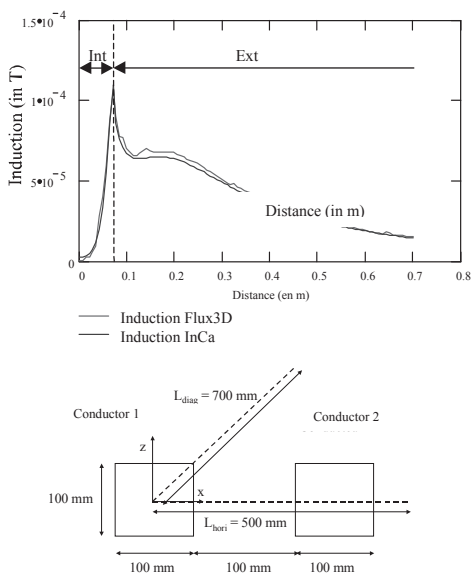


Figure 6.66. *Induction evaluated using the analytical expressions and digitally*

6.6.2.2.2. Calculation of electrodynamics efforts [GUI 00b]

Then the electrodynamics efforts exerted on the plates of a bus bar are immediately deduced, for example under short circuit. Indeed, in this case the destruction of structures occurs (Figure 6.67).

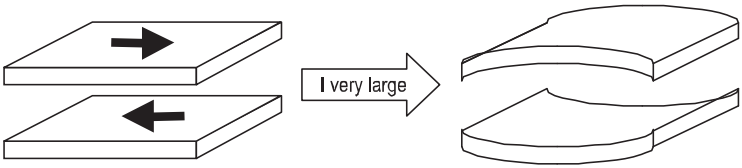


Figure 6.67. *Deformation of bus bars with a very strong current*

Knowing B(M), we can use the Laplace law placed in M, which expresses the variation df of the force exerted on an element d flown by a current I2, immersed in magnetic field B.

To calculate the effort, we use the Laplace law:

$$\mathbf{df} = I_2 \cdot \mathbf{d}\ell \wedge \mathbf{B}$$

Consider the case where currents I1 and I2 are parallel between them, and therefore conductors which carry it too (Figure 6.68). This is the case of the majority of industrial bus bars.

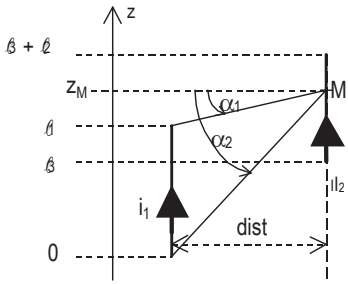


Figure 6.68. *Convention for the calculation of electrodynamics efforts*

After treatment, we obtain an analytical expression which gives the electrodynamics effort between two linear and finished conductors:

$$F = \frac{\mu_o \cdot I_1 \cdot I_2}{4 \cdot \pi \cdot dist} \left[\sqrt{dist^2 + z^2} \right]_{l_3 - l_1, l_3}^{l_3 + l_2, l_3 + l_2 - l_1}$$

with: $\left[f(z) \right]_{z_2, z_4}^{z_1, z_3} = f(z_1) - f(z_2) + f(z_3) - f(z_4)$.

To know effort between two massive conductors, it is required to integrate across the width and the thickness of the conductors the expression above, taking as hypothesis that the current density is uniform in the section of conductors. This calculation has led to very complicated expressions, since primitive forms are elliptical functions.

A question then arises: is it enough to express electrodynamics efforts between two linear conductors in order to know what happens between two massive conductors?

A validation with a numerical calculation showed that it was sufficient to mesh coarsely conductors to take into account the massive behavior of conductors (Figure 6.69), and the overall effort obtained by the sum of the efforts of each mesh is comparable to the effort calculated digitally.

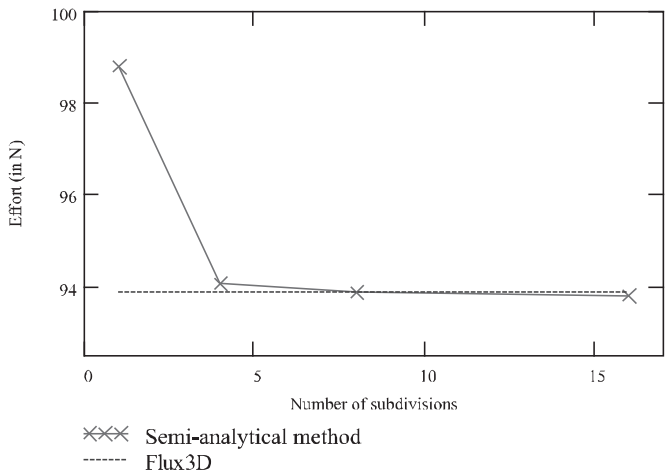


Figure 6.69. *Electrodynamics effort between two massive and parallel conductors*

Similar calculations have been carried out in the case of perpendicular conductors, where we must distinguish between conductors that touch or not. The analytical expression, always in the case of linear conductors, but taking into account a uniform distribution of current in the section, is:

$$F = \frac{\mu_0.I_1.I_2}{4.\pi}.\left[\left[\frac{x}{r_1^2}.\sqrt{p^2+y^2+x^2}\right]_{l_3}^{r_1}(y)\,(x)_{E}^{E-l_1} + \left[\text{sign}(x).\ln\left(\frac{\sqrt{x^2}+\sqrt{p^2+y^2+x^2}}{\sqrt{p^2+y^2}}\right)\right]_{r_1}^{l_3+l_2}(y)\,(x)_{E}^{E-l_1}\right]$$

The previous expressions of efforts between parallel or perpendicular conductors, with or without contact, involve products of currents ($I_1 \times I_2$). In the case that these currents are complex and they are neither opposed nor in phase, it is necessary to take into account their phase shift. The purpose of this section is to show how we will take it into account.

We want to calculate the product $i_1.i_2$, with:

$$i_1 = I_1.\sqrt{2}.\sin\left(\omega.t + \varphi_1\right)$$

$$i_2 = I_2.\sqrt{2}.\sin\left(\omega.t + \varphi_2\right)$$

The development of this product gives the following result:

$$i_1.i_2 = I_1.I_2.\left(\cos(\varphi_1 - \varphi_2) - \cos(2.\omega.t + \varphi_1 + \varphi_2)\right)$$

The average value of the second term of the previous expression is zero. Accordingly, the expressions of electrodynamics efforts when electrical currents are in any phase shift are:

Cases of parallel conductors:

$$F = \frac{\mu_0.I_1.I_2}{4.\pi.\sqrt{p^2+E^2}}.\left[\left[\sqrt{p^2+E^2+x^2}\right]_{l_3,l_3+l_2-l_1}^{l_3+l_2,l_3-l_1}(x)\right].\cos(\varphi_1 - \varphi_2)$$

Cases of perpendicular conductors without contact:

$$F = \frac{\mu_0.I_1.I_2}{4.\pi}.\left[\left[\text{sign}(x).\ln\left(\frac{\sqrt{x^2}+\sqrt{p^2+y^2+x^2}}{\sqrt{p^2+y^2}}\right)\right]_{l_3}^{l_3+l_2}(y)\,(x)_{E}^{E-l_1}\right].\cos(\varphi_1 - \varphi_2)$$

Case of perpendicular conductors with contact:

$$F = \frac{\mu_0 . I_1 . I_2}{4.\pi} . \left[\left[\frac{x}{r_1^2} . \sqrt{p^2 + y^2 + x^2} \right]_{l_3}^{r_1} (y) \, (x)_{E}^{E-l_1} + \left[\text{sign}(x) . \ln \left(\frac{\sqrt{x^2} + \sqrt{p^2 + y^2 + x^2}}{\sqrt{p^2 + y^2}} \right) \right]_{r_1}^{l_3+l_2} (y) \, (x)_{E}^{E-l_1} \right] . \cos(\varphi_1 - \varphi_2)$$

with I_1 and I_2 effective currents in Amps.

To address the mechanical structure, we must then translate the global efforts between conductors in terms of constraints on connections to incorporate these new data in design tools.

6.7. Conclusion

The purpose of this chapter was to show that, given the current need to take into account the wiring in power electronics as a component like the others, we can propose a method that is both generic and adapted to the design. This PEEC (Partial Element Equivalent Circuit) method not only calculates the values of model interconnection elements (resistance, inductance and mutual inductance), taking into account the frequency and proximity effects but, it provides a better understanding of magnetic phenomena, thus generating design rules to make little inductive connections, depending on the available technology.

It can justify many modern technological solutions dedicated to the “nanohenry hunt” for high power applications, such as bus bar technology, and provides criteria to choose an interconnection geometry rather than another. We show that for a constant volume of copper, a plate will be less inductive than a square bar.

Already, it is possible to add manually in “circuit” software, parasitic capacitances whose evaluation does not raise any particular problem.

The InCa3D software, based on this method, now opens the door to a real CAD technology in power electronics, to quantify, before realization and prototyping, the gain expected on the inductance by a particular geometry interconnection.

In addition, it enables EMC evaluation of an electrical device based on its wiring (coupled with the electrical simulation software SPICE, SABER, SIMPLORER, etc.).

In the future, this software will be able to take into account the mechanical and thermal constraints exerted on the wiring; it will be the complete design tool for wiring technology.

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