Power Electronics Semiconductor Devices
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Chapter 4

Silicon Carbide Applications in Power Electronics

4.1. Introduction

Despite its extreme rarity in the natural state, silicon carbide was one of the first semiconductors discovered: J.J. Berzelius (the "father" of silicon) was the first to study its physical properties, in 1824. The first to exploit its electro-luminescent properties was H.J. Round, in 1907 [ROU 07]). In 1955, Lely [LEL 55] was defining the first method of synthesizing mono-crystalline substrates, the dimensions were admittedly small and random, but had very good structural quality. Thus, the first period of intense research devoted to silicon carbide (in the USA, Russia, Japan, Germany) dates back 50 years, driven from the beginning by the very interesting physical properties of this material for solid state electronics.

Yet it is only recently (in 2000 and 2001) that the first ads for industrial manufacturing of power components, based on silicon carbide, were made (by Microsemi, then Infineon), in the form of Schottky diodes, with voltage and current ratings that now reach 600 V and 12 A. These initial products are the result of works revived and expanded throughout the world in the 1980s, thanks to new major discoveries in the field of manufacturing techniques usable by the industry. Despite the tremendous growth of the silicon industry and the considerable developments already achieved, the approaching of silicon's physical limits in many applications, particularly those in power electronics, also contributes to the high level of interest

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being generated for some semiconductors with large prohibited broadband energy, particularly silicon carbide.

Given the potential of power components made of the emerging silicon carbide, and those of the prototypes reported by the specialized journals, this "new" semiconductor now appears to be able to:

– favorably replace silicon in certain applications by improving the overall performance of the system (remembering that silicon is the material of choice almost exclusively for the manufacture of power components);

– to expand the fields of existing applications; or even

– give rise to new areas of use previously inaccessible for semiconductor components.

Before presenting the various potential applications of new silicon carbide (SiC) power components, this chapter will become better acquainted with the material, before describing the state of the art technology. The final section will present designs already made with SiC, SiC impact on the design and performance of systems, and will indicate the likely applications of these systems.

4.2. Physical properties of silicon carbide

4.2.1. *Structural features*

Electronic applications involve devices based on semiconductor materials with crystalline structures.

The crystal structure of monocrystalline silicon is characterized by an arrangement of Si atoms along a face centred cubic network, with a mesh parameter of 5.431 Å. The structure of crystalline silicon carbide on the other hand can be described simply by stacking compact plans, each plan being a double layer of a compact plan of C atoms on a compact plan of Si atoms. The pile of a second double layer on a first one can be in two positions, different from each other and different from the position of the first level. This is obviously the same for the next level, and so on. The three possible positions for a double layer are generally named A, B and C. According to the stacking sequence (e.g. ABCB…) and its recurrence (e.g. 2 for AB*AB*AB*AB*… and 4 for ABCB*ABCB*ABCB…), the elementary mesh can be cubic (C), hexagonal (H) or rhomboid (R). Only one dimension of the grid (height, in the direction [0001] perpendicular to the plains, which is the axis of growth, axe c), is different from one pile to another. This way, several crystallographic arrangements may exist for the same chemical composition SiC.

This peculiarity of silicon carbide is named after polytypism (which is a polymorphism in one dimension).

170 to 200 crystallographic varieties or polytypes have been counted. Among them, few have been synthesized into the form of mono and stable materials (without inclusion of different polytypes). The polytypism of SiC also explains in part the difficulties historically found, and even today, for the production of substrates and homogenous SiC films, especially since it gives to each polytype physical properties whose ranges vary from one to another (as shown in the following section).

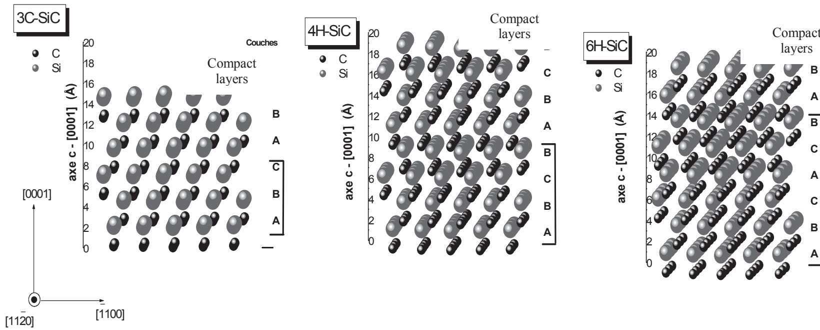


Figure 4.1. *Presentation of polytypes SiC-3C, SiC-4H and SiC-6H, and of Ramsdell notation. This allows kinds of SiC to be distinguished by a number (stacking periodicity) followed by letter C, H or R (form of the elementary mesh)*

Polytype	**3C**	**4H**	**6H**
Stacking sequence	ABC	ABCB	ABCACB
Mesh parameters (Å) **Si : a = 5.431 Å**	a = 4.349	a = 3.073 c = 10.05	a = 3.081 c = 15.12

Table 4.1. *Characteristic dimensions of crystalline meshes of SiC-3C, SiC-4H, SiC-6H and Si, at 300 K*

The most common polytypes studied for electronics are known as SiC-3H, SiC-4H, SiC-6H, according to the notation of Ramsdell. Figure 4.1 illustrates these three structures and the principle of Ramsdell notation. Table 4.1 shows for each polytype

the specific dimensions of their crystal mesh at room temperature, as well as those relating to silicon.

4.2.2. *Chemical, mechanical and thermal features*

The link between the Si atom and the C atom is strong, with an energy equal to 6.34 eV (the binding energy between two atoms of silicon is only 4.63 eV). This simple fact makes silicon carbide a resistant material from various points of view, and contributes to the interest for it, for various applications including electronics. This property, however, includes drawbacks for the implementation of the SiC semiconductor.

Firstly, SiC is high temperature resistant, breaking only at 2,830°C. Sublimating rather than melting under reasonably accessible pressure, silicon carbide cannot be synthesized from the liquid phase by conventional techniques of recrystallization. The growth of a single crystal is more delicate than that of silicon, especially as the resulting crystalline arrangement is very sensitive to the conditions of temperature and pressure.

Silicon carbide is also chemically resistant, and it is very difficult for a foreign atom to penetrate the network of this material to travel inside. An input of energy (e.g. heat, photonics, electrical, or mechanical, etc.) higher than the case of silicon is necessary. In terms of temperature stability, these features are assets for operation in hostile environments and for reliability, but they do not facilitate the steps of production of components based on chemical reactions (cleaning, engraving, oxidation) or diffusion of impurities.

Since Acheson developed the first manufacturing process of SiC, in the 19th century, silicon carbide has been well known for its mechanical resistance as an abrasive n the form of clusters of hexagonal mono crystals, impure and from various polytypes and sizes). This hardness (about three times that of silicon), which is not really a superiority for electronic applications, is reported here because it has an effect on mechanical treatments, such as cutting and polishing units in the manufacture of semiconductors for electronics.

In terms of thermal expansion, the coefficient of silicon carbide ($4x10^{-6}$ K^{-1}) is approximately two times greater than that of Si, which increases the gap with that of silica ($5.5x10^{-7}$ K^{-1}), but reduces to that of copper ($17x10^{-6}K^{-1}$), or aluminium ($22x10^{-6}$ K^{-1}).

4.2.3. *Electronic and thermal features*

As referred to in the introduction of this chapter, the attraction to the physical properties of silicon carbide for use in electronic applications is at the heart of many studies that have been, and are now doomed. The vast majority of these studies concern the three most common polytypes: 3C-SiC, 6H-SiC and 4H-SiC. Many publications present measurements and modelling parameters of these materials, and some properties are nowadays accurately determined (such as the forbidden energy band, or the effective masses, etc.). However, due to sensitivity to the purity of the material, or its anisotropy, some parameters are fairly dispersed or incompletely determined (e.g. mobility and saturation speeds of load porters, especially holes; or critical breakdown field, etc.). Table 4.2 brings together the main important features for the performance of semiconductor components. The values given are trying to account for dispersions, being an average of the main results of edited measures, for a temperature of 27°C, and for a doping of 10^{15} cm^{-3}. All three SiC polytypes, with whom structure tests were performed, are considered here along with silicon, as a benchmark. For hexagonal polytypes, the values of mobility and speeds of load porters are provided for both parallel directions ($||$c) and perpendicular ($\perp$c) to the axis of growth c.

	Si	3C-SiC	6H-SiC	4H-SiC
E_g (eV) **Forbidden bandwidth**	1.12	2.2	3.02	3.26
E_c (MV/cm) **breakdown electric field**	0.28	1.5	2.2	2.2
ε_r **dielectric constant**	11.8	9.66	9.7	10
μ_n (cm^2/Vs) **intrinsic mobility of electrons**	1350	900	400 ($\perp$c) 90 ($||$c)	800 ($\perp$c) 1,000 ($||$c)
μ_p (cm^2/Vs) **intrinsic mobility of holes**	480	40	100 ($\perp$c) 20 ($||$c)	110 ($\perp$c) 140 ($||$c)
v_{sat} (10^7 cm/s) **saturation speed of carriers**	1	2.5	2 ($\perp$c) 0.2 ($||$c)	2.2 ($\perp$c) 0.33 ($||$c)
n_i (cm^{-3}) **intrinsic concentration**	$1.4x10^{10}$	6.9	$2.3x10^{-6}$	$8.2x10^{-9}$
λ_{th} (W/cm.K) **thermal conductivity**	1.5	4.9	4.9	4.9

Table 4.2. *Main physical properties for components performances: comparison of most common SiC polytypes and silicon (values at 300 K for doped materials at 10^{15} cm^{-3})*

4.2.3.1. *A large forbidden energy bandwidth*

Silicon carbide is part of the family of semiconductors known as "big gap" because of its *prohibited energy bandwidth* E_g, which is higher than that of silicon (2 to 3 times according to the polytype). Two other important properties follow on from this, which are a higher *breakdown electric field* E_c (almost multiplied by 10), and a lower *concentration of intrinsic* n_i *load carriers* (9 to 19 orders of magnitude depending on the polytype).

4.2.3.1.1. Improvement of the voltage and temperature strengths

With such features, silicon carbide makes it possible to increase the range of blocking voltages allowed by the semiconductor components, and this includes at high junction temperatures. Indeed, breakdown voltages, exceeding 10 kV in volume, can be supported by layers with doping levels between 10^{14} cm^{-3} and 10^{15} cm^{-3}, and thicknesses as low as 70 µm – 80 µm, as shown in the charts presented in Figure 4.2.

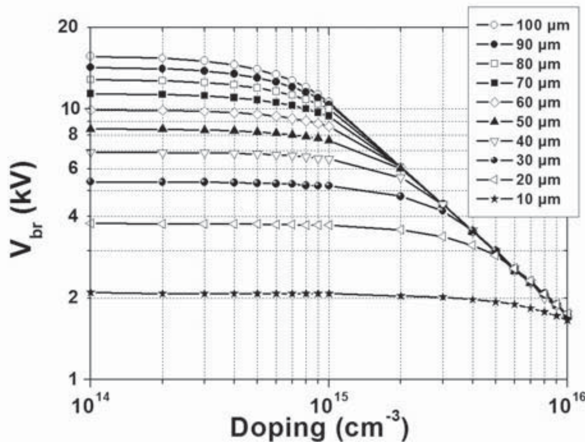


Figure 4.2. *Breakdown voltage V_{br} (V) as a function of doping N_D (cm^{-3}) and thickness W_N (µm) of the voltage submitted layer, providing numerical calculation of the inverse characteristic, and taking into account ionization coefficients per impact provided [KON 97]*

Recall that the breakdown mechanism is the ionization of an atom of the network, by impact with a free carrier greatly accelerated by the local electric field. If the kinetic energy gained by such a carrier is enough, it can "obtain" an electron from the top of the valence band to the bottom of the conduction band, leaving a vacancy in the valence band called a hole. A new electron-hole pair is created, which will be able to participate to the increase of the reverse current through the

structure (possibly generating, in turn, an electron-hole pair by ionizing collision, thus contributing to the increasing number of load carriers).

Charts in Figure 4.2 provide the breakdown voltage in volume of a plane structure P^+NN^+, with dissymmetric and abrupt junctions. The breakdown voltage is calculated numerically and corresponds to the voltage where the multiplication factor of holes or electrons becomes infinite along a line of maximum field in the structure. The calculation is made according to the slight doping of the central layer slight N doped (the "voltage held layer"), for different thicknesses, and at a uniform temperature of the semiconductor equal to 300 K; having retained as a coefficient the values of ionization of electrons and holes published by Konstantinov *et al.* [KON 97].

Calculations of leakage currents through the P^+NN^+ structure in the opposite polarization, as a function of temperature, also show that the leakage currents associated with the thermal generation assisted by inherent pitfalls porters in the deserted area (J_{gen}), and with the diffusion of minority carriers from the adjacent neutral areas (J_{dif}), remain low in the case of silicon carbide up to a very high temperature.

Concentration of intrinsic carriers in a semiconductor of gap E_g: where N_C and N_V are state densities in conduction and valence bands, and where T is temperature	$n_i = (N_C.N_V)^{1/2}.\exp(-E_g/2kT)$
Thermally generated current in the state charge area: in which width is W_N, with τ rate of generation, and q elementary charge	$J_{gén} = q.n_i.W_N/\tau$
Diffusion current of holes from N zone: with doping N_d, with μ_p and τ_p mobility, and lifetime of holes	$J_{dif} = (qk.T)^{1/2}.(\mu_p/\tau_p)^{1/2}.n_i^2/N_d$

Table 4.3. *Intrinsic concentration of carriers and volume leakage current through a P^+N junction (abrupt and dissymmetric) under reverse polarization*

For example, an analytical assessment (from the relationships mentioned in Table 4.3) of J_{gen}, J_{dif} and of evolution in temperature of intrinsic concentration n_i, shows that we should reach 600°C, in the case of the SiC polytype 4H, so that the density of total leakage current exceeds 1 $mA.cm^{-2}$, in a deserted layer, with a thickness $W_N = 100$ µm, which is doped at $N_d = 10^{15}$ cm^{-3}, and where the time constant of carriers generation would be equal to $\tau = 1$ µs (considered as independent from temperature).

For comparison, in the case of silicon, the purest and thickest layers produced nowadays are characterized by thicknesses and doping slightly below 1 mm and 10^{13} cm^{-3} respectively. The maximum corresponding voltage ratings (in volume) reach 10 kV maximum, as can be seen on the charts in Figure 4.3. A $P^+N^-N^+$ structure with a "voltage holding" layer with the characteristics mentioned above, considering carrier lifetime is maintained at a high value of 100 µs, must operate with a junction temperature below 150°C, so that the leakage current does not exceed a density of 1 $mA.cm^{-2}$. Note: a decrease of lifetime (including concerns about giving more rapid features to the structure during commutations between on-state and off-state) would lead to a severe reduction of this temperature (50°C less for a decrease of τ by a factor of 10 only…

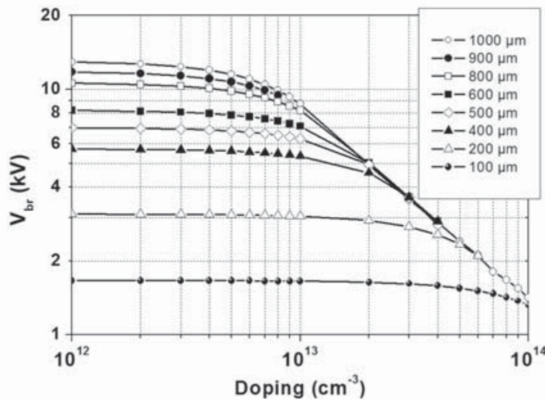


Figure 4.3. *Breakdown voltage V_{br} (V) as a function of doping N_D (cm^{-3}) and thickness W_N (µm) of the layer of Si under voltage, provides the numerical calculation of the reverse characteristic, taking into account the impact ionization*

So the progress made by the silicon carbide due to a forbidden energy band is broader (resulting in a higher breakdown electric field), and appears to be significant in terms of increased voltage ratings and the setback of the allowable operating temperature limits, if considering physical properties of the material in volume; and ideally free of defects.

4.2.3.1.2. Note about bipolar components

We should note that prohibited energy bandwidth also means a higher barrier of the PN junction. It will be more necessary to apply an extra 2 V to the terminals of a homo-junction of 4H-SiC, than to a homo-junction of silicon, to achieve the on-state. However, for applications with very high voltage, as considered in this part, this drawback will not present a drawback for bipolar components.

4.2.3.2. *Sufficiently mobile load carrier*

Let us now consider the range of voltage ratings already covered by components made of silicon, and consider the fact that the higher *breakdown field* of SiC leads to the ability to withstand a voltage under switch-off state, with a semiconductor layer whose doping is higher for a lower thickness. In addition to the reduction of the corresponding dimensions (interesting itself), this is especially relevant in terms of reducing conduction losses, all the more important since the *mobilities (μ_n and/or μ_p) of load carriers* involved in the mechanism are high.

Expressing these concepts with numbers, Table 4.4 shows the relative values of the factors of merit introduced by Baliga to indicate the interest in a new material for the design of a unipolar high-voltage component, minimizing conduction losses (with the BFM [BAL 82]), or the switching losses (with the BHFFM [BAL 89]). These values are normalized by those of silicon and allows a N-type conduction either lateral (perpendicular to the c axis), or vertical (parallel to the axis c), to reflect the anisotropy of the physical properties of 6H and 4H polytypes. (Note: the crystal structure 3C-SiC has no anisotropy in terms of its physical properties, as it is cubed). Note only the resistance of the layer of holding voltage is taken into account when calculating conduction losses.

This table shows again that significant progress is expected from the use of silicon carbide for the manufacture of high-voltage unipolar components. According to this "first order" assessment, the 4H polytype is the most promising, both for structures with vertical conduction and with lateral conduction.

We can greatly reduce the compromise between high current density in the on-state and high voltage rating, and increase the voltage range of unipolar components. From 200 V (maximum voltage rating with Si), the voltage ratings of Schottky diodes could be extended up to 3 kV. As unipolar devices (Schottky diodes such as field effect transistors) commutate faster than bipolar devices, a step forward in terms of reduced switching losses and increased switching frequencies of operating systems, which result at the same time.

Merit factor	**3C-SiC**	**6H-SiC**	**4H-SiC**
BFM / BFM (Si) *where* $BFM = \pi \mu_n E_g^3$	4	4.5 (⊥c) 1 (‖c)	12 (⊥c) 14.9 (‖c)
BHFFM / BHFFM(Si) *where* $BHFFM = \mu_n E_c^2$	16	15 (⊥c) 3.5 (‖c)	31 (⊥c) 38 (‖c)

Table 4.4. *Merit factors by B.J. Baliga for SiC common polytypes, divided by the corresponding values in the case of silicon (notations and values of physical parameters from Table 4.2 were used for these calculations)*

For the highest voltage ratings, the possibility of modulation of the electrical resistivity of the voltage held layer makes the bipolar device a more attractive option. In the case of bipolar components in SiC, the large voltage drop across the terminals of the PN junction (as a result of the broad band of prohibited energy) will be less of a drawback, for a given voltage class, as levels of current densities and frequency of the application will be higher. These conditions of use are promoted by both the ability of these devices to operate at high temperature, and to switch quickly.

4.2.3.3. *A high speed to saturation*

Under strong electric field (over some 10^5 V/cm), the drift velocity of electrons and holes tends towards a limit value. This *saturation speed* v_{sat}, which is twice as fast with silicon carbide, is still in its favor compared to silicon, for application on power components working at a high frequency.

Merit factors	3C-SiC	6H-SiC	4H-SiC
JFM / JFM (Si) *where* $JFM = v_{sat}^2 E_c^2 / 4\pi^2$	156	215 (⊥c) 2 (||c)	260 (⊥c) 6 (||c)

Table 4.5. *Merit factors by E.O. Johnson for common polytypes of SiC, divided by values for silicon (notations and values of physical parameters from Table 4.2 were used for these calculations)*

An idea of the expected gains is rendered by Johnson's figure of merit of (JFM [JOH 63]), whose values are presented in Table 4.5. These performance gains are very important, especially for the two hexagonal polytypes, when the electronic conduction is perpendicular to the axis of growth c.

4.2.3.4. *A high thermal conductivity*

Losses in the components (both during their conduction or commutation phases) are an internal source of heating. When they cannot (for one physical intrinsic reason), or should not (to meet their immediate environment) work beyond a certain temperature, the ability of the device to dissipate heat is a desired quality, starting with the semiconductor itself. The latter is also appreciated when the structure is sensitive to the presence of hot spots, to reduce the temperature deviations by spreading better heat fluxes. With a thermal conductivity about three times higher than that of silicon, silicon carbide offers prospects for improvement in this regard.

4.2.3.5. *More generally (at the system level) and abstract*

The benefits of using silicon carbide as the basic material for the manufacture of components for power, have been mentioned above:

– the rise of voltage;

– the rise in temperature;

– reducing the size;

– minimizing losses;

– the increasing frequency;

– the rising power.

These gains at the component level obviously have an impact on the performance of the system into which the component will fit. In particular, silicon carbide allows for the consideration of a greater density of system integration with smaller components, whether active or passive (including inductive elements working at higher frequencies), and the prospect of less complex systems (with fewer series or parallel connections, or simplification of the problems of adaptation of impedance, or problems of cooling, etc.).

In summary, considering the elements presented above, silicon carbide satisfies theoretically the first clauses for an alternative solution to replace an existing and already very well established solution: to obtain a significant gain on the performances of many systems. We will further see that sectors previously out of the reach of silicon may even be involved.

4.2.4. *Other "candidates" as semiconductors of power*

In fact, outside the silicon, only gallium arsenide (GaAs) is the subject of sales of slices (up to 150 mm diameter), and the market for telecommunications systems implementing GaAs components is booming. however, this material progress appears inadequate next to that of silicon, and to the needs of power systems to allow a significant place for this material.

Other semiconductor materials, such as diamonds, or some nitrides, particularly GaN, are also alternatives that are currently being researched [CHO 00], because they present the potential for a major increase in the level of performance for power electronics, sometimes earning well above what has been described for SiC. Nevertheless, they do not comply with yet another essential clause for the emergence of a new industrial application: the availability of mono-crystalline

substrates of sufficient size and quality. The major obstacles have not yet all been removed in terms of the mastery of basic techniques required for the achievement of a semiconductor component on the basis of these materials, such as control of the conductivity (type N or P) by doping, etching, metallization of contacts, filing of dielectric or encapsulation.

Instead, the maturity of the technology in the industry based on silicon carbide, especially for 6H and 4H polytypes, is already sufficient to enable the emergence of the first power components on the market. The following section gives state of the art expertise on the components acquired at various stages of manufacture, as well as on the main areas of current research.

4.3. State of the art technology for silicon carbide power components

In this section we briefly describe, as a priority, the techniques adopted by the industry, or most commonly used by research centres. The technology of silicon is mentioned to highlight the differences or the similarities between the two chains.

The characteristics able to assess the level of quality achieved at each stage of the development of a component are mentioned. Those characteristics likely to have an impact on the proper operation of the devices are primarily selected, in order to understand their performances in the final part. We are also trying to provide an overview of the derivative of progresses.

4.3.1. *Substrates and thin layers of SiC*

Three among many identified polytypes of silicon carbide, were able to be synthesized in the form of massive monocrystalline materials, used in the manufacture of electronic components: they are chronologically 6H-SiC, 4H-SiC, and very recently 15R-SiC. These materials are prepared to be used as substrates, on which thin films are implemented for devices realization. Only substrates 6H-SiC and SiC-4H, epitaxial or not, are commercially available. Note that 6H-SiC N-type also has a broad market potential as a GaN substrate for the production of electroluminescent components.

As this section reports, synthesis techniques of SiC are much more sensitive than those of silicon, this justifies the historical difficulties, and suggests that the cost of this type of material is likely to remain high.

4.3.1.1. *Monocrystal growth for the production of substrates*

4.3.1.1.1. Roles and qualities expected

The substrate serves mostly as mechanical support around which will be deposited the various films (single-crystal film, insulation or metal) to make the final device. In silicon technology, when the voltage rating requires a layer of semiconductor very thick and lightly doped, it can be produced by the substrate itself. In all cases, the structural properties, electrical and thermal, of this substrate are very important, as an integral part of the structure.

4.3.1.1.2. Technical production and marketing

The commercialization of the SiC material dedicated to microelectronics began in the USA in 1989. The company CREE Research proposed slices of 6H-SiC of 25.4 mm in diameter. Today several vendors ([CRE 01a], [STE 01], [OKM 01], [NIP 01], [SIX 01], [SICr 01]) of platelets of 6H SiC up to 76.2 mm diameter and 4H-SiC up to 50.8 mm diameter are present on the world market (Finland, Japan, Germany, and always the USA).

The most common growth technique is based on the vapor phase transport of the chemical species involved, obtained by sublimation of a source of SiC material in the 2,200-2,500°C range, therefore high if the reference is once again that of silicon, followed by condensation on a germ of monocrystalline SiC, introducing the polytype desired. The germ is placed near the source and brought to a temperature slightly below the temperature of the source (the pressure inside the crucible is in the order of 10 to 50 Torrs). The speed of growth by this technique is in the order of several mm/h.

A monocrystalline ingot of a few centimeters in height is obtained by this method, also known as the “Lely modified” (originally discovered by Tairov and Tsvetkov [TAI 78]). The ingot is then rectified in the form of a cylinder to provide slices after sawing and polishing (which are non-trivial steps because of the hardness of the material).

4.3.1.1.3. Current characteristics

In addition to controlling the polytype (by the nature of the germ), the growth of massive SiC by this technique allows control of the size, structural quality and electrical conductivity of the substrate produced.

In regards to the crystalline quality, which has been making constant progress in recent years, typical values and best results characterizing the major flaws existing in the marketed silicon carbide substrates are presented in Table 4.6. Only those defects inducing an impact on the quality of epitaxied films on these materials are

cited. (For example, parallel dislocation loops to the base plane of the substrate, present in very high density but which do not propagate in the epitaxial layer, are not included in Table 4.6 [NEU 00].) It is also known that the material still contains many chemical impurities.

The resistivity of the semiconductor is also controlled for the growth of the monocrystal, by incorporation of doping atoms (nitrogen for N and aluminum for P). The heavily doped substrates required for the manufacture of components for power electronics, have resistivities that vary between suppliers. We can find, for example, 15-30 mΩ.cm for the 4H-SiC N-type and 2.5-8.5 Ω.cm for 4H-SiC P-type (corresponding to the doping of some 10^{18} cm^{-3}). Several substrates 6H-SiC or 4H-SiC, semi-insulating materials, are also available from some manufacturers, primarily dedicated to the market of power microwave components. The resistivities in these cases are above 10^5 Ω.cm.

It should be noted that the thermal conductivity of the material is affected by the crystalline quality: it is typically 3 to 3.8 W/cm.K (at room temperature) for the traded substrates, compared to 4.9 W/cm.K measured for the purest substrates (produced by Lely's method).

Type, nature of defects	**Density or % of the surface of the substrate**
Micro pores (or dislocation opened screw)	< 30 cm^{-2}
dislocations closed screw	3,000 cm^{-2} to 10,000 cm^{-2}
Hexagonal form plates	< 10 %
Small growth cavities (orange skin)	< 10 %
inclusions (polytype 3C, ...)	< 5 %

Table 4.6. *Typical data from CREE [CRE 01a] for SiC substrates (50.8 mm diameter) of "Production" quality (qualified area corresponds to the whole surface of the slice, excluding a border of 2 mm width)*

4.3.1.1.4. Avenues of research

The process of growth is the subject of much research to improve the ingot's quality [ANI 99]. Further progress is required to reduce the density of defects in large-diameter substrates, in order to increase yields and reduce manufacturing costs, both of the base material and components that will use it. Diameters of up to 100 mm have been demonstrated in the laboratory, along with micropore densities of less than 1 cm^{-2}. With regard to this type of defect, Figure 4.4 [HAR 01]

illustrates the evolution of their presence in recent years, as well as the changes expected for the future: according to these forecasts, obtaining the required densities for the production of large-scale power components (for ratings in currents beyond 100 Amps) should occur around 2005.

In parallel to these studies for optimization by the "classical" method, alternative techniques provide material of good crystal quality, such as chemical vapor deposition at high temperature (HTCVD) [ZHA 01], or liquid phase epitaxy (LPE) [REN 98], are investigated, with the goal of increasing their deposit rates (which are currently in the order of several hundred μm/h). We would like also to mention that the HOYA Corporation [HOY 01] has presented at the International Conference ICSCRM 2001, a slice of 3C-SiC of 100 mm diameter, produced by hetero epitaxy on a silicon substrate, eliminated thereafter [NAG 01]. The main characteristics of this material are a thickness of 200 μm, a density of crystalline defects less than 10 cm^{-2} with no micropores, and a level of doping (N or P type) from 10^{15} cm^{-3} to 10^{19} cm^{-3}. 3C-SiC substrates are even marketed at a very attractive price.

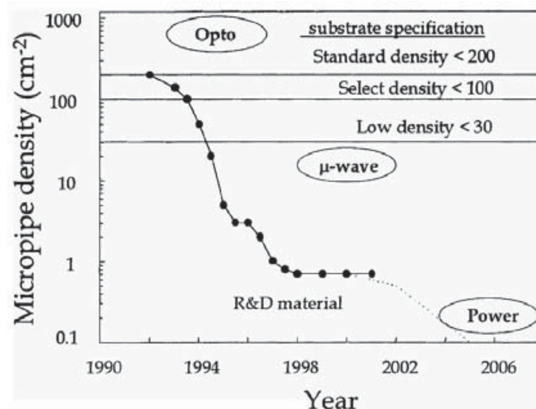


Figure 4.4. *Temporal evolution of the defect density of micropore type, in substrates elaborated in laboratories by the "modified Lely method" (figure from [HAR 01]). The authors indicate the required levels for commercialization of optoelectronic components, microwaves or power, together with specifications of substrates by the supplier CREE*

4.3.1.2. *Obtaining monocrystalline thin films*

4.3.1.2.1. Roles and expected qualities

The active parts of a component are generally in "thin" semiconductor layers filed to that effect on the substrate. This substrate typically has a thickness of 350 μm, which is necessary to give an overall mechanical rigidity sufficient for

manipulation. The N-type or P-type layers needed for the construction of the component, in fact, have a thickness which can vary over a wide range (orders of magnitude ranging from 100 nm to the nearest hundred µm). This thickness, which depends on the role of the layer within the component and also the voltage rating of the device must be controlled precisely. Another important feature if the deposited film is to be controlled finely is its resistivity. In addition to these two quantities, the quality of the crystal layer, must be uniform over the entire surface of the layer. The number of suppliers of epitaxial substrates is smaller than that of simple substrate providers. Some component manufacturers also have their own in-house source.

4.3.1.2.2. Techniques

In this section, we will consider the homoepitaxy of 6H-SiC and 4H-SiC by CVD, which is the only technique used industrially today. We also discuss homoepitaxy of 3C-SiC and the postponement of SiC films on various substrates, for the economic interest they represent, although these processes are still at the research stage.

Homoepitaxy

The technique currently used by industry is the chemical vapor deposition. The growth takes place at a temperature between 1,400°C and 1,600°C, sweeping a gas rich in species Si and C, on a substrate with a disoriented surface from the axis c [KOR 98].

This disorientation of the surface (from 3.5° for the polytype 6H, and 8° for the polytype 4H) provides an homoepitaxial layer without inclusions of parasitic polytypes (epitaxy called “steps control “). The mastery of the process also helps to prevent the increase of micropore densities and other dislocations compared to those of the starting substrate.

The growth rate is relatively low (2 to 5 µm/h) for basic systems, but heavy thicknesses are available thanks to the new hot-wall systems allowing high velocity deposition (50 µm/h).

The unintentional conductivity of the films produced by this process is N type, with a level of residual doping between 10^{13} cm^{-3} and 10^{14} cm^{-3}. The mastery of the resistivity is in a range of 10^{15} cm^{-3} to 10^{19} cm^{-3}, and is produced by the incorporation of the doping impurity in the gas source (nitrogen to get the type N and aluminum for the P-type) during the epitaxy, and control of the mechanism of site competition [LAR 97].

The commercial buildings have improved the uniformity of thickness and doping layers (typically equal to 10% for doping) by rotating platelets in the flow of gas,

while allowing for the simultaneous processing of multiple wafers [EPI 01]. It is worth noting, however, that uncertainty about the actual value of the thickness of a commercial epitaxy remains high (up to 25% if less than 1 µm, and 10% if over 10 µm), and that the constancy of doping throughout the thickness of a layer is not specified. This can be a significant source of error in assessing the performance of a component, in particular whether it should be “high voltage”.

The lifetime of minority charge carriers is a highly sensitive parameter to the purity (structural, chemical) of the semiconductor, and also critical for the smooth operation of bipolar components. The maximum values published for the lifetime of holes in the thick SiC epitaxies have increased in recent years, in agreement with the simultaneous improvement of the quality of substrates and epitaxies, reaching levels in the order of several microseconds [KOR 96]. We will see in section 4.4 that these materials allow for bipolar devices (diodes) with low differential series resistance, and high speed.

The various possible consequences of the present imperfections of epitaxies (mainly induced by the substrate) on the final characteristics of power components are under investigation. Some are already well known, like the premature breakdown of the components due to the micropores, which propagate from the substrate through the thickness of the epitaxial layer. The best current densities of these defects (1 cm^{-2} for substrates of 50.8 mm in diameter, see Table 4.6) already allow for the use of some high-voltage devices sized in the order of 10 mm^2. The polytypes inclusion, or surface defects, will also affect the inverse characteristics (blocking of bipolar junctions or Schottky) or direct characteristics (channel conduction of MOSFET transistors). The frequency of these defects is already relatively low and on the decline. However, the screw dislocations present in much higher densities (also spread throughout the thickness of the epitaxy) worry today’s designers more because of their impact on the current and electrical behavior in the vicinity of the breakdown voltage. While it has changed little in recent years, a dislocation density of less than 1,000 cm^{-2} would be required to obtain power components. It should be noted that the silicon wafers, which are at the foundation of existing devices, have dislocation densities within this order of magnitude.

In addition to a constant search for improving the chemical and crystalline quality of epitaxial films (but first of all through an improvement in the substrates), the concerns of scientists focus on increasing deposit rates, while preserving the control and uniformity of low doping (about 10^{14} cm^{-3}), with the main objective of meeting the needs of power electronics. The technique of chemical vapor deposition at high temperatures (up to 2,000°C), must also be mentioned, with which growth speeds as high as 800 µm/h were obtained [ELL 00].

Other techniques (at the research stage)

Because good quality substrates (6H-SiC, 4H-SiC) are expensive and small (though the latter tends to reduce grievance), or because they are still lacking (as for 3C-SiC), the search for obtaining monocrystalline of SiC films on various other substrates have continued.

Homoepitaxy by heteroepitaxy

The absence of substrates (except of small ones, mainly of 6H polytypes, obtained by the Lely method), largely contributed to research efforts into heteroepitaxy of SiC on silicon, with first interesting results appearing at the beginning of the 1980s [NIS 83]. The obtained polytype was 3C-SiC, which has the lowest disagreement mesh with Si.

The physical properties of this polytype (particularly in terms of mobility of carriers), have kept the interest of this research despite the emergence of 6H-SiC substrates onto the market in early 1990. Today, the main interest of such research into power electronics, while substrates and thin layers of 4H-SiC are available, is primarily economic (reduced cost of silicon and manufacturing stages on this substrate of "standard" size). The 3C-SiC materials owns good factor of merit (as shown in section 4.2) relating to obtaining vertical conduction, and fast devices. Applications outside the field of power electronics (particularly as sensors in hostile environments – temperature, radiation) also contribute significantly to the research efforts.

Due to differences in parameter mesh (of 20%), and coefficients of thermal expansion (8%), the films of 3C-SiC deposited on silicon contain crystalline defects in large quantities, even when a preliminary step known as "carbonization" of the silicon surface is included [MAT 88]. Some of the defects annihilate during growth, and beyond a thickness of about 5 μm, the monocrystal is homogenous, but the density of defects is still about 10^8 cm^{-2}. Growth temperatures of above 1,000°C are necessary to prevent the incorporation of micro-crystals into the layer of SiC. In addition, these films suffer important constraints that curve the substrate, or even cause cracks [CHA 01]. Thus, the electrical characteristics of the layers of SiC-3C are degraded.

Homeopitaxy by postponing thin layers

A more recent form of research, with the same economic concerns, applies the Smart-cut process (developed by LETI/CEA [BRU 95] in conjunction with SOITEC), to provide reports on the surface of a substrate A (preferably low cost and standard dimensions): a thin layer of silicon carbide cut off on the surface of a monocrystalline substrate B. This process was first tried with success from wafers of 6H-SiC on silicon substrates [DIC 96].

The process applied to the silicon carbide is, as a first step, establishing a strong dose of hydrogen on the surface of sample B (SiC), in order to create a weakened plan, to a depth determined by the energy of implantation. The established face of this sample B is then pasted (by molecular accession) to sample A. A proper separation process (e.g. thermal), generally applied, causes a cut in the B sample to the depth of implantation, separating it from the SiC thin film transferred to sample A. Sample B can then be recycled to provide a new film of silicon carbide.

When an insulating gluing interface (for instance, SiO_2 or Si_3N_4, etc.) is used, in order to form a structure called "SiCOI", the target is in addition to combine the advantages of silicon carbide and those of structures on insulator. The purpose (for power electronics) is to obtain lateral power components, or even to have an adaptive technology to achieve power integrated circuits, if the characteristics of the material transferred and of the devices which can be made permit it. The optimization of the process has now reduced the level of compensation for N-type films (resulting from the implantation of hydrogen). At the moment, 6H-SiC or N-type transferred 4H films, used for the creation of components, have a thickness between 0.5 µm and 1 µm, and a concentration of acceptor-type defects of less than 4×10^{16} cm^{-3} [HUG 00].

When a metal interface bond is chosen, the hetero structure is created in the hope of achieving power components with vertical conduction from a "quasi substrate" of cheaper silicon carbide, called "QuaSiC" [LET 01]. The possibility of obtaining a coat of mono crystalline 4H-SiC, 8 µm thick, created by homoepitaxy on a thin film previously transferred on a substrate of polycrystalline SiC (the bonding interface used is WSi_2) has been reported.

4.3.2. *Technological steps for achieving power components*

Once the required piling of thin layers on the substrate, necessary for the achievement of a component (for example: N^- epitaxial growth on N^+ substrate to get a Schottky diode, or P^+ on N^-, on N^+ substrate for a bipolar diode, or P^+ on N on P^-, on substrate N^+ for a thyristor, etc.) has been achieved, a number of technological steps are necessary to complete the chosen structure and allow it to be connected and integrated into a box or a system ensuring its operation.

Two techniques traditionally used for silicon can also be used by manufacturers creating components based on SiC: these are *wet etching* and *doping by localized impurity diffusion* through a mask. Despite these two features, it was not required, in general, to develop specific equipment: the processing of wafers of silicon carbide largely benefited from the know-how and facilities developed, and became the industry standard for silicon (for example, wet etching installation, implementers,

but also oxidation or deposition installations, photolithography, etc.). Other examples are the characterization and analysis techniques that have accompanied them. This has contributed to the rapid progress of research on the components, allowing for the early opportunity to experimentally test most of the known architectures. However, great efforts have been made to develop procedures adapted to the new semiconductor, especially with regard to temperature and duration of treatment (for oxidation and ion implantation, etc.), the chemical nature of the elements (gas, dopers, metals, insulators), which are often redefined and optimized. The small size of SiC substrates also intervened significantly in the development of these procedures. An exception must however be mentioned: the stage of post-annealing used for ion implantation doping of SiC implements specific furnaces, as high temperatures are required.

The following sections will review the key steps for the successful implementation of a power component of silicon carbide, in order to clarify the state-of-the-art features that underlie the performances of modern demonstrators (the results shown are for polytypes 6H and 4H).

4.3.2.1. *Etching*

4.3.2.1.1. Roles and qualities expected

The etching of the semiconductor is an indispensable tool, used for many purposes, such as surface treatment, the attainment of trenches, resuming buried contact, and achieving periphery (mesa), etc. Unlike in the case of silicon (or amorphous silicon carbide), the attack by wet chemistry is ineffective for a material with a high binding energy like SiC (except by molten salt at temperatures above 500°C, using unsuitable techniques for an engraving to be selective, not contaminating the structure, etc.). In the early 1980s the dissolution of this technological blockage contributed, alongside the discoveries of a method of controlled growth (“LELY amended”) and a process of hetero epitaxy for 3C-SiC on Si, to renew interest in this semiconductor. This is due to the advent of plasma etching systems (developed to improve the sharpness of definition of the grounds on silicon), which were used successfully to attack SiC. Good control of the speed of etching, its selectivity towards masks and the state of the etched surface (physical, chemical and morphological) is usually required for this step.

4.3.2.1.2. Techniques and current features

The dry etching simultaneously results from a chemical attack and a physical attack, respectively caused by the presence of neutral reactive species in plasma (fluorine or chlorine, which react with Si, and oxygen that reacts with C, etc.) and ions accelerated to the surface to be etched (Ar^+, etc.). The “high density” etching systems of the latest generation (with a high concentration of ions) allow for etching

speeds of 100 nm/min. These speeds are sufficient to build most of the component structures, provided there is a material masking not eliminated (or distorted) throughout etching SiC. The etching selectivity represents this quality as the ratio of the attack speed of the material to be etched and that of the mask, as presented in Figure 4.5.

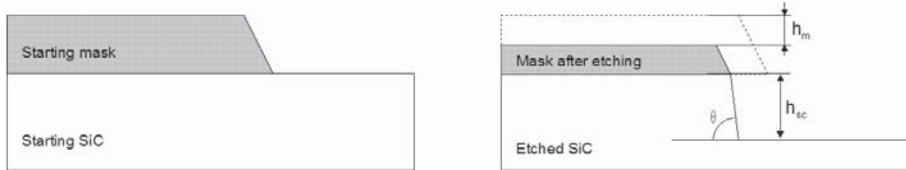


Figure 4.5. *Representation of SiC etching with an angle θ. The mask is represented in gray. After etching, the original mask is represented by the dotted line. Etching selectivity is* V_{sc}/V_m, *with* $V_{sc} = h_{sc}/d$ *and* $V_m = h_m/d$, *for an etching duration d*

The various natures (and *selectivities* of etching) of the most commonly used masks are: aluminum (> 20), silica (from 1 to 6 depending on the quality of SiO_2 and chemical attack process), and resins of photo litho etching (0.3 to 0.4 [MER 01]). The very low speed attack of aluminum compared to that of SiC authorizes deep engravings, with relatively vertical walls. Selectivities much lower (as in the case of SiO_2) can be restrictive in terms of depth of attack, according to the feasibility of filing a thick mask. Nevertheless; they are used for obtaining etching flanks with a slope angle (angles from 30° to 80° from the horizontal, with a depth of etching of SiC of 3 µm [LAN 96]) around 5° tested on 5 µm [MER 01]).

The research focuses on achieving deep engravings, with controlled angle and quality etching flanks.

4.3.2.2. *Selective doping by ion implantation*

4.3.2.2.1. Roles and expected qualities

Selective doping is essential to achieve planar devices (i.e. without relief from the surface of the semiconductor), whether for the creation of emitters P^{++}, grids P, N^{++} sources, contacts (N^{++} and P^{++}), or peripheral protections (P or N^+). For the latter aspect of peripheral protection, the ion implantation is also sometimes used to locally make amorphous the semiconductor surface. Here we will only address the application concerning doping, which is to create boosted regions in a range of concentrations ranging from a few 10^{16} cm^{-3} to 10^{20} cm^{-3}, preserving a good crystalline and chemical quality, in the volume and on the surface.

4.3.2.2.2. Current techniques and features

The ion implantation followed by annealing is the only feasible technique for localy doping silicon carbide (because of the prohibitive temperatures required for doping by diffusion of doping impurities). Typically, the bombing serves to incorporate the ionic doping impurities in the material at a depth dependent on the energy transmitted to the ions, the size of these, the density of the target, and its crystalline orientation from the incident beam. The high density of silicon carbide (see section 4.2.2) will result in shallower penetrations than in the case of silicon with a given implantation energy and impurity, when the direction of implementation is misaligned from any crystallographic axis. Note, however, that the structure of SiC promotes a secondary pipeline, which could lead to the creation of deformed and little steep junctions with a tail of the implementation profile. This phenomenon is more difficult to avoid than in the case of silicon [MOR 99].

Because of the very low mobility of doping impurities in SiC (their coefficients of thermal diffusion being very small), the spatial distribution of implemented impurities is generally not changed during the post-implantation annealing (boron is an exception, which has a circulation assisted by defects), while this phenomenon is often exploited in the case of Si (although also sometimes has detrimental effects). Multiple implantation with high energy (or more rarely intentionally channelled implantations) is usually implemented to achieve junctions or deep boxes (i.e. beyond µm) in SiC.

The post-implantation annealing is nevertheless essential to rebuild the crystal damaged during the ion bombardment, and make the implanted impurity migrate to a site for replacement of an atom of the network, so as to be an electrically active doping. In SiC, some generated defects are particularly stable. Accordingly, it is important to minimize the degree of damage of the crystal. To do so, a hot implantation is generally used when the level of referred doping requires a dose above the threshold which makes the material amorphous at room temperature. It also follows that temperatures during the consequent annealing need to be much higher than those usually used (especially for the P-type doping). These high temperatures (at least 1,700°C for Al) also require good atmospheric control to maintain a suitable surface on the samples. Specific ovens or techniques to the SiC industry are needed for this step.

	N-Type				P-Type	
Nature of impurity	**Nitrogen**		**Phosphorus**		**Aluminum**	**Bore**
Atomic mass (u.a.m)	14.003		30.974		26.982	11.009
Ionization energy (E_A , MeV)	***h***	***c***	***h***	***c***		
for 6H-SiC	81	140	85	135	200-250	285-390
for 4H-SiC	42	84	53	93	191-230	300-400
Ionized impurities at 25°C (for $N_{A,D} = 10^{19}$ cm^{-3} and $N_{comp} = 5x10^{15}$ cm^{-3})	70% (E_A=0.08eV)		#70% (E_A=0.08eV)		2% (E_A=0.2eV)	0.15% (E_A=0.3eV)
Orders of magnitude of the depth of implantation (µm). Examples for:						
– classical energy: 200 keV	0.3		0.18		0.22	0.39
– high energy: 1 MeV	0.92		0.8		0.95	1.14
Threshold to be amorphous at room temperature (cm^{-2})	4 x 10^{15}		~2 x 10^{15}		~10^{15}	5 x 10^{15}
Implantation temperature (°C)	RT – 1000		RT – 600		RT –850	RT – 700
Annealing temperature (°C)	1,300-1,500		1,300-1,700		1,500-1,800	1,500-1,800
Resistance/square (Ω/) (examples, for 4H, at T_{amb})	285 [RAO 98] (N : 2.5x$10^{19}$$cm^{-3}$, thickness: 0.4 µm)		110 [HAN 00] (P: 1x$10^{20}$$cm^{-3}$, thick: 0.45 µm)		285 [KIM 01] (Al : 1.6x$10^{20}$$cm^{-3}$, thick: 0.25 µm)	Very high

Table 4.7. *Characteristic quantities for the doping impurity, doping process, or the layer of SiC implanted and annealed*

Table 4.7 presents the dopings which are currently used by technologists, and some characteristics of impurity, process, or either the implanted and annealed layer. Aluminum and nitrogen are respectively P-type and N-type doping, encountered in the majority of devices because they have low ionization energy compared to other impurities. While the minimum values of the N-type layers resistance implanted with nitrogen are close to the values obtained on Si [RAO 98], those of the P-type layers doped with aluminum remain very high [KIM 01].

For the P-type doping, boron is also used: its small size facilitates its incorporation. The threshold for amorphous is higher and implanted profiles are

deeper for the same acceleration energy when compared with Al, especially since during the post-implantation annealing, this impurity displays the ability to disseminate significantly, beginning at 1,400°C. However, dissemination occurs in all directions, especially to the surface (exodiffusion) [LAU 99], making the control of the incorporated dose difficult [TRO 97]. More rarely, phosphorus is used for the N-type doping, due to the improved values for electron mobility, leading to a lower resistance per square.

Finally it must be noted that an ionization energy similar to aluminum (especially that of boron) leads to an incomplete ionization of doping on a large portion of the range of operating temperatures covered. This represents an additional factor (compared to the case of silicon) and a very important consideration for the prediction or analysis of trends in temperature performance of SiC devices. The bipolar structures with a P^+-type emitter, which is dependent on an efficient injection of holes, are in particular affected by this consideration, as may be found in section 4.4.2.

4.3.2.2.3. Research avenues

The progress to be achieved thus lies in improving control of profiles and levels of doping, especially in the case of strong doping and P-type. From the viewpoint of implantation techniques, research teams work in particular on the implantations at high energy, to reduce damage to the crystal and therefore make it possible to increase the implanted doses [TAK 98]. The co-implantation is also considered to improve the incorporation of Al and B in substitute sites [OSH 01]. Finally, the channelled implantation (oriented along a preferred crystallographic axis) is a line of research seeking to increase the depths of implantation, while reducing damage to the crystal.

From the viewpoint of the annealing process, many studies are conducted to improve the electrical activation of doping and the quality of the crystal, not only in volume but also on the surface. For this, quality depends not only on that of doping, but also the success of subsequent manufacturing steps such as etching or more thermal oxidation. Different techniques (such as, induction furnaces [LAZ 00] or pulsed annealing [PAN 01], etc.) and various configurations of environment of samples were studied.

4.3.2.3. *Oxidation, and deposition of insulation*

4.3.2.3.1. Roles and expected qualities

Different functions involving the presence of an insulator in contact with the semiconductor within the components include passivation and surface protection,

insulation between the electrodes or between semiconductor areas, insulation of command grid, etc.

The silicon industry exclusively uses the product of silicon thermal oxidation, SiO_2 for insulation. The excellent properties of this insulator on silicon (also accessible by certain deposit techniques) have been one of the key factors in the development of microelectronic applications based on silicon. As the thermal oxidation of silicon carbide also produces silicon dioxide, the same functions of insulation and surface passivation are desired for SiC based components. There is therefore much work towards development and optimization, as was the case for silicon. The difficulties encountered today in obtaining good electronic properties at the interface (low charge density and interface statements) are reminiscent of those encountered at the beginning of development for the MOS on silicon.

However, specific features of SiC (its nature or future use) cause new issues to arise, which require research into new methods for making SiO_2, or investigations on other insulators. The current state of knowledge is summarized here. A comprehensive and recent review [RAY 01] on this key issue can be accessed for more details.

4.3.2.3.2. Thermal oxidation (and depositing silicon dioxide)

As with silicon, the chemical reaction (in the presence of O_2, wet or dry, activated by temperatures from 850°C to 1,150°C) leads to a consumption of the semiconductor thickness equal to 45% of the thickness of the resulting SiO_2. As on silicon too, the volume properties of that oxide are a refractive index of 1.45, a very good dielectric strength of 10 to 12 $MV.cm^{-1}$ (if obtained on dry material of good crystalline quality) and a low resistivity in the field of 10^{14} $\Omega.cm^{-1}$. We can therefore consider this technique in terms of the same goals, namely mainly cleaning and polishing the surface by sacrificial thermal oxidation (for manufacturing techniques) and creation of an insulator (at component level, as isolated grid or protection of surface or insulation cabinet, etc.).

Note however that the use of SiO_2 as insulation on SiC must take into account that the maximum values of the electric field, inside a component that are optimized to take advantage of the strengths of silicon carbide, become similar to the magnitude of the breakdown field of SiO_2. This is a new situation for the designer accustomed to the values of electric fields in Si, which remain some 20 times lower than the critical threshold for SiO_2. This will also have repercussions on the architecture or on conditions of use of components employing SiO_2 as insulation.

Among the differences affecting the technological level, the first to be reported concerns the kinetics of oxidation which is much slower for SiC than for Si (for example, in the order of 10 nm/h by dry oxidation at 1,150°C, and for Si in the order

of magnitude of 300 nm/h by dry oxidation or 4 µm/h during wet oxidation at 1,100°C), which will restrict the ability of this process to achieve preferably thin oxides, such as grid oxides or primary passivation. While remaining of the same order of magnitude, speed of growth of the oxide on a given polytype of SiC varies significantly depending on the crystalline orientation of the surface (kinetics is the fastest on face Si, slowest on face C, and intermediate on the other sides), and its level of doping. Note also that a damaged crystal (for example, by an ion implantation) oxidizes more easily than the blank crystal, in particular the oxidation of amorphous silicon carbide is much faster than mono crystalline SiC. To obtain relatively thick layers or uniform thickness over a surface with regions of different types, processes for implantation of SiO_2 previously developed for Si are used (for example, to make ion implantation masks or plasma etching).

The second difference is a current difficulty that exists when dealing with the quality of the interface between SiO_2 and SiC. This is lower than that obtained on silicon, in terms of effective charge density and the density of interface states, as well as potential fluctuations in the interface, this includes the quality of "first choice" commercial material. These three quantities (the values still widely dispersed) are indeed usually greater than those obtained today with silicon. Wet oxidations at a temperature exceeding 1000°C and some processing of the surface before oxidation, and annealing after oxidation, have recently helped to reduce them [LIP 98]. In general, it is noted that oxides on the silicon face of SiC exhibit an effective charge density lower than that of the carbon face (best value: $2x10^{10}$ cm^{-2}). The density of interface states, remains currently higher on the 4H-SiC polytype [AFA 00] (around 10^{12} $cm^{-2}.eV^{-1}$). And what is more, implanted P-type materials are penalized even further. Now the MOSFET in 4H-SiC with N channel inversion in an implanted P box is expected to be "flagship" structure achieving SiC transistors (as shown in section 4.2.3.2). Apart from non-ideal threshold voltages, these structures suffer from an apparent mobility of the electrons in the channel inversion, well below its theoretical value of temperatures around 150°C (the gap is reduced when temperature increases). The channel mobility of electrons is generally less than 25 $cm^2.V^{-1}.s^{-1}$ for SiC-4H at room temperature, while being two to three times greater for SiC-6H. The interface statements of acceptor type located at energy levels very close to the bottom of the conduction band [SCH 99], as well as the sharp fluctuations of the surface potential [OUI 97], seem to be recognized today as contributing to the high resistivity of the inversion channel. The deposited oxides do not solve this major problem (which is explained by, and confirms, the fact that the disorder derives mainly from the interface rather than the volume of insulation).

A third difference lies in the values of height barrier potential between the conduction bands of SiO_2 and the semiconductor, which are much lower with SiC than with Si (the same is true among their valence bands), as shown in Figure 4.6. These values, which are reduced when the temperature increases, facilitate the

injection of carriers in the presence of an electric field. The undesirable consequences manifest in terms of the reliability of MOSFET structures, which is increasingly affected while the operating conditions are expected for use at high temperatures, and while this architecture of the component does not preserve the oxide from the large electric fields, that can handle silicon carbide. In addition, the current crystalline quality of substrates and epitaxies of SiC is probably still the cause of premature breakdowns of SiO_2 on SiC, under strong field and high temperature (as was formerly the case with silicon), also leading to reduced MOSFET structure lifetimes on SiC compared with those on silicon.

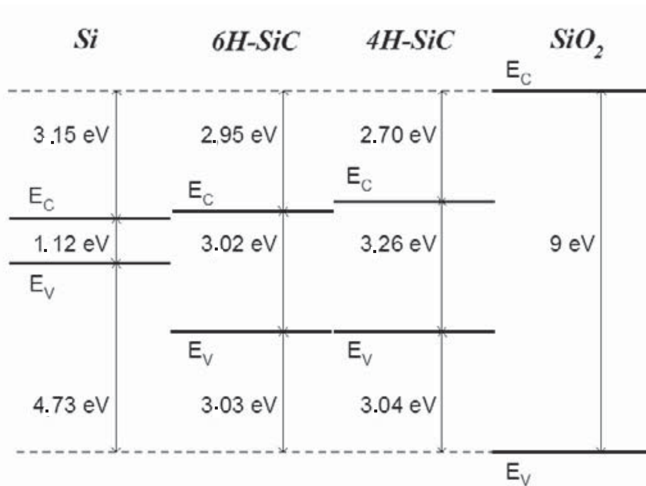


Figure 4.6. *Diagrams of energy band at 300 K for Si, SiC-6H, 4H-SiC and SiO_2 showing the reduction in height of the barrier when the gap of the semiconductor increases, facilitating the injection of carriers into the insulation [AGA 97]*

The physical nature of elements at the root of these electric events (for example, disorder at the interface, or low lifetime, etc.) is not fully clarified (for example, SiC crystal purity, clusters of carbon and surface roughness). A significant part of current research is trying to elucidate this [AFA 99] [AMY 01], and offers treatments [RAI 01] [KRA 01] in order to obtain a SiO_2 film quality compatible with the expected performance of power MOSFETs based on SiC. Without further delay, work is also focused on the architecture of the component itself, in order to circumvent this difficulty (examples will be provided later on in this chapter). At an intermediate level, some research, described below, is focused on alternative insulation that would allow the achievement of insulations for grid control or surface passivation better suited for SiC material.

4.3.2.3.3. Other insulators

A triple stack of oxide and silicon nitride (ONO) is the only insulation currently discovered that leads to both a significant improvement in the threshold voltage, and in the lifetime at high temperature (ten days at 335°C) under a grid field of 2 MV/cm for MISFETs (horizontal structure on P epitaxy, with source and drain implanted in nitrogen). The breakdown electric field of the insulation is also higher (14 MV/cm) [LIP 00].

Some groups are interested in AlN, because of its dielectric permittivity which is similar to that of SiC, and a theoretical breakdown field in the same order of magnitude as SiO_2 (very high). A1N also has a good agreement of mesh with SiC, good thermal conductivity, and a good temperature strength. The maximum electric field of breakdown is currently measured at 3 MV/cm (by MOCVD filing), however, the experimental leakage currents remain prohibitive [LEL 00].

4.3.2.4. *Metallization*

4.3.2.4.1. Roles

During manufacturing of the component, metal depositions may take place (to make etching, or implantation masks, etc.). In the finished component, metals deposited on the semiconductor are intended to provide either an electrical connection with ohmic contact, or a junction via Schottky contact. Placed on top of an insulator, they can also take the role of the grid driving the switch; field plate, for the peripheral protection of a junction; or an interconnection path. We present here only the state of the art of features of ohmic contacts and Schottky on SiC, whose properties (e.g. height of barrier and thermal stability, etc.) are dependent on the state of the interface metal/SiC, and on the nature of metals and reactions.

4.3.2.4.2. Schottky contacts and current features

As recalled in Figure 4.7a, the junction between a metal and a semiconductor produces a potential barrier, called the Schottky barrier Φ_B, which may display a rectifying behavior. A low doped semiconductor, moreover presenting a large gap, promotes obtaining a rectifier contact, also known as a Schottky contact (case of Figure 4.7b). In this way, many metals form a Schottky contact simply by layering upon SiC.

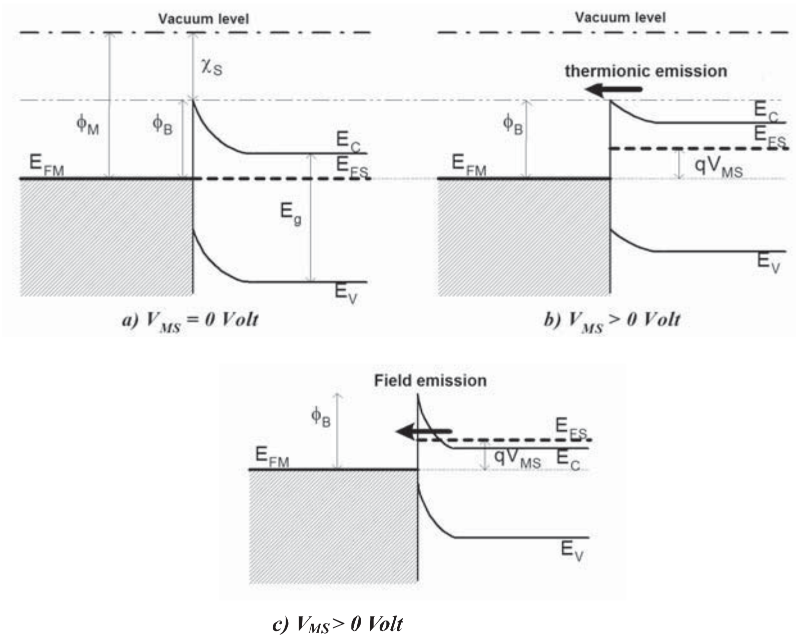


Figure 4.7. *Diagrams of energy band of a metal/semiconductor contact:*
a) Ideal case of a Schottky barrier, such that $\Phi_B = \Phi_B - \chi_S$
b) Schottky contact on lightly doped n-type semiconductor: only the electrons able to overcome the barrier height will participate to the current flow
c) Ohmic contact on highly doped n-type semiconductor: electrons flow across the thin barrier by tunnel effect

The height of the barrier Φ_B depends on the nature of the deposited metal, on the semiconductor (since ideally the barrier is equal to the difference between the work output of metal, Φ_M, and the electronic affinity of the semiconductor, χ_S, according to the Schottky-Mott relationship) and also on the chemical and structural condition of the semiconductor surface (of the polytype, its surface orientation – face C, face Si, or another face; the presence of a native oxide; or surface graphitization, etc.).

The experimental results show that Φ_B depends on Φ_M less than is expected by the theory. The summary of results on N-type, obtained in 1995 by Porter and Davis [POR 95], shows a range of values between 0.8 and 1.25 eV on SiC-6H (0001) – Si face, and between 1.0 and 1.6 eV on SiC-6H (0001) – C face, for all metals: Au, Al, Ag, Ti, Pd, Mn, Mg, Hf, Co, Ni. It was shown that the presence of surface conditions inside the forbidden energy band (intrinsic to the surface or induced by metallization) influences control of the Schottky barrier height, moderating the

influence of output work. The semiconductor surface preparation stages before metal deposit, the parameters of this deposit and the quality of the SiC material are all crucial for the result and reproducibility of rectifier contact.

Ni is the most commonly used metal for the production of prototypes based on N-type rectifier contacts in 4H SiC because it has a high output work, leading to a barrier height of 1.24-1.29 eV on a 6H-SiC silicon face (after sacrificial oxidation of the surface and pre-annealing under ultra-vacuum [WAL 93]). Barrier height is equal to 1.6 eV on 4H-SiC (after chemical cleaning and cleaning *in-situ* before filing under ultra-vacuum), this increases by 0.23 eV after annealing at 700°C for 10 min; these works also relate to an ideal ratio of 1.1 [KES 00]. Titanium is the second most commonly used metal for obtaining Schottky contact on a N-type, leading to a rectifier contact coefficient ideally close to 1. The height of the barrier is 0.95 eV on 4H-SiC face Si (for a deposit after wet chemical cleanings) [ITO 97]. A change in barrier height, from 0.88 eV to 1.08 eV, was reported on 6H SiC-N-type after annealing at 700°C for 1 hour (linked to the changing nature of the interface metal [POR 95]).

The leakage currents in reverse polarization are higher than projected in the theory of simple thermo ionic emission. In addition to the possible participation of localized defects, or suburb effect, the contribution of a thermo ionic emission assisted by the field has been researched [HAT 02].

Works on SiC Schottky contacts of P-type are infrequent, given the rare need for this type of contact by applications. Barrier heights higher than those of the N-type are reported for SiC-6H (1.45 eV to 2.56 eV for Au, Ni, Pd, Al, Co, Ag, Ti, Cs, Mg face Si [ITO 97]), with ideal rectifier contact factors of greater than 1, showing that thermo ionic emission is not the predominant mechanism for conducting the current.

Current research is focused on optimizing manufacturing processes (by monitoring influence of surface pre-treatments [MOR 00], and type of metal [HAT 01], etc.), mainly in terms of temperature stability, quality and consistency on the large surface of the interface metal/SiC of P-type.

4.3.2.4.3. Ohmic contact and current features

Achieving a metal/SiC contact with good ohmic properties requires the reduction of heights of Schottky barrier (usually obtained by annealing at relatively high temperature), and high levels of doping (in order to improve current conduction via the tunnel effect through the barrier, as shown in Figure 4.7c, with the example of a N degenerated semiconductor).

On the areas of N-type SiC, nickel is often chosen as a demonstrator. It is deposited at room temperature and annealed at approximately 1,000°C for a few

minutes, enabling the creation of a layer of silicide Ni_2Si at the interface (this reaction consuming Ni and SiC in a ratio of 1:1), and others (such as the migration of C far away from the interface), are all necessary for lowering the height of the Schottky barrier (equal to 0.35 eV on 6H SiC). The lowest specific resistance of contact for Ni/SiC-6H or -4H is about 10^{-6} Ω.cm^2 at room temperature for doping greater than 10^{19} cm^{-3} [CRO 97]. The physical and electrical stability of this contact is appropriate for long-term uses at temperatures below 500°C (Crofton *et al.* did not observe evolution of specific contact resistance after 300 hours at 650°C; instead resistance increases with temperature [CRO 95]).

On SiC P-type regions, aluminum produces both a reasonable specific resistance (about 10^{-3} Ω.cm^2 on 6H material moderately doped at 8x10^{18} cm^{-3} [ADA 94]) and a low depth of reaction in the semiconductor. Annealing at relatively high temperature (800°C) during several minutes of aluminum (or one of its alloys) allows Al to disseminate superficially in SiC, which increases the doping on the surface, thus promoting ohmic properties of contact. The film of aluminum must be "encapsulated" (usually with Ti, and possibly Pd), to withstand such annealing temperatures and avoid the formation of an insulating layer on the contact surface. Proper dosage of the layer and very good control of the annealing conditions are essential to control the various reactions involved, and therefore the quality and reproducibility of this type of ohmic contact [NOR 96].

The recent feasibility of higher levels of doping (above 10^{19} cm^{-3}) has reduced the specific resistance of contact on P-type SiC, down to 10^{-4} Ω.cm^2 for contacts based on annealed Al, and annealed or non-annealed Mo, Ta, Ti, and Pt [CRO 97]. Values of a few 10^{-5} Ω.cm^2 were also reported with, for example, Ti annealed at 800°C for 1 min on SiC doped at 10^{19} cm^{-3}. In publications specifically dedicated to the experimental evaluation of SiC demonstrators, metallization on anodes or P-type grids remain the most often-based annealed Al-Ti (for research into employment of annealed titanium or platinum see [SIN 01]).

Current research attempts to better understand the nature of the interface and develop processes to solve disadvantages: such as, low Al grip on SiC, SiC consumption that can be crippling in implanted or epitaxied areas with little depth (TaC is proposed on 6H SiC N-type [JAN 00]); and quite high annealing temperatures and stability in high temperature, etc. Mastering high level doping (especially by ion implantation) is also a crucial factor influencing the progress of research into ohmic contact on P-type.

4.4. Applications of silicon carbide in power electronics

4.4.1. *SiC components for high frequency power supplies*

As previously explained (see section 4.2), the physical properties of silicon carbide contribute to the simplification of the compromise between on-state low voltage drop and switching speed, that the designer has to face when choosing a switch, or a diode, when the voltage is imposed by the target application. Due to its operating principle and its relative simplicity, the Schottky diode is the first component that should succeed in demonstrating this potential.

4.4.1.1. *SiC Schottky diodes in 4H N-type*

These were the first SiC power device to lead the market. An initial marketing announcement was made by Microsemi in 2000 [MIC 00] (in association with the supplier of substrates Sterling Semiconductor [STE 01]), this was followed by a second announcement made by Infineon Technologies AG in 2001 [INT 01].

4.4.1.1.1. Marketed diode specifications

The updated basic specifications of some of these devices are displayed in Table 4.8.

Changes in the temperature of direct and reverse electrical characteristics are shown in Figure 4.8, using reference SDP06S60 as an example extracted from the publication of Kapels *et al.* [KAP 01]. The specific on-state differential resistance R_{on}, is indicated for 25°C equaling 0.9 mΩ.cm^2. We conclude that the nominal current of 6 Amps corresponds to a high current density (about 400 A.cm^{-2}) for a direct voltage of 1.5 V, at 25°C. R_{on} increases with temperature, as do leakage reverse currents.

Features	UPSC600[MIC 00]	SDP06S60[INT 01]	SDT12S60[INT 01]
Rated current (I_F)	1 A (75°C)	6 A (100°C)	12 A (100°C)
Reverse voltage (V_{RRM})	600 V	600 V	600 V
Max overload current. (I_{FSM})	10 A	21.5 A	120 A
On-state voltage (V_{on})	1.3 V (1 A / 25°C) 1.6 V (1 A / 150°C)	1.5 V (6 A / 25°C) 1.7 V (6 A / 150°C)	1.5 V (12 A / 25°C) 1.7 V (12 A / 150°C)
Capacitive charge	-	21 nC (400 V / 6 A / 200 A/µs / 150°C)	30 nC (400 V / 12 A / 200 A/µs / 150°C)
Total capacity	15 pF (200 V / 1 MHz)	15 pF (600 V / 1 MHz)	43 pF (600 V / 1 MHz)
Reverse current (I_R)	20 µA (600 V / 25°C)	20 µA (600 V / 25°C) 55 µA (600 V / 150°C)	40 µA (600 V / 25°C) 100 µA (600 V / 150°C)
Max. junction temperature (T_{jmax})	150°C	175°C	175°C
Thermal resistance (R_{th})	30 K/W (Junct-Tab) 10 K/W (Junct-Bot)	62 K/W (Junct-amb)	62 K/W (Junct-amb)

Table 4.8. *Typical electrical characteristics of marketed Schottky diodes in 4H-SiC*

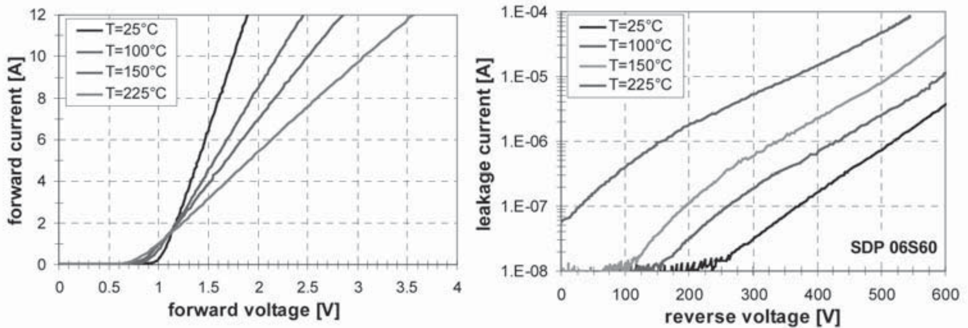


Figure 4.8. *Direct and reverse features of a SDP06S60 depending on temperature (figure extracted from [KAP 01])*

Opening switching of the Schottky diode is a mechanism of capacitive load (the capacity of the junction which switches off). The movement of the charge of desertion creates a reverse peak current at blocking, that is independent of

temperature, and at the rate of decay of the current in the diode (e.g. -3 Amps for a direct current of 4 Amps switched under -300 V).

4.4.1.1.2. Other results on high-voltage SiC Schottky diodes

Prototypes of 4H-SiC at much higher voltage than 600 V were made by different laboratories: with Infineon Technologies already planing to extend its range up to 3.3 kV.

Table 4.9 brings together a number of best results, showing breakdown voltages around 4 kV, specific on-state resistances (at 25°C) of between 2 and 6 mΩ.cm^2 for structures up to 1,700 V, and between 14 and 34 mΩ.cm^2 beyond. The leakage currents at 25°C, for a reverse polarization close to the breakdown voltage, are high.

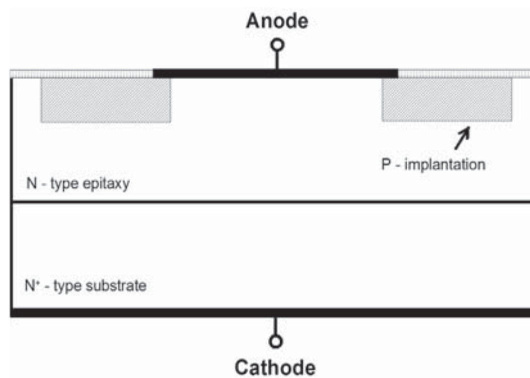


Figure 4.9. *Schematic of the structure of a Schottky diode on SiC type N, with a peripheral protection device implanted as a P-type pocket*

The peripheral protection (necessary to reduce electric field reinforcements on the peripheral of the junction) is provided by the field plate, or more frequently (on latest structures) by being implemented a P-type pocket (or junction termination extension, JTE), as shown in Figure 4.9.

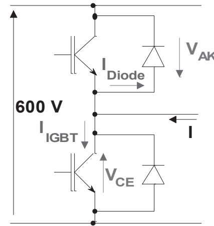
Structure passivation protection reference	**Doping / thickness of voltage strength layer** **(cm^{-3}/µm)**	**Anode section** **(cm^2)**	**Reverse voltage strength / Temp.** **(V/°C)**	**Direct voltage / current density / temp.** **(V/A.cm^{-2}/°C)**	**Specific differential series resistance / temp.** **(mΩ.cm^2/°C)**	**Current density / reverse voltage / temp.** **(µA.cm^{-2}/V/°C)**
Ti/N$^-$N$^+$ Polyimid/SiO_2 JTEepi + mesa [TEM 01]	1x10^{16} /6	0.015	600/25	1.1/100/25 1.5/533/25	- / -	6x10^3/500/25
Ni/N$^-$N$^+$ Pl. of field [KIM 98]	6x10^{15} /22	-	910/25	1.63/100/25	2,6/25	4x10^5/800/25
Ni/N$^-$N$^+$ Pl. of field [KIM 00]	3-5x10^{15} /8-10	7x10^{-4}	800-1000/ 25	- / - / -	4-6/25	0.2/100/25
Ti/N$^-$N$^+$ photoimid JTE [PET 01]	5x10^{15} /13	0.1	1200/25	1.7/250/25 2.3/250/125	3/25 6/125	40/1200/25 120/1200/125
Ti/N$^-$N$^+$ JTE [PET 01]	2,5x10^{15} /15	0.1	1700/25	2.3/250/25 3.4/250/125	5/25 10 /125	1500/1700/25 4500/1700/125
Ni/N$^-$N$^+$ JTE [TSU 01]	3x10^{15} /27	0.008	2400/25	2.7/100/25	13.8/25	0.1-1000/ 600/25
Ni/N$^-$N$^+$ Pl. of field [KIM 98]	1x10^{15} /42	-	2800/25	- / - / -	34/25	0.7/1000/25-
Ni/N$^-$N$^+$ SiO_2 Pl. of field [WAH 00]	7x10^{14} /43	7x10^{-4}	3850/25	4.4/100/25	30/25	1.7/2000/25

Table 4.9. *Major technological and electrical characteristics of various Schottky diodes demonstrators, at high-voltage, on SiC-type 4H N*

4.4.1.1.3. Comparison with silicon

The competing silicon structures in the 300 V range and beyond, are bipolar diodes. The superiority of the Schottky diode (even over an ultra-fast silicon diode) is due to the lack of stored charge when conducting. For this reason, there is no recovery at blocking. It is important to note that the equivalent junction capacitance of a Schottky diode is independent of the direct switched current density in the structure and is insensitive to

temperature rise (as opposed to the bipolar diode reverse capacitance, dependent on the stored charge, i.e. forward bias and operating temperature). However, it is greater than the charge of displacement of a silicon bipolar diode of the same voltage range by a factor equal to the ratio of the critical electric fields of both materials. A reduction of the section of the component is then necessary to limit the junction capacitance (to compromise with the performances for electrical and thermal conduction).



(a) With bipolar silicon diode (b) With SiC Schottky diode

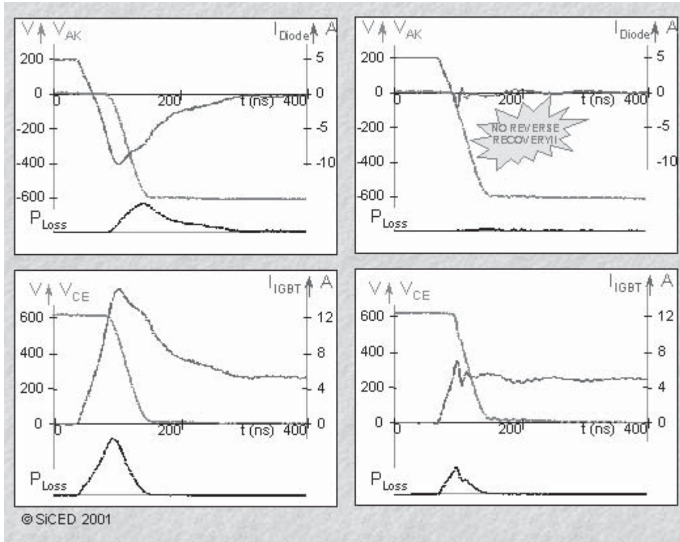


Figure 4.10. *Comparison of the current and voltage waveforms of the diode and the associated switch in assembling a chopper, powered under 600 V, providing a current load of 5 A. Diode voltage rating: 1,200 V [SICe 01]*

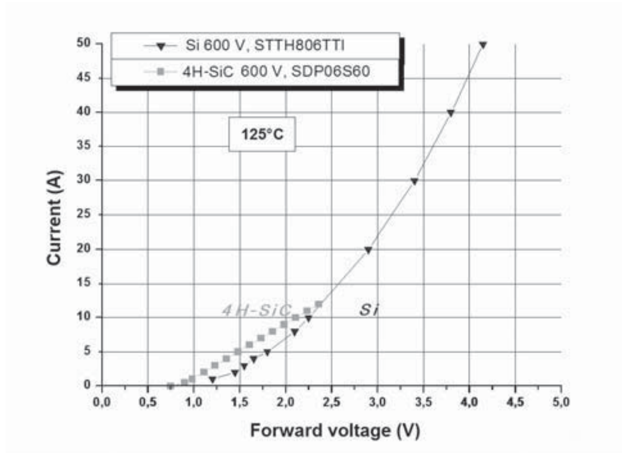
The impact of switching times, on the constraints of over-current and over-voltage, and especially on switching losses for the associated switch of the diode is clearly displayed in Figure 4.10 (extracted from [SICe 01]). This figure provides a comparison of the current and voltage waveforms of the diode and the IGBT partner switch in an inverter, powered under 600 V and providing a current load of 5 A.

The graphs on the left correspond to the result of the use of a bipolar silicon diode, while the graphs on the right display results for a 4H SiC Schottky diode. The voltage rating of the diodes is 1,200 V.

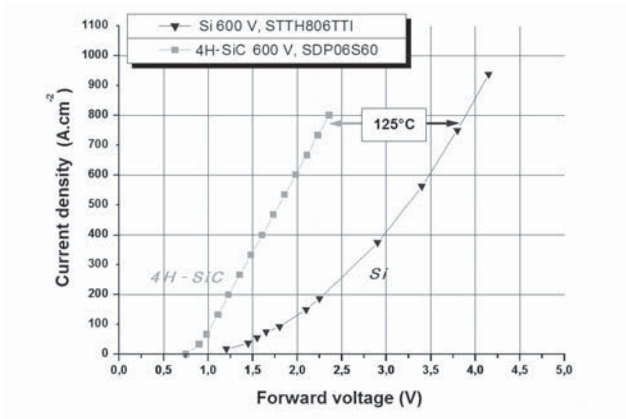
The impact on switching time and the associated losses can allow an increase in the maximum operating frequency of the power supplies, this is useful for reducing the dimensions of the inductive and capacitive elements involved.

The impact on efficiency and on the possibility of reducing cooling systems, depends on the balance between switching losses and conduction losses of the diode. Figure 4.11 compares the Schottky diode, 600 V/6 A in SiC (SDP06S60), with a silicon diode, 600 V/8 A ultra-fast (STTH806TTI); in terms of terminals voltage depending on the current, and in terms of current density. For the $J_d(V_d)$ characteristic of the silicon diode, the average current I_{Fav} of the data sheet of the manufacturer is assumed to have a current density of 150 $A.cm^{-2}$. The SiC diode is assumed to have a nominal current, I_F, density of 400 $A.cm^{-2}$. The direct characteristics $I_d(V_d)$ at 125°C reported here are rebuilt from the data sheets of these two products ([STM 01] [INT 01]). Figure 4.11 shows that at a 125°C junction temperature the voltage across the SiC diode is lower than that of its competitor for a same current. This is true until the current is less than the current I_C (point of intersection of compared characteristics), in this case equal to 12 A. Note that an increase in operating temperature of the SiC diode (T_{jmax} is equal to 175°C) to 150°C will favor the silicon diode silicon, while I_C is slightly reduced to 10 A. In contrast, a decrease in the junction temperature of the two diodes will contribute to increasing the SiC diode by the value I_C.

Therefore, improvement of conduction losses can also be obtained by the choice of a SiC Schottky diode as an ultra-fast diode, for applications where the direct current passing through the diode is less than I_C, in other words when the average current I_{Fav} and the duty cycle δ of the diodes conduction have the relation: $I_{Fav} < I_C.\delta$. This gain is highly dependent on conditions of use (T_j, δ, I_F), is less spectacular than the gain on switching losses, and will be reduced when the required holding voltage increases.



(a)



(b)

Figure 4.11. *Comparison of the typical direct characteristics of two 600 V ultra-fast diodes in competition: the Si bipolar diode STTH806TTI (from the manufacturer catalogue, assumes 8 A corresponds to 150 A.cm^{-2}) and the Schottky diode in 4H-SiC SDP06S60 (from the manufacturer catalogue, assumes 6 A corresponds to 400 A.cm^{-2}): (a) characteristics I_d-V_d; (b) characteristics J_d-V_d*

In the forward state, the high-voltage SiC Schottky diode differs from the bipolar silicon diode via its differential resistance and a positive temperature coefficient. The SiC Schottky diode is an advantage for release in parallel obtaining high current ratings (which is also an answer to the current problem caused by the small size of chips). This SiC Schottky diode is not, however, as effective as the bipolar diode when operating in a regime of over-load current: the surge of direct voltage in the

case of unipolar device leads to a self-heating of the material, which can lead to destruction (by environmental degradation of the SiC chip, including metallizations). This is a limitation on the I_{FSM} characteristic [RUP 00].

We should note, finally, that the gap between the diode in 4H-SiC 600 V and its silicon rival is much more important in terms of current density than in terms of current, for a given direct voltage drop (and a given temperature) (see Figure 4.11). The manufacturer's choice to use of the 4H-SiC diode refrains from exploiting this advantageous characteristic seriously limiting the size of the silicon carbide component, due to the already mentioned compromise between conduction performance (V_F, I_{FSM}, R_{thja}) and commutation performance (charge of desertion). The choice probably also reflects a cost constraint. The current surface price of a silicon carbide component is indeed high and increases with its size (because of substrate cost and the density of defects that they contain, both of which are very important).

4.4.1.2. *Example of application: the power factor correction*

The availability of commercial SiC Schottky diodes led to research into their implementation and their contribution at the system level. The function of power factor correction (PFC) is an example generally retained to assess the interest of a SiC Schottky diode and its field of application. This function is essential for all equipment connected to the alternative network and requiring a continuous supply, which, for example, includes computers. The "boost" circuit type in continuous conduction is the most interesting technical solution, its setback being losses caused by the opening of the diode, which is done under strong current (hard switching).

Various studies implementing the product of reference SDP06S60 in a PFC with output voltage of 380 V for a range of frequencies from 100 kHz to 500 kHz, agree on the following comments:

– At approximately 100 kHz, the PFC circuit with a 4H-SiC Schottky diode does not improve significantly in terms of total losses in semiconductors (diode + transistor) compared to the use of a (less expensive) Si ultra-fast diode, or even a slow Si diode combined with a circuit for commutation aid (snubber) [BEN 01].

– The SiC based solution is justified when using a higher frequency. Indeed, the efficiency almost does not change when the frequency increases from 100 kHz to 500 kHz for the circuit using SiC Schottky diode, although it falls very quickly when a silicon bipolar ultra-fast diode (examples: STTH806TTI or MURH860) is used. The MOSFET switch used in this study [KAP 01] is the silicon CoolMOS SPP20N60C3. The main advantage is obtained at the level of inductive components: it was shown that the operation of a 400 W PFC circuit at 500 kHz with a SiC

Schottky diode and a Si CoolMOS, compared with the same circuit at 140 kHz with a more conventional diode and switch, requires an inductance with a diameter divided by 2, and an overall cost reduced by 8% (the division by 3 of the cost of the PFC inductor erases the increased costs of the SiC diode). Note that the comparison is made with the same cooler and with comparable filters against electromagnetic interference (EMI).

Additionally, the gain in terms of switching losses in the cell can be utilized not only by increasing the frequency: but alternatively by reducing the section of the switch; by reducing the complexity of the system; by reducing the cooler; or by raising the temperature, etc. The designer is vigilant when creating the system, basing the design on the determination of losses (by simulations and/or measures). This becomes particularly difficult with the reduction of switching time (around ten nanoseconds), and the exacerbated influence of the parasitic elements of the circuit. Design tools (and measures) still require improvment in order to be able to report accurately on all the elements of this system, like current and voltage waveforms, and the various couplings (electrical, thermal and magnetic).

In the example considered above, the transistor associated with the SiC Schottky diode was in silicon, because at the moment, no silicon carbide switch is available on the market. We will present the new technology, using explanatory examples of demonstrators currently being developed by various research centres.

4.4.1.3. *High-frequency SiC power switches*

As with the Schottky diode (and following a "silicon logic"), theoretical analysis predicted the silicon carbide MOSFET with N inversion channel as the high frequency and high voltage switch (up to 3 kV at least) of the future, and research largely focused on such structures. Although prototypes have already helped to overcome the limits imposed by the silicon diode by reducing the on-state resistance for a given blocking voltage, SiC MOSFET is slow to keep its promises and to fully emerge as a commercial product. It remains a deeply researched option. Research tries to clarify and eliminate the causes of SiC MOSFETs current performance-cons (described in section 4.3.2.3). These difficulties have promoted the proposal of other unipolar structures to ensure the function of high voltage fast switching.

4.4.1.3.1. Silicon carbide MOSFET transistors with a N inversion channel

As was the case for silicon, the first published structures of power SiC are etched structures, not "V" structures (as with the first Si VMOSFETs), but "U" structures, to underline the form of trenches where the isolated grid command is located, in the UMOSFET switch, and where an inversion channel will be formed (see Figure 4.12). These trenches surround the P regions, through a layer which may have been created earlier by epitaxy on the N layer of voltage holding the component.

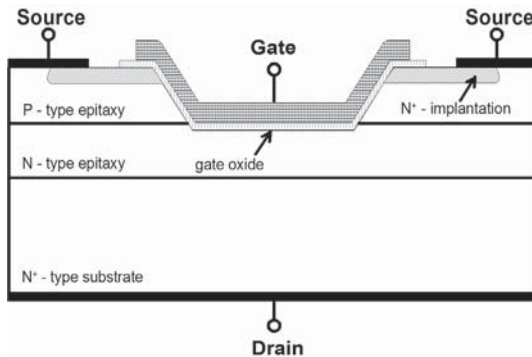


Figure 4.12. *Schematic of a silicon carbide UMOSFET cell*

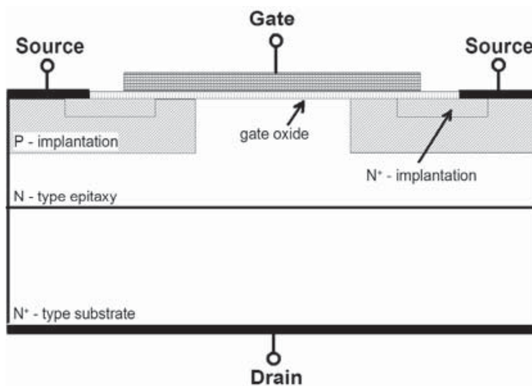


Figure 4.13. *Schematic of a silicon carbide DIMOSFET cell*

With the progress of P-type doping, plane structures (which are generalized in the silicon industry, as better suited for high voltage), have been carried out in SiC by double (or triple [SCH 00]) N epitaxy locations. Figure 4.13 shows a DIMOSFET structure, which requires a first implantation (or two) for the creation of P areas upon which the inverting canal will be induced, and a second implantation for the creation of strongly doped N^+ type sources. This last step also appears in the manufacturing process of the UMOSFET. The two architectures are also based on a heavily doped N^+ type substrate.

Table 4.10 shows results for the SiC MOSFET whose on-state specific resistance is less than the theoretical limit set for the silicon (25°C). The best performance is obtained on 6H-SiC, while the worst was obtained on 4H-SiC

(despite the fact that the latter has a lower theoretical resistivity of drain layers (see section 4.2.4.2). This indeed reflects a limitation of conduction by the inversion canal area (where the problem of an apparent low mobility of electrons has been transferred, see section 4.3.2.3).

Structure Polytype reference	**Doping / thickness of voltage strength layer** **(cm^{-3}/µm)**	**Sec-tion** **(cm^2)**	**Voltage strength** **(V)**	**Direct voltage strength / current density** **(V/A.cm^{-2})**	**Specific differential series resistance** **(mΩ.cm^2)**	**Effective mobility of channel** **($cm^2.V^{-1}.s^{-1}$)**
UMOSFET 4H [PAL 96]	- / -	-	260	2.65/200	18	-
DIMOSFET 6H [SHE 97]	1,7x10^{16} /10	-	510	6.5/100 at V_{GS}=30 V	66 at V_{GS}=30 V	17
UMOSFET 4H [AGA 98]	2x10^{15} /12	0,0015	1400	8/100 *at 100°C* and V_{GS}=26 V	74 at V_{GS}=26 V	7 *at 100°C*
UMOSFET 4H [SUG 98]	10^{15} /25	-	1400	- / -	311	-
DIMOSFET 6H [SCH 00]	9x10^{15} /12	0,0047	1800	5/100 at V_{GS}=10 V	46 at V_{GS}=10 V	15

Table 4.10. *Major technological and electrical characteristics of the best MOSFET transistor demonstrators in SiC-6H high-voltage, and 4H Channel N, at 25°C (temperature indicated if other)*

The most interesting prototype is the plane structure 6H-SiC with a direct keeping voltage 1,800 V (section equal to 0.47 mm^2), a threshold voltage of 4.8 V at room temperature, and an on-state specific resistance of 46 mΩ.cm^2 (of which 36% would be induced by the channel) for a command voltage, V_{GS}, of 10 V [SCH 00].

4.4.1.3.2. Accumulation MOSFET transistors and JFET transistors

Such structures no longer rely on the control of current passage in the N inversion channel (created in a P area), instead they rely on the N accumulation channel or N pre-formed "channel" (in the N layer). The field-effect allowing control of the resistivity of this channel is induced by a MOS grid or bipolar junction. As presented in Figures 4.14 and 4.15, a layer of type P^+ delineates the

channel area. It ensures the full control of conduction in the case of JFET. It also participates in the case of Accu-MOSFET, where it helps to protect the grid insulation against the strong electric fields present in the silicon carbide. According to the depth and the doping of the superior N layer (of the channel), the device is normally opened (the usual case for users of silicon power transistors) or closed.

Table 4.11 shows the result of the main experiments recently published, showing that the specific conduction resistance, R_{on}, is lower than those obtained for silicon components of comparable voltage strength. The best current characteristics in terms of low on-state resistance and high voltage strength, correspond to a 1,800 V JFET with a R_{on} of 14 mΩ.cm^2 at 25°C [FRI 00]. This unipolar component, normally conducting, has a dependence on temperature for R_{on} proportional to $T^{2.58}$, which leads to a decrease in the passing current, under constant polarization due to self-heating.

This feature allows the setting of chips in parallel (as is the case with any MOSFET, and as previously mentioned for the SiC Schottky diode). This property is important considering once combined with the robustness of silicon carbide at high temperature, it can be used to satisfy a function of current limit.

Due to the availability of normally conductive unipolar transistors a revision of conventional electric schematics is required: this may be restricted to the component (for it to operate as a normally open-switch, such as SEJFET, for "Static Expansion JFET" [ASA 01]), or on a more global circuit level. Infineon Technologies offers such an association of "Cascode" type of a 1,800 V JFET controlled by a 60 V silicon MOSFET [SICe 01].

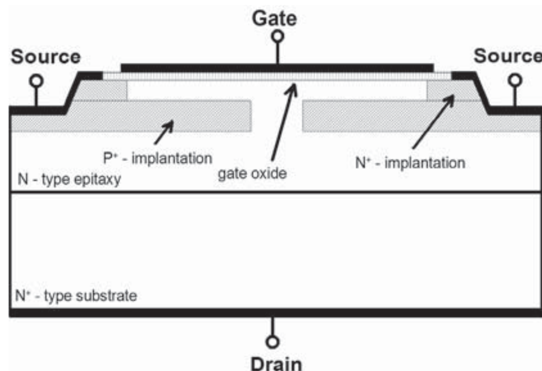


Figure 4.14. *Schematic of a cell of silicon carbide Accu-MOSFET*

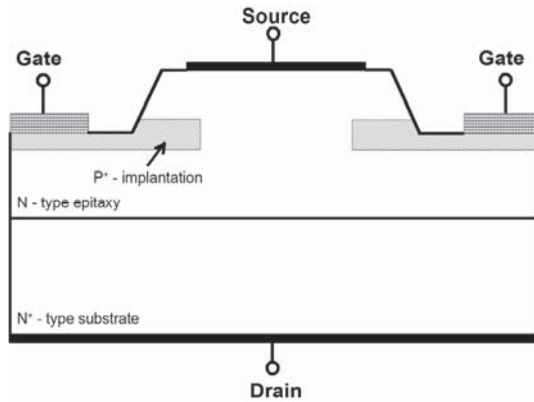


Figure 4.15. *Schematic of a cell of silicon carbide JFET*

Structure polytype protection reference	**Doping / thickness of voltage strength layer** **(cm^{-3}/µm)**	**Section** **(cm^2)**	**Direct voltage strength** **(V)**	**Direct voltage strength / current density** **(V/A.cm^{-2})**	**Specific differential series resistance** **(mΩ.cm^2)**	**Effective mobility of channel** **(cm^2.V^{-1}.s^{-1})**
ACCUFET without 6H [SHE 98]	1×10^{16}/ 10	-	350	- / -	18 at V_{GS}=5 V	120
EC-FET 4H [HAR 98]	1.7×10^{15}/ 10	1.2×10^{-2}	450	10/0.1 at V_{GS}=10 V	11 at V_{GS}=10 V	108
UMOSFET 4H [TAN 98]	2.5×10^{15}/ 10	1.728×10^{-4}	1400	10/86.8 at V_{GS}=10 V	15.7	9-30
JFET 4H [FRI 00]	4.5×10^{15}/ 15	0.041	1800 at V_{GS}=-20 V	1/100 at V_{GS}=0 V	14 at V_{GS}=0 V	-
SEJFET 4H Mesa+JTE [ASA 01]	7×10^{14}/ 50	0.0037	4450 at V_{GS}=0 V	0,75/5,5 at V_{GS}=2.6 V	121 at V_{GS}=2.6 V	-

Table 4.11. *Major technological and electrical characteristics of various unipolar transistor demonstrators in high-voltage SiC 6H, and 4H N-type, at 25°C*

4.4.1.3.3. Comparison with silicon

The classic DMOSFETs family on silicon is marketed for a range of required voltage up to 1,200 V. For these structures, on-state resistance is essentially that of the voltage holding layer. It increases with the voltage rating according to $V^{2.3 \text{ to } 2.6}$, but also increases sharply with the temperature of silicon (by reducing the mobility of electrons). For example, the specific resistance of this layer alone is about 100 $m\Omega.cm^2$ for a 600 V component and 700 $m\Omega.cm^2$ for a 1,200 V component, at 25°C. Such values are an improvement on the values previously presented for the best MOSFET structures (46 $m\Omega.cm^2$) and JFET (14 $m\Omega.cm^2$) made with 4H-SiC and support higher voltages (1,800 V).

However, the performance of SiC structures is currently equivalent to those of the new MOSFET silicon technology, based on the principle of compensation, marketed from 1998 under the name CoolMOS™ [LOR 98]: and R_{on} of 3 $m\Omega.cm^2$ at room temperature for a 600 V component, a rating which corresponds to the limit in voltage currently available for this family.

So far, unipolar switches made in SiC already demonstrate the possibility of increasing the voltage range of switches beyond 600 V without penalizing the system by increasing conduction losses, knowing that the theoretical limit of silicon carbide has not yet been reached (located, for example, at 4 $m\Omega.cm^2$ for a 3 kV component in 4H-SiC, with the R_{onS} characteristic), and knowing the technological difficulties to be overcome.

4.4.1.4. *SIT and MESFET power transistors in SiC for applications at very high frequency and microwaves*

Although applications in microwaves and power microwaves are a very specific area of power electronics, it is still interesting to devote a few lines to UHF and power microwave components as they constitute an important potential market for silicon carbide (as previously mentioned, see section 4.2.3.3). The first announcement of a commercial MESFET in SiC (in 1999 by CREE [CRE 01b]) is even earlier than the first Schottky diodes, the requirements of such structures on the characteristics of the material being less severe.

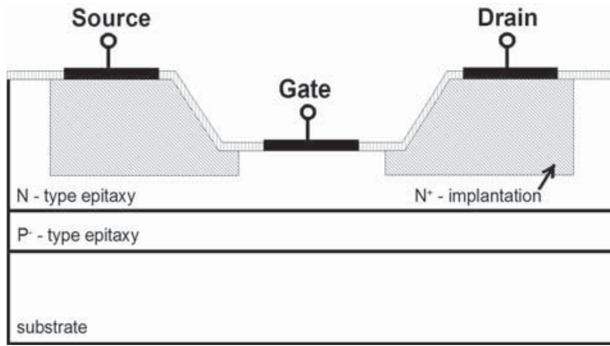


Figure 4.16. *Schematic of a silicon carbide MESFET cell*

The MESFET switch is a unipolar component with lateral conduction, where the sensitive area represents only a small surface (for example about 0.1 mm^2 for a "big" component of width 36 mm) and requires only a small epitaxy thickness with relatively high doping. The epitaxy is supported by a P-type layer that is filed on the departure substrate, preferably semi-insulator to increase the maximum frequency (the purity of the substrate must be very high). The basic layout is presented in Figure 4.16. The N-type epitaxy (with a doping of about 10^{17} cm^{-3}) is localy implemented, with N$^+$ type to create source and drain areas. An etching of the N layer sets the conduction channel between the two chambers. A metal grid lodged at the bottom of this etching, performing a Schottky contact with the N semiconductor, controls the conduction through the channel, by field-effect and by applying a negative voltage compared with the drain.

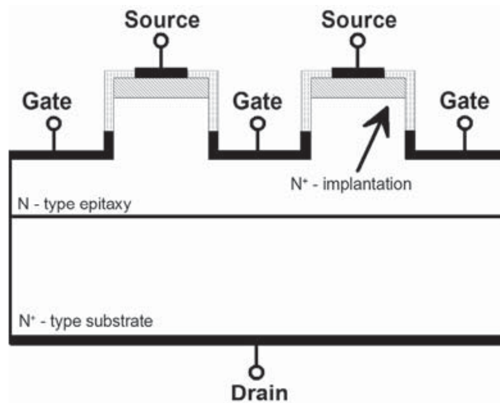


Figure 4.17. *Schematic of a silicon carbide SIT cell*

The SIT (Static Induction Transistor) switch seen in Figure 4.17 is better suited for applications under high voltage due to its vertical conduction structure [WEI 98]. The SIT switch consists of trenches, etched in an N-type epitaxial layer, coated on their sides and bottom with a metal in Schottky contact with the semiconductor. These trenches define the conduction channel of the component. The negative voltage applied between the grid and the source must allow for the pinching of this channel, which requires low doping and minimal width (respectively around 10^{16} cm^{-3} and 2 µm). Before etching, a new epitaxy or an implantation were conducted on the N epitaxy to create a strongly doped N^+ layer in order to get a good source ohmic contact on the surface.

Table 4.12 gives recent research results, including those for the commercial product of CREE [CRE 01b]. High voltage strengths are confirmed (up to 60 V, against 30 V for MESFET transistors in current silicon or GaAs) with powers of a few W/mm for total powers between 1 and 10 W at a few GHz. The latter, however, remains below the theoretical predictions.

In addition to the increase in output power supported by silicon carbide (up to a factor 4), higher levels of supply voltage (100 V are concerned) will considerably simplify the adaptation of impedance, both for passive elements to be added inside or outside of the boxes, as for very difficult settings (the removal of any system adaptation for applications of up to 3 GHz is even possible). As the MESFET SiC transistors are more linear, this simplification ensures the feasibility of broadband amplifiers that will allow the transmission of several telecommunication standards with the same equipment, thus resulting in substantial savings in terms of infrastructure (in volume, weight and cost).

Structure substrate reference	**Maximal frequency** (GHz)	**Small signal gain / drain current / drain voltage / frequency** (dB/mA/V/GHz)	**Total transconductance** (per grid width unit)**/ drain current / drain voltage** (mS/mA/V) (mS.mm^{-1}/mA/V)	**Total output RF power** (per grid width unit)**/ drain current/ drain voltage / frequency** (W/mA/V/GHz) (W.mm^{-1}/mA.mm^{-1}/V/GHz)
MESFET 1/2-insulating [CRE 01b]	4	12/500/48/2	160/500/48 *- / - / -*	12/500/48/2
MESFET 1/2-insulating [CAR 99]	20	12.5/-/60/3.5	- /- / - *40 (maximum)*	3.36/ - /60/3.5 *4/-/60/3.5*
MESFET 1/2-insulating [NOB 00]	-	8.4/140/80/2	- /- / - *- / - / -*	- /- / - / - *2,5/-/-/2*
MESFET conductor [MOO 97]	16	-	- /- / - *- / - / -*	1.1/37/50/0,85 *3.3/112/50/0.85*
SIT [SIE 97]	7-8	-	- /- / - *14 / - / -*	38/-/90/6 *1,2/ - /90/6*
SIT-module [SIE 99]	-	-	- /- / - *- / - / -*	190/500/90/2.9 (*) *- / - / - / -*

Table 4.12. *Major technological and electrical characteristics of various MESFET and SIT transistor prototypes in 4H-SiC N-type, at 25°C, in continuous wave mode (or pulsed (*))*

In summary, applications within the frequency range of 30 MHz to 10 GHz are mainly targeted: such as power amplifier systems for wireless applications (base station emitters for new generations of telecommunications systems), the digital television and radio systems, radar equipments, microwave ovens, missile detection, meteorology, etc. While the theoretical output powers of these new SiC components are not quite confirmed, research carried out over the next two years should help to discern whether silicon carbide or materials based on gallium nitride (which are better suited for frequencies beyond 10 GHz, but whose technology is less advanced) will penetrate the pre-cited markets.

4.4.2. *SiC components for switching systems under high voltage and high power*

The physical properties of silicon carbide mentioned earlier in this chapter should help to achieve very high voltage strengths from epitaxial films with very reasonable thickness and doping level. We have already mentioned demonstrators of unipolar components with high breakdown voltages close to 4 kV (see section 4.4.1). Bipolar components are theoretically better suited for very high voltage and high power applications. The demonstration of the possibility of reaching very high breakdown voltages, even higher than the limits of silicon devices, was shown by many demonstrators.

The state of the art of performances of SiC diodes and high-voltage thyristors are presented in the following sub-section. Mixed unipolar/bipolar structures of demonstrators (for example, bipolar junction diodes, Schottky diodes, and IGBT) also made in SiC, will be presented, in an attempt to extend the power of the unipolar “family” or frequency range of other the bipolar “family”. Positioning of the respective areas of preferential use of the different technologies, including silicon, is proposed. This is provisional, given the immaturity of the SiC devices presented here (still at the research stage) and the progress of each chain. Currently known potential applications will also be mentioned.

4.4.2.1. *Bipolar diodes and bipolar and Schottky mixed junction diodes*

The SiC bipolar diode is made on a heavily doped N^+-type substrate, more generally of 4H polytype for the last tests. The low doped N-type voltage holding layer, is epitaxied on this substrate (often after filing of an intermediate N^+ layer with a thickness of about 1 µm). The emitter is strongly P^+-type doped and then applied either by implantation or by resumption of epitaxy. In the latter case, the termination of the junction requires an engraving (to provide protection by simple mesa, or with JTE), while plane structures can be used to protect the periphery of P^+ emitters against enhancements of the electric field under strong reverse polarization. Most often there is a lateral extension of the junction termination (JTE, itself implanted), as shown in Figure 4.18.

The goal of achieving diodes with Schottky mixed bipolar junctions (so-called “JBS”' or “MPS”) simultaneously benefits the lower voltage drop at the on-state of the metal/semiconductor junction, and the lower leakage currents at reverse state of the P^+N junction, for a given voltage rating. The ion implantation of the P^+ emitter regions produces plane JBS structures on N-type epitaxied substrate, as shown in Figure 4.19. Non-plane JBS structures can also be made from a pile of epitaxies P^+ on N (on N^+ substrate), etching the P^+ layer onto the desired locations for Schottky contacts, and onto the periphery.

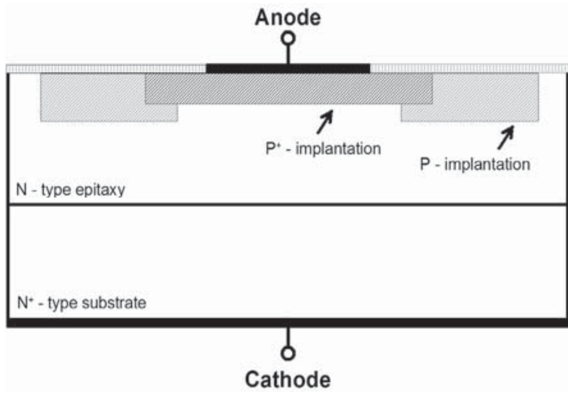


Figure 4.18. *Schematic of a SiC bipolar diode P^+NN^+ with JTE type peripheral protection*

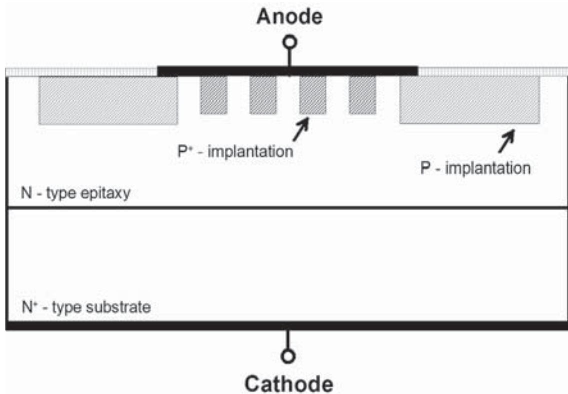


Figure 4.19. *Schematic of a SiC diode with mixed bipolar and Schottky junction with JTE type peripheral protection*

4.4.2.1.1. Performances of bipolar and "JBS" diodes

Tables 4.13 and 4.14 present direct and reverse, technological and electrical characteristics of prototypes of bipolar and JBS diodes, published in recent years.

Structure passivation protection reference	**Doping / thickness of voltage strength layer** **(cm^{-3}/µm)**	**Anode section** **(cm^2)**	**Reverse voltage strength / temp.** **(V/°C)**	**Direct voltage / current density** **(V/A.cm^{-2}/°C)**	**Specific differential series resistance / current density / temp.** **(mΩ.cm^2/ A.cm^{-2}/°C)**	**Current density / reverse voltage / temp.** **(mA. cm^{-2}/V/°C)**
P^+(imp)NN^+ JTE [MIT 98]	8x10^{15} /14 5x10^{15} /26	0.01 0.01	2000 3000	3/100/25 4/500/25 3.15/100/25 3/100/125 4.8/500/25	 2.2/500/25 3/500/25	3x10^{-6}/ 1000/20 3x10^{-5}/ 1000/150 3x10^{-6}/ 1000/20 3x10^{-5}/ 1000/150
P^+(imp)NN^+ JTE [CEG 01]	1.2x10^{15} /40	0.01	2300	5/60/25	30/60/25	<10^{-4}/1100/25
P^+(imp)NN^+ SiO_2 JTE multiple [LEN 00]	10^{15} /35	0.2	3000	3.4/100/25	5/150/25 3.8/150/125	<10^{-2}/3000/25
P^+(imp)NN^+ SiO_2 JTE multiple [LEN 01]	10^{15} /35-45/	0.2	4500	3.4/100/25 3.3/100/125 4.3/300/25	7/200/25	<10^{-3}/4500/25
P^+(epi)NN^+ 2 µm SiO_2 JTE bore + stop. Channel [SIN 01]	9x10^{14} /50	0.04	5300/25	3.7/100/25 3.3/100/225 6.9/1250/25	3.5/200/25 4/200/250 3/600/250	1/5000/25 3x10^{-4}/ 2000/50 3x10^{-2}/ 2000/225
P^+(epi)NN^+ JTE [SUG 00]	10^{15} /50	3.14x10^{-4}	6200/25	4.7/100/25	7.4/150/25	15x10^{-3}/6200 /25
P^+(epi)NN^+ JTE bore [SUG 01]	2x10^{14} /120 8x10^{13} /200	3.14x10^{-4} to 7.85x10^{-1}	14900/25 19500/25	4.4/100/25 4.1/100/250 5.1/300/250 6.5/100/25 7.5/100/250	6/150/25 5.3/150/250	1/14000/25 10/14000/250 3/19000/25 25/14000/250

Table 4.13. *Major technological and electrical characteristics of various demonstrators of bipolar high-voltage SiC-4H diodes from recent literature*

Structure polytype passivation protection reference	**Doping / thickness of voltage strength layer** **(cm^{-3}/µm)**	**Anode section** **(cm^2)**	**Reverse voltage strength / temp.** **(V/°C)**	**Direct voltage / current density / temp.** **(V/A.cm^{-2}/C)**	**Specific differential series resistance / temp.** **(mΩ.cm^2/°C)**	**Current density / reverse voltage / temp.** **(mA.cm^{-2}/V/°C)**
$(Ni/P^+)_{50\%}NN^+$ SiO_2 JTE etched [TON 00]	$9.7x10^{15}$ /13	0.031	1000	1.3/100/25 2.3/100/255 3/460/25	6.4/25 15/255	0.03/800/25 0.3/800/255
$(Ni/P^+)_{44\%}NN^+$ SiO_2+1 µm Si-poly Floatting rings [SHE 01]	$1\text{-}2.5x10^{15}$ /30	$3.14x10^{-4}$ to $1.26x10^{-3}$	2500	2.9/100/25		0.4/2000/25
$(Ti/P^+)NN^+$ SiO_2 JTE multiple [LEN 01]	10^{15} /35	$1x10^{-3}$	2500	2/100/25 2.6/100/125 3.6/300/25 4.7/300/125	8/25 14/125	0.02/1000/25
$(Ti/P^+)_{75\%}NN^+$ SiO_2 JTE [DAH 01]	$3x10^{15}$ /27	$4x10^{-4}$	2800	1.75/100/30 3/100/225 4.2/500/30	6/30 20/225	$3x10^{-3}$/500/30
$(Ni/P^+)_{50\%}NN^+$ JTE [ASA 00]	$1.3\text{-}1.8x10^{15}$ /30 $1.3\text{-}1.8x10^{15}$ /50	$9x10^{-4}$	2000 3600	3/100/25 6/100/25	 43/25	10/2000/25 10/3600/25

Table 4.14. *Major technological and electrical characteristics of various demonstrators of JBS high-voltage SiC N-type 4H diodes from recent literature*

The increase in deposit speeds of films has allowed for an increase in the achievements of high voltage demonstrators in recent years. In 2001 a 19 kV voltage (approximately double the maximum value offered by silicon) was recorded, voltage for a bipolar diode in 4H-SiC with an epitaxied base, N-type, thickness 200 µm [SUG 01]. The mixed junction structures were tested for up to 4 kV voltages.

The majority of prototypes are still small. The reduction of the density of defects in the substrates, however, recently allowed the characterization of a few prototypes of relatively large section bipolar diodes (40 mm^2 positioned in pre-selected regions), with tests run under direct currents of several tens of Amps [LEN 01]. The

efficiency of manufacturing such structures remains low starting on available substrates.

The leakage currents of bipolar diodes under heavy reverse polarization are generally very low, even when measured close to the maximum voltage, and even at relatively high temperatures, also in most cases these structures are without an optimal passivation surface. The leakage currents of JBS structures seem to be generally more important, from 25°C.

These demonstrators in bipolar SiC diodes, support several thousand of volts under reverse voltage, and have differential specific resistances at on-state from as low as a few mΩ.cm^2 (for direct current densities greater than 100 A/cm^2) at room temperature, but also at high temperatures (250°C), while their characterizations in commutation also reveal that they are very fast components. Indeed, the reverse-recovery charge, and hence the associated peak reverse current, which were seen at blocking, are very low for all structures studied, as in the example of Figure 4.20 for a 5 kV diode [SIN 01]. Moreover, their speed is not affected by the rise in temperature. Such performances thus make it possible to operate very high voltage systems with switching frequency beyond the range of kHz.

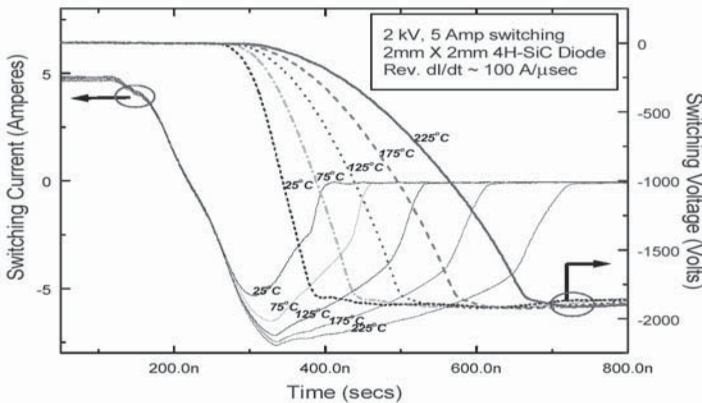


Figure 4.20. *Waveforms of current and voltage at the opening of a P^+NN^+ 5 kV diode at different temperatures. The switched current cut is 5 Amps (125 A.cm^{-2}), descending at a speed of 100 A/µs, under a 2 kV voltage (extracted from [SIN 01])*

Table 4.14 shows that JBS diodes keeping voltage to about 3 kV, also set a specific resistance of some mΩ.cm^2 at room temperature. In terms of direct voltage these fast components confirm their interest in relation to the purely bipolar SiC structures, however, stronger voltage ratings, higher operating temperatures, and increasing values of series resistance (see also leakage current) make JBS diodes

much less attractive than bipolar junction devices for high power applications. Note also the low dependency (or stability) on temperature (in the operational range) displayed by the behavior of bipolar diodes, compared with unipolar conduction diodes.

The bipolar diodes potential for very high density current can be illustrated by the results of Dyakonova *et al.* [DYA 00] who reports on the feature of a direct current of up to 55 kA.cm^{-2}, depending on a voltage below 20 V, for a diode in 4H-SiC keeping a 5.5 kV voltage (diameter 100 µm, and N base of thickness 85 µm doped between 7 and 10 x 10^{14} cm^{-3}).

Some recent publications [LEN 01], however, reported an increase in direct voltage of certain bipolar devices subject to a polarization of long duration, which would put into question the reliability of the systems using them. This instability of the direct characteristic of the bipolar high-voltage SiC diode has not been observed for Schottky or JBS devices, and is attributed to defects in the base material (stacking faults), activated during operation (under current densities of about 100 A.cm^{-2}).

4.4.2.1.2. Comparison with silicon

We have seen that the high-voltage SiC based diodes, even when they are only bipolar type, are very fast devices. First, we will compare them to silicon bipolar diodes described as “fast”, with voltage ratings between 3 and 6 kV (which is the highest rating currently offered in this category). Then we will discuss briefly, with an example, the case of recovery diodes with voltage strengths of up to 9 kV.

“Fast” silicon diodes with voltage strength between 3 kV and 6 kV

Although the active area of the semiconductor is unknown, it is possible to approximate a few orders of magnitude of performances of such products from manufacturers data sheets

– maximum junction temperatures in operation (T_{jmax}) are generally 125°C or 140°C;

– maximum leakage currents are between 10 and 100 mA/cm^2 at T_{jmax};

– specific series resistances estimated from values of differential resistance given at T_{jmax} vary broadly, within the range of 5 to 50 mΩ.cm^2;

– the maximum voltage drop in the forward state varies within a wide interval, ranging from about 3 V to 6 V at T_{jmax}, and for a current density (probably different from one component to another) around 300 A/cm^2 as a maximum.

Compared with the results presented in the preceding paragraph, we can see that the prototypes of a bipolar SiC diodes, with similar voltage strength (3 kV to 6 kV), show their superiority, including progress in terms of series resistance. The currently mastered technology has probably not as yet achieved the best results in terms of ohmic contact, efficiency of peripheral protections and surface passivation. This must also be made subject to encapsulation techniques adapted to conserve these performances.

In terms of voltage drop at on-state, the data shows that the range of values are equivalent for both SiC and "fast" Si bipolar technologies and that the extra voltage difference introduced by the SiC is not a handicap for this range of voltage strength and temperature.

For example, Figure 4.21 shows a direct comparison of the characteristics of a prototype of bipolar diode in 4H-SiC keeping a voltage of 4.5 kV [LEN 01], with those from the data sheets of a commercial product 4.5 kV (reference D911SH45T [EUP 01]), sold as a free wheeling diode for hard commutation converters based on IGBT or IGCT. To meet this function, the diode was necessarily designed to minimize its reverse-recovery charge, during its blocking. Comparison with the diode in 4H-SiC chosen itself for being fast, is very interesting.

Even if the values of current densities of the Si structure should not be regarded as accurate values (but rather over-estimated in order to evaluate the silicon carbide in a "worst case senario"), Figure 4.21 clearly shows that use of SiC is not necessarily a disadvantage from the viewpoint of the direct voltage on a fast diode: for this example at 4.5 kV and 125°C "only" (for silicon carbide, etc.) the 4H-SiC structure reduces conduction losses for current densities near or above 90 A/cm^2. This benefit will begin at a level of current density (and, therefore, power density to dissipate) even weaker than the increase in voltage rating (even as the operating temperature increases).

Thus, the power dissipated in conduction by high voltage SiC bipolar diodes will not reduce the silicon carbide drive to increase the frequency of commutations, and/or reduce cooling systems, which is allowed by the speed of these structures and their very limited switching losses. On this point, an example of comparison is also provided by Lendenmann *et al.* [LEN 00] They show that the commutation loss, measured for a module involving (in a pressed box conventional technology) the SiC diode from Figure 4.21 (actually 4 chips of 40 mm^2) and a 2.5 kV silicon IGBT (4 chips of 1 cm^2), switching 400 A under 1,250 V at a 125°C junction temperature, represents only a few per cent of a modules loss, including Si diodes of the same voltage rating. This way the switching frequency, limited to kHz by current Si devices due to the losses they suffer, partly due to the recovery of the free wheeling diode, may be increased.

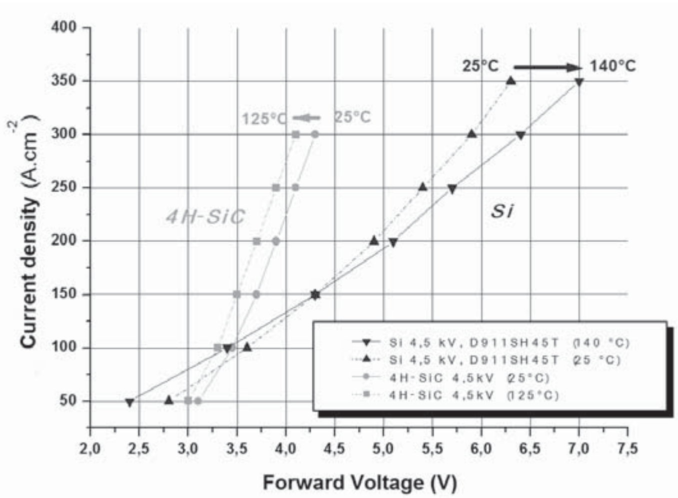


Figure 4.21. *Comparison of direct characteristics of "fast" bipolar silicon diodes D911SH45T in 4H-SiC studied by Lendenmann [LEN 01], with a voltage strength of 4.5 kV, for both provided junction temperatures. Note that, due to their size difference, the current values provided by the technical data sheet of the silicon component are converted into values of current densities. To do so, the average value of direct current I_{Fav} (911 Amps at 50 Hz and 85°C) was supposed to correspond to 100 A.cm^{-2}*

The on-state direct voltages of 4H-SiC JBS diodes, recorded in the preceding section as being smaller than those of bipolar diodes (in SiC as in "fast" Si) may have an interest in the lowest range of voltage considered here, for which their other performances remain very competitive. They would thus extend the scope of applications of SiC Schottky diodes. (This note would be even more important if the reliability problem of bipolar SiC diodes, mentioned above, remains unresolved). For these intermediate levels of voltage (between 2.5 kV and 3.5 kV approximately), four families of diodes should be placed in competition to meet the specification of a specific application, namely: SiC Schottky, SiC JBS, Si bipolar, or SiC bipolar (frequency-related matters, overload current, and volume are always the first criteria to be considered).

Recovery diodes for voltages up to 10 kV

When the function to be ensured is a recovery function, or a function for which the commutation speed is no longer a critical characteristic, the example seen here and shown in Figure 4.22 shows that silicon remains the best choice for applications up to 10 kV (the commercial current limit of Si).

Figure 4.22 shows the direct feature $J_d(V_d)$ of diode prototype 4.5 kV in 4H-SiC at 125°C used for the previous figure, and compares it with the same feature at 160°C for D471N80...90T diode, which has a voltage strength of 9 kV [EUP 01]. The characteristics of the SiC diode (at least up to 125°C) remain mostly to the right of the graph for the current densities considered, despite its voltage rating being lower than that of the Si diode.

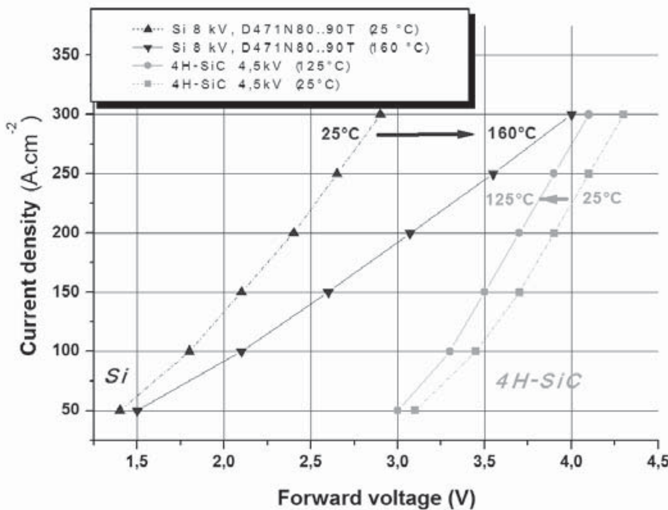


Figure 4.22. *Comparison of characteristics of the recovery silicon bipolar diode D471N80...90T keeping 9 kV, and the bipolar diode in 4H-SiC studied by Lendenmann [LEN 01] keeping 4.5 kV, for junction temperatures of 160°C and 125°C respectively. Note that, given the difference in size of these devices, the values of currents provided by the technical specification of the silicon component are converted into values of current densities, conceding that the average value of direct current I_{Fav} (565 A at 50 Hz and 85°C) corresponds to 100 A.cm^{-2}*

In this case, exploitation of the SiC junction's ability to operate at junction temperatures beyond 220°C[1], and thus dissipation of powers far beyond those possible for the silicon (theoretically limited to 400 W.cm^{-2}), may make silicon carbide rectifiers more advantageous at the limits of the voltage still covered by silicon.

1. Note: the value of this temperature is difficult to evaluate as it depends on the voltage rating. On the other hand, it will evolve according to the progress of SiC technology (control of doping profiles, carrier's lifetime, improvement of ohmic contacts and peripheral protection), which will lead to lower on-state voltage drops.

This assumes, of course, resolution of the issues raised by the feasibility of setting housing adapted to the operation under very high voltage and high internal temperature. The gain will result in the form of maximum current densities, and thus smaller or more powerful systems.

4.4.2.2. *Thyristors and IGBT*

The research onto this category of components is far less numerous than research into diodes (which are easier to build), and unipolar switches (whose theoretical benefits are more obvious and widespread). Thyristors and IGBTs (isolated gate bipolar transistors) in silicon concern more specifically the scope of applications of very high power (up to 80 MVA for thyristors and GTOs (thyristors opened by the gate) and 10 MVA for IGBTs). This specificity should be even more marked with SiC.

These components require, on the other hand, the implementation of at least four semiconductor layers (instead of the norm of three minimum), and include (exclusively or in part) a bipolar conduction, which requires a superior quality for the semiconductor and its doping. Finally, the IGBT structure inherits most of the problems of the SiC MOSFET structure (linked to the current quality of the SiO_2/SiC interface and to the strong electric field in the oxide). The first thyristor (symmetric GTO [PAL 96]) and IGBT (N-channel [RAM 96]) demonstrators date back to 1996.

The majority of structures obtained so far are in 4H-SiC and made by locally engraved and epitaxied layers, as presented by Figures 4.23 and 4.24.

In the case of the GTO thyristor (Figure 4.23), the thick layer intended to keep the blocking voltage under direct polarization is P-type. It is in most cases epitaxied on a P-type layer used to stop the electric field under direct blocking voltage in order to make the component robust against digging. (Note, the presence of this layer makes the structure asymmetric because it does not allow the switch to withstand a strong reverse polarization voltage). The P layer itself is deposited on the N^+-type substrate (or an intermediate N^+-type epitaxy to better control the quality of the material, including the PN^+ junction).

The N base epitaxy is about a few µm thick and is doped to about 10^{17} cm^{-3}. The P^+ anode emitter is from a final P^+-type layer engraved and then localy filed over its entire depth delineating the anode areas (usually fingers from 20 to 30 µm wide). The underlying N layer is thus laid bare, and can be localy N^+-type doped and metallized to make the trigger ohmic contact between each anode finger. This makes inter-digitations of the anode and the trigger (widely studied for silicon devices), which improves the performance of the switch, especially during the transitional

phases of ignition and blocking. Different techniques for protecting against the premature breakdown of the NP^- junction at the periphery of the component under heavy direct bias were used: by mesa with plasma etching of the material throughout all the P^- base, by niche etched into the N base (of slightly greater height than the thickness of the layer), which will play the role of custody floating rings, or by N-type pocket located in the P layer after plasma etching of the N layer, creating an extension of the lateral NP junction to be protect (as presented on Figure 4.23).

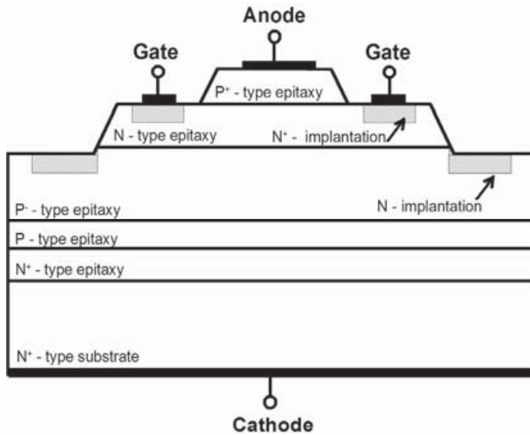


Figure 4.23. *Schematic of an asymmetric, silicon carbide GTO thyristor $P^+NP^-PN^+$ with JTE-type peripheral protection*

The first demonstrators of IGBTs have been made on P^+ type substrates, (SiC-6H then SiC-4H), like their silicon counterparts. A PN^-P^+ bipolar transistor is then combined with a N-channel MOS transistor, as shown in Figure 4.24. The layer of voltage holding in N^- is then deposited on the substrate N^+ (or an intermediate buffer layer N^+ previously epitaxied). The P layer of the canal and N^+ layer of the drain are also made by epitaxy, and trenches are etched in order to create a UMOSFET structure (see section 4.4.1.3.1).

However certain specificities (natural or cyclical) of silicon carbide architecture present the following disadvantages: the P^+ type substrate is difficult to make, and resistive; its injection effectiveness is low at classical temperatures due to the incomplete ionization of acceptors; the PN^-P^+ transistor has a safe operating area smaller than the NP^-N^+ transistor because the ionization coefficient of the holes impact is larger than that of the electrons. These considerations argue in favor of a P channel IGBT structure (despite the lower mobility of holes carriers). A comparative study by simulation of 5 kV structures based on 4H-SiC [WAN 00] concludes that in terms of on-state low voltage drop, P channel IGBT is better suited

for uses between 300 K and 400 K than the N channel component. In terms of switching, the P-channel structure remains faster than the N channel, whatever the temperature of the semiconductor. Polytype 6H is even used by some people to improve the series resistance, (because of better behavior of the SiO2/SiC interface obtained today).

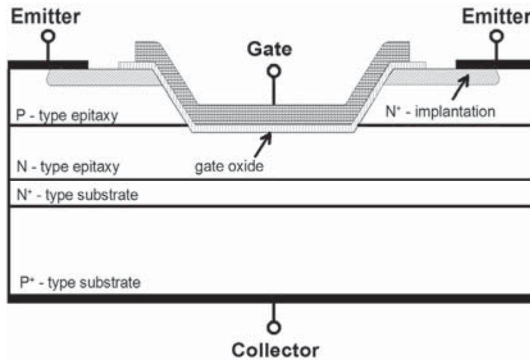


Figure 4.24. *Schematic of an IGBT transistor with N-channel U-MOSFET*

4.4.2.2.1. Performances of GTO and IGBT demonstrators

Table 4.15 provides the main features of several GTO demonstrators tested experimentally, and already shows interesting performance results.

The maximum voltage strength at the moment is 3 kV. Operations under high current densities and high junction temperatures were observed. The maximum demonstrated current rating was 12 A, corresponding to a current density of 700 $A.cm^{-2}$, leading to a direct voltage of 6.5 V at 300°C, obtained for an asymmetric GTO thyristor with voltage strength of 2.6 kV [AGA 00]. The on-state performances at near ambient temperature are less desirable than those at higher temperatures, due to the ionization of acceptors and lengthening of the carrier lifetime with a rising temperature. The SiC GTO are easily trigged and opened, by low amplitude trigger currents.

Structure passivation periphery reference	**Doping / thickness of voltage strength layer** **(cm^{-3}/µm)**	**Anode section** **(cm^{-2})**	**Direct voltage strength / temp.** **(V/°C)**	**Direct current density / temp.** **($A.cm^{-2}$/V/°C)**	**Specific differential resistance / current density / temp.** **($m\Omega.cm^2$/ $A.cm^{-2}$/°C)**	**Trigger current for switch-on / blocked voltage / temp.** **(mA/V/°C)**	**Reverse current density / reverse voltage / temp.** **(mA/V/°C)**
$P^+NP^-N^+$ [PAL 96]	-	$3.2x10^{-3}$ $3.2x10^{-3}$	900/25 700/25	625/3.93/25 1000/3.67/25	 0.82/300/25	-/-	$22x10^{-6}$/800/27
$P^+NP^-P^+N^+$ triple JTE [FED 00]	-/12	$4.6x10^{-4}$	1100/200	100/12-15/25 100/4.5-5/200	#1/500/200 -	- -	10^{-3}/1000/25 10^{-2}/1000/200
$P^+NP^-P^+N^+$ SiO_2 engraved floating rings [FUR 00]	$2.1x10^{15}$/13 -	$4x10^{-5}$ -	800/25 1200/25	4000/-/25 -	- -	0.4/600/25 -	10^{-3}/1000/25 0.2/1100/25
$P^+NP^-PN^+N^+$ 4H JTE [AGA 00]	$7-9x10^{14}$/50	0.0167	2600/25	100/4.25/62 100/3.4/300 700/6.5/300	4/500/100	-	-
$P^+NP^-PN^+N^+$ 4H JTE [RYU 01]	$7-9x10^{14}$/50	3.7 $x10^{-3}$	3100/25	100/4.25/62 100/3.4/300 300/5/25	4/500/100	65/2000/25	-

Table 4.15. *Major technological and electrical characteristics of GTO demonstrators in SiC-4H*

In addition, the switch-off of current densities up to 4,000 $A.cm^{-2}$ has been reported [FUR 00]. The rise times of the current observed at switch-on decrease with temperature, while switch-off times increase [FUR 00]. For all the structures tested, commutation times are less than a few hundred nanoseconds, including at high temperature (300°C), thus demonstrating the rapidity of these switches.

Table 4.16 provides the main characteristics of experimental IGBTs discovered so far.

Structure polytype periphery reference	**Doping / thickness of voltage strength layer** **(cm^{-3}/µm)**	**Emitter section** **(cm^2)**	**Direct voltage strength / temp.** **(V/°C)**	**Direct current density / direct voltage / temp.** **($A.cm^{-2}$/V/°C)**	**Specific differential resistance / current density / temp.** **(mΩ.cm^2/ $A.cm^{-2}$/°C)**	**Grid threshold voltage / direct current density / temp.** **(V/mA.cm^{-2} /°C)**
P^+NP^- PN^+ UMOS P channel 4H MESA [SIN 99]	5x10^{15}/10	0.02	85/-	1.25/-14/25 70/-14/300 (for V_{GE}=-36 V)	32000/-/25 226/-/350	-29/-/25 -22/-/350
P^+NP^- PN^+ UMOS P channel 6H JTE [RYU 00]	5x10^{15}/15	0.02	400/25	15/-10/25 100/-10/400 (for V_{GE}=-30 V)	431/6/25 80/35/400 (for V_{GE}=-30 V and V_{CE}=-5 V)	-10/1/25 -4/1/400 (for V_{CE}=-5V)

Table 4.16. *Major technological and electrical characteristics of IGBT demonstrators in a SiC-6H and 4H*

The voltage ratings of the first IGBTs demonstrators in SiC are low, due to the use of relatively thin films. The direct performances remain modest, especially at room temperature: the highest current densities (100 $A.cm^{-2}$) are measured for the highest test temperature (which corresponds to a current of 2 Amps obtained at 400°C [RYU 00]). The SiC MOSFETs structures cannot currently allow low voltage commands for P channel IGBTs.

4.4.2.2.2. Other structures

In the same spirit that led to IGBT (MCT, MOS controlled thyristor and other) structures being developed on silicon, studies are appearing (essentially by simulation) to assess the performance of silicon carbide components. These studies involve a bipolar structure together with a "drive" structure, so as to exploit the best characteristics of both parties while avoiding their disadvantages. A GMT (gated

MOS transistor) with an architecture of 5 kV is proposed and compared to the N channel and P channel IGBT structures [TAN 00] in order to overcome the compromise between on-state resistance and safe operating area, and eliminate the problem of the parasitic thyristor, imposed by the SiC IGBT structures.

Note that published research on the SiC $N^+PN^-N^+$ bipolar power transistor were, in the past, even rarer than those on IGBTs, more or less guided by the experience of silicon (where this “kind” of large power system gradually disappeared). The demonstrated speed of SiC bipolar structures (as seen previously with diodes and GTOs), and progress in mastering the technology (on which the current gain depends) encourages researchers reconsideration [HUA 00]. Several papers on the power bipolar transistor were proposed at the international conference on silicon carbide ICSCRM’2001, while none were presented for the IGBT transistor.

Many other structures are certainly possible or able to be combined, and there substantial work remains in the area of design for these types of high-power components, taking into account the differences between Si and SiC (which can play a vital role in the strengths of the devices), and also development of optimized tools for both manufacturing and simulation.

4.4.2.2.3. Comparison with silicon

The current performances of the first GTO thyristors and IGBT transistor demonstrators in SiC (with low currents as in the case of diodes, but also low breakdown voltages) does not allow for a direct comparison with existing commercial devices.

Figure 4.25, representing the voltage and current ratings of silicon components for high power applications, and their developments over recent years, is proposed here to predict how long evolution of a pipeline can take, with impressive progression between the original structures and the latest designs. Since this figure was presented in 1999 [DED 99], the situation has further evolved with, for example, the emergence of IGBTs 6.5 kV/600 A onto the market.

It seems even more obvious to say that several years of efforts are still needed to develop a powerful switch benefiting from the advantages of the SiC semiconductor. All elements in the chain must be reinforced, to create higher quality electronic materials, high-voltage and high temperature housing, passing through the various stages of design and manufacturing optimization.

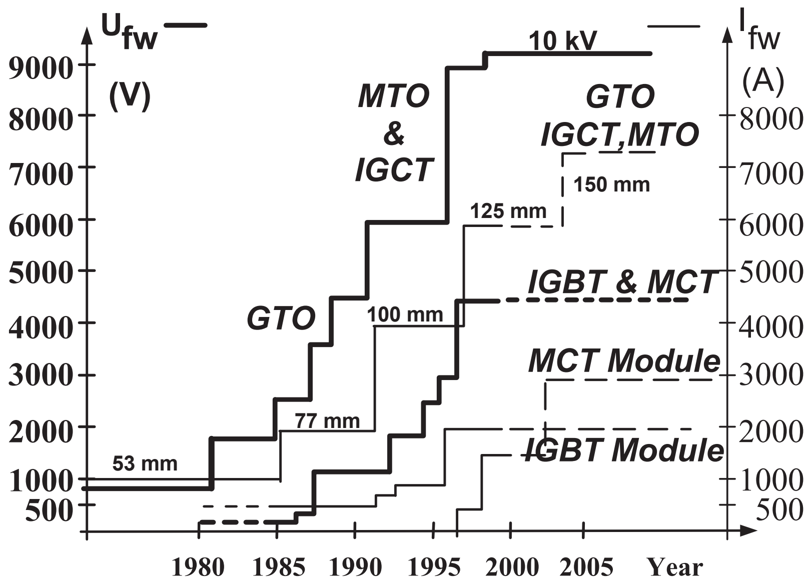


Figure 4.25. *Areas of voltages and currents covered by different families of powerful silicon components and evolution over time [DED 99]. Relevant acronyms: IGBT, insulated gate bipolar transistor; MCT, MOS controlled thyristor; GTO, gate turn-off thyristor; MTO, MOS-turn-off thyristor; IGCT, integrated gate commutated thyristor*

4.4.2.3. *Potential applications*

Given the theoretical potential of very high voltage and high power silicon carbide components, and performances offered by the first demonstrators (including bipolar diodes and GTO thyristors), the first potential applications are certainly in the areas of production, conversion, and transmission of energy, especially since the current trend toward decentralized sources of production generates increased or new demands (multiplication of electrical power distribution stations, network management, quality, etc.). The emergence of solid state electronic devices in systems up until now outside of their bearings, represents a step towards greater flexibility, controllability, even “intelligence” of these ensembles. Power electronics is already present on most of the systems (alternators, engine control, etc.). The downsizing of power electronics (by avoiding serial connections of components, reducing coolers and filters) will allow its direct integration on the machine.

The reduction of losses, and the increase in eligible temperatures (under the condition of integration issue resolution) are also relevant for the field of transport,

from electric traction (train, bus, subway, streetcar) and electric propulsion (cruise ship), to the hybrid vehicle.

High-voltage applications based on the generation of very strong current pulses (electromagnetic launchers [ARS 01]), or with lower current (high density lamp ballast) are also affected by the prospective volume reductions and good energy management offered by silicon carbide.

Maintaining high energies also relates naturally to specifications regarding the protection of electrical circuits. This feature applies to all types of applications: those with very high voltage, as in the field of energy mentioned above with special needs in parallel protection devices, and those at low voltage for domestic installations, for example those requiring series protection devices.

The prospective use of silicon carbide for the series protection of facilities on a low voltage network is discussed in the following section.

4.4.3. *High energy SiC components for series protection systems*

The series protection equipment of electrical circuits, including that supplied by the home network, is currently electro-mechanical systems. No current semiconductor component is able to both; have a sufficiently low resistance under normal operation, and be able to dissipate the energy during a short-circuit on the load. The silicon in particular can not withstand a sufficiently long period of self-heating, produced by the simultaneous presence of short-circuit (even of a few amps) and the voltage at its terminals. Such applications would seem to be within the scope of the properties of silicon carbide, particularly through its high temperature features and its good thermal conductivity.

Figure 4.26 shows a proposed current limiting structure, adapted to the series protection on the low voltage network (voltage strength: 600 V, rated current: 5 A) [NAL 01]. Operating on the same principle the JFET structure (see section 4.4.1.3.2), this structure is normally under a low V_{DS} voltage. Increased V_{DS} voltage causes pinching of the conduction path by the JFET effect, producing current saturation, the following current decline is the result of the semiconductor self-heating, due to the simultaneous presence of high current and high voltage. A thermal runaway may follow if the overheating is created locally.

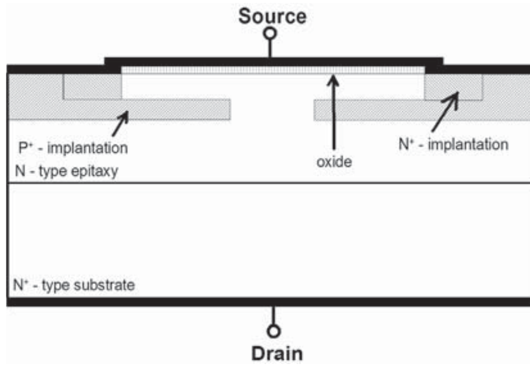


Figure 4.26. *Schematic of a unipolar SiC component proposed for use as a current limiteron low voltage networks [NAL 01]*

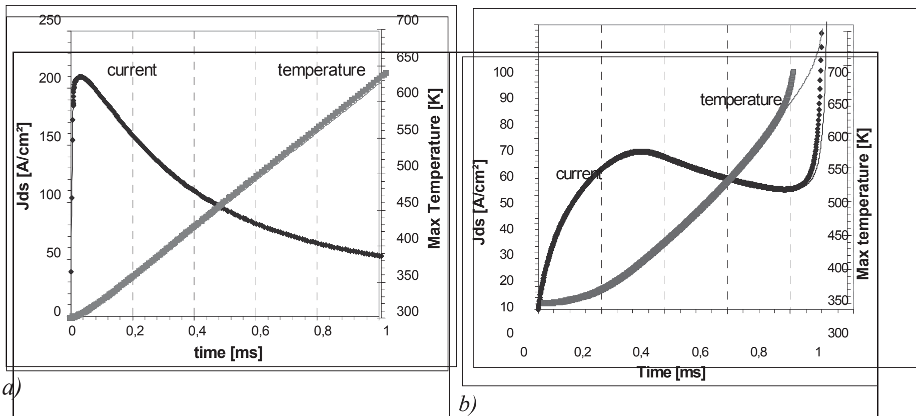


Figure 4.27. *a) Current density and maximum temperature in the 4H-SiC component, as a function of time, the application of a linear increasing voltage (from 0 V (at t=0 ms) to 500 V (at t=1 ms)). between Drain and Source terminals resulting from (The main parameters of the structure are: $N_{epi}=10^{16}$ cm^{-3}, $W_{epi}=6$ µm, $X_{Jcanal}=0.2$ µm, $L_{canal}=4$ µm, $N_{canal}=2x10^{17}$ cm^{-3}, $T_{amb}=300$ K, $R_{Thcomp/ambinferior)}=0.5$ K.cm^2.W^{-1}, $R_{Thcomp/amb(superior)}=0.5$ K.cm^2.W^{-1}) b) Idem for a 600 V silicon MOSFET (implanted channel and epitaxy thickness of 40 µm doped at 10^{14} cm^{-3}), with the aforementioned constraints, leading to the emergence of a thermal runaway after 0.9 ms (extracted from [NAL 00])*

Figure 4.27 shows the assessment of the maximum temperatures inside devices at 600 V in 4H-SiC and Si, obtained by simulation (using the DESSIS program from ISE TCAD [ISE 98]) of their electro-thermal behavior as a result of a linear rise in the voltage applied to the terminals up, to 500 V after a millisecond (only cooling by the underside is considered, with a thermal resistance of 0.5 K.cm^2.W^{-1} between the

component and the atmosphere) [NAL 00]. An acceptable compromise between low series resistance under normal operation and no thermal runaway in current limiting operation cannot be achieved with the simulated silicon structure (on the principle of a 600 V MOSFET with implemented channel), however, can be observed for the 4H silicon carbide structure. The latter shows a stable electrical behavior despite internal locally temperatures rising up to 350°C, and a power increase up to 25 kW.cm^{-2} after 1 ms (for this example).

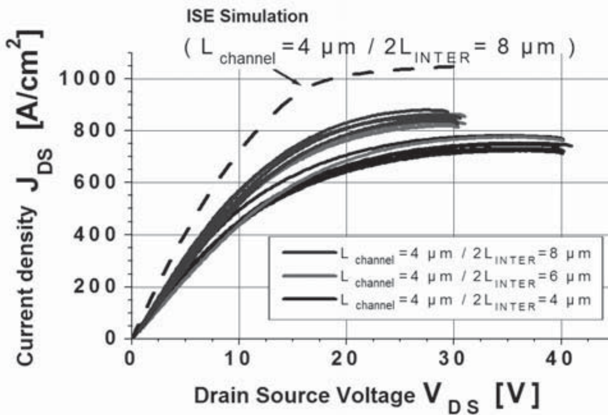


Figure 4.28. *Experimental characteristics $J_{DS}(V_{DS})$ of current limiting demonstrators for 600 V / 5 A applications in SiC-4H (measures on wafer, by testing under peaks at room temperature, without control of self-heating). The simulated characteristic considers a mobility of electrons in the channel of 400 cm^2.V^{-1}.s and no charge at the SiO_2/SiC interface (from [GOD 01])*

Figure 4.28 shows a series of experimental characteristics $J_{DS}(V_{DS})$ obtained from the first demonstrators made in 4H-SiC (peripheral protection is provided by custody P^+ rings made at the same time as the P^+ areas) [GOD 01]. Strong current densities are reached (900 A.cm^{-2}) in the saturation regime, and the experimental specific resistance to linear operation (characterizing the operation without default) at room temperature is low, 13 mΩ.cm^2 on these structures with non-optimal ohmic contacts. These initial achievements validate the concept of current limitation power, being fairly close to the simulation results; also the feasibility of such structures in 4H-SiC with a simple technology encourages further performances.

Current limitation in the alternative network is achievable by setting a "tumble" series of two components (see Figure 4.26). The series resistance, and especially the lack of cut-off power of this solution will not be able to completely eliminate

electro-mechanical breakers from electrical installations, however, a part can be removed, design size can be reduced, and lifetime can be prolonged by reducing peak values of the currents to be interrupted. Structures in SiC including control electrodes are also envisaged [TOU 01]. Compared with the classic solution of the fuse for example, they have the added advantage of not requiring human intervention following a default (thus reducing maintenance on some systems). The introduction of controllable electronic devices in the home automation sector could also provide the possibility of expanding the functions of devices beyond mere protection, by combining these new types of components with interactive control systems.

Optimization of technology (including box setting), and an overall analysis of facilities, are both still necessary before seeing the emergence of these new components on the market, which is a desired advancement while there is no competition of semiconductor based devices.

4.5. Conclusion

The silicon carbide (SiC) is a material with proven and potential applications, almost as numerous as its various forms. Used from a long time as a composite or abrasive material because of its mechanical and chemical properties in polycrystalline state, also acknowledged more recently in jewellery for its crystalline beauty, SiC has also been marketed for the first time as semiconductor for blue light-emitting diodes (where it is still present today, as a substrate for the active gallium nitride). An increasing number of research studies are being undertaken examining the electronic applications of SiC semiconductors in hostile environments (such as sensors at very high temperature, radiation detectors, etc.), in the field of optoelectronics, and in the field of power electronics. Together with its high prohibited energy band, its critical electric field and its good thermal and electronic properties, the SiC semiconductor provides an attractive solution for meeting the new requirements of tomorrow's power systems.

To deal with applications of silicon carbide in power electronics, we felt it was necessary to give an overview regarding this "new" semiconductor material: its main properties and associated potentials, its technology and degree of maturity, the structures obtained so far and their performances, compared with the current power devices based on silicon.

First of all, remember that a few points on a technical level maintain doubts about the future of some branches of power components based on silicon carbide. The first is the quality of the material upon which in turn manufacturing impacts upon the yield (of substrates, epitaxy and components), the feasibility of high

current devices, and ultimately the reliability of the functions carried out and of course their cost. The second, is the existence of an insulating grid adapted to the operation conditions of SiC, and maintaining a good interface, in order to benefit from the theoretical advantages of this semiconductor. The third point relates to obtaining operational and reliable, switches with isolated commands. The same issue arises about the surface passivation of SiC, and more generally in terms of the materials needed to implement housing, including components intended to operate at high junction temperature (i.e. above 200°C). In addition to this blocking points, efforts are still required to improve the performance of components based on SiC and reinforce the technical and economic superiority of the systems using it. These improvements are particularly at the manufacturing level: such as doping control, increased speeds of low residual doping epitaxy, and the mastery of lifetime; but also the physical modelling of these new components. In addition, research also undertaken for the optimal design of their architectures and those of the converters which implement them, and their packaging, is continuing.

In terms of applications and expected progress, it is clear that silicon carbide is theoretically adapted, and probably also necessary to remain inline with the new requirements of electronic power systems: less energy consumption, more power supplied, more miniaturization (or "integration"), more functions (or "intelligence"), and more reliability. Current demonstrators already show (by structures which currently drive tens of amps) SiC's potential to extend the ratings in voltage, frequency and energy, beyond what silicon can achieve. This is done by reducing conduction and switching losses (by reducing or abolishing their causes), or by raising the threshold of tolerance of those losses by the semiconductor (through a higher allowed operating temperature).

The "high voltage" SiC Schottky diode, already a reality on the marketplace for a voltage range up to 600 V, corresponds to the first case (significant reduction of losses). The studies of implementation, in competition with bipolar silicon diode, show that its favored area of use is schematics, involving hard commutation at frequencies above 100 kHz. The extent of the voltage forecast range in the SiC Schottky diode family is 2-3kV within the horizon of two to three years. The high current ratings do not need necessarily large dimensions for substrates, as the Schottky diode is perfectly suited to the parallel setting. The maximum junction temperature of such components is still "classic", less than 200°C. The normally open-switch associated with the very fast silicon carbide diode remains, to this day, silicon; the emergence of a commercial component SiC MOSFET is postponed due to the technological difficulties mentioned above. New circuit topologies will probably emerge in order to benefit from the very interesting performance of "normally closed" switches such as SiC JFETs, which could also be available within two to three years. Note that MESFET type transistors dedicated to UHF and power microwave applications are already on the market (being based on a material whose

characteristics are easier to make). The exploitation of silicon carbide properties to significantly extend the voltage levels of lateral conduction structures (SiC solid material, or SiCOI, etc.), allowing the realization of genuine power integrated circuits, is another prospective major interest for low voltage applications, whose reality is still dependent on the technological advances of each component.

The issue of these devices is thus in the context of reducing dimensions (radiators, filters); increasing efficiencies of conversion, which promote miniaturization and autonomy of the systems of low and medium voltage; and reducing costs (including maintenance and infrastructure).

For applications beyond 4-5 kV wishing to increase their operating frequency, demonstrators in bipolar SiC diodes have shown their superiority to the existing competition (fast silicon bipolar diodes), in terms of speed, of direct current density, of temperature, and therefore power dissipation ability. Aspects concerning the operational reliability and availability of high current ratings (related to the quality of the material) remain unclarified. The marketing forecast for these components is, in the favorable case, estimated at five years at least. The emergence of SiC switches in this range of voltage and for high power applications (such as bipolar transistors, GTO thyristors, or their combination with command by gate isolated structures (IGBT transistors, MGT transistors, or else to be invented, etc.) is at best feasible in a similar period. Demonstrators remain today at low voltage and current ratings, but already attest their switching speed, their temperature strength and high current density, confirming the hopes of increasing the power density of systems.

Thus, there are a number of areas accessible to silicon carbide for which there is no competition, at least in the form of semiconductors components: such as applications at very high voltage (19 kV diodes with very low current have been demonstrated); applications under high temperatures; and static protection systems, with proof of the robustness under high energy of some structures (such as 600 V JFET transistors for the current limitation on the low-voltage grid). The consequences can look similar in this case to the famous 1960s revolution in power electronics; the introduction of semiconductors being in fact a considerable progress in terms of flexibility of command and control of systems, interactivity (even "communication") with their environment, and expanding the scope of their actions.

These are encouraging results and motivating prospects for the progress and innovation of domestic or industrial facilities, individual or collective transportation, production and management of energy, and telecommunications; for which fascinating research subjects remain to be discovered and discussed.

4.6. Acknowledgments

We can not conclude this chapter without expressing our gratitude to the people without whom we could not have written the lines above.

Our sincere thanks go first to men who, in the late 1980s, were at the foundation of French research dedicated to power components in SiC: mainly, Jean-Pierre Chante (Professor INSA Lyon), Pierre Merle (Professor at the University of Montpellier and head of the Group of Industrial and Research Centres in Power Electronics – GIRCEP), Michel Amiet (Officer of Technical Strategies and Common Technologies of the DGA) and Christian Parnière (former Director of the Research Group in Electronics at Schneider Electric).

We also deeply appreciate the research contribution of the cited authors: some of whose results have been repeated in this chapter.

We are also very grateful to the various people who have directly contributed to the results presented in this chapter, or who have spent time to discuss, correct its contents, or who have "supported" (in all senses of the term) this work, including: the "SiC" team members of AMPERE (Lyon), Frédéric Lanois (STMicroelectronics Tours), Hervé Morel (AMPERE), Henri Schneider (LAAS Toulouse), and also not forgetting our beloved families.

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