CASE 18

Parameter Design of Fine-Line Patterning for IC Fabrication

Abstract: We developed our research on the patterning process by including everything up to the actual process of forming metal circuits. More specifically, focusing on electrical characteristics as evaluation metrics, we investigated a circuit's ability to improve wire width stability and voltage and current characteristics simultaneously.

1. Introduction

To miniaturize the width of an electric wire is an essential technology not only for downsizing and high accumulation of integrated circuits (ICs) but also for performance enhancement of transistors. Currently, a 1.0-μm-wide wire is used as the smallest-width wire for a circuit on a printed circuit board. However, variability in the wire width causes fluctuation of a transistor's threshold voltage, and the ICs malfunction. Additionally, since the fluctuation of a transistor's threshold voltage is affected more by variability in width as the width decreases, to stabilize this is regarded as important in improving the degree of accumulation.

Until now we have focused especially on the patterning process in the IC manufacturing process, to improve the ability to pattern circuits from a mask to a photoresist using the line-and-space pattern of one-to-one wire width. Figure 1 shows the process that we researched. First, a photoresist applied onto a wafer was exposed to ultraviolet light through a mask. Only the exposed part of the photoresist was dissolved with solvent, and as a result, a pattern was formed. As a next step, after metal material was sputtered onto the patterned wafer, a metal pattern (circuit) was created through dissolution of the photoresist remaining.

On the other hand, considering that this experiment was also conducted to accumulate technical know-how that could be widely used, we laid out not only specific circuit patterns but also various patterns designed as shown in Figure 2, whose wire widths range from 0.4 to 1.2 μm in the middle and at the edge of the mask surface by grouping different types.

By utilizing simple patterns, we also tested the functionality of electrical characteristics of a pattern together with patternability in accordance with the wire width. We set the photoresist type, prebaking temperature, and developing time as control factors, assigned them to an L_{18} orthogonal array, and investigated the patternability. As a result, we found that exposure time, focusing depth, developing time, and descum time greatly affect patternability.

2. Evaluation Characteristics and Experiment

On the basis of our experimental results and experience, we selected four control factors and levels (Table 1). As a noise factor, we chose two pattern positions in the center and at the edge of the wafer. These factors were allocated to an L_9 orthogonal array. Although an L_{18} is recommended for this case in the field of quality engineering, we used an L_9 because we knew that there was no interaction among control factors. As evaluation characteristics, we selected the current and voltage characteristics of a circuit. More specifically, by setting the wire

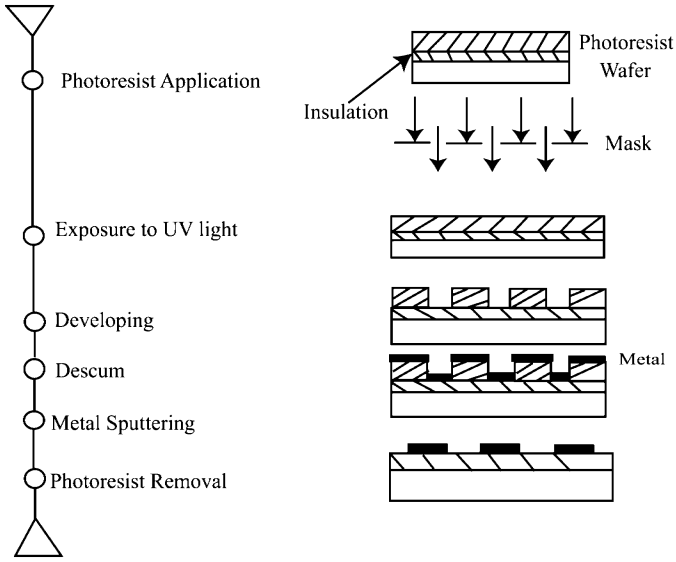

Figure 1
Patterning process

width as a signal factor M (with seven levels between 0.4 and 1.2 μm) and at a given voltage M^* (with seven levels between 0.5 and 4.0 V), we measured the current.

The resistance of a formed circuit is proportional to its length, L, and inversely proportional to its section area. On the other hand, the section area can be expressed by a wire width, M, and its height, t.

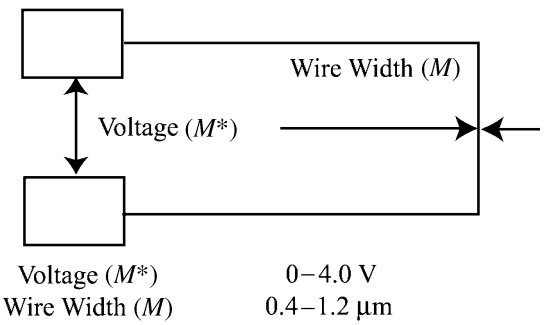

Figure 2
Mask pattern

In this experiment, since we fixed L and t, the resistance,

$$R = \frac{k}{m} \qquad \left(k = \frac{\rho L}{t}\right) \tag{1}$$

Thus, the current y flowing in the circuit is expressed as follows:

$$y = \frac{M^*}{R} = \beta M M^* \qquad \left(\beta = \frac{1}{k}\right) \tag{2}$$

The control factors were assigned to the inner L_9 orthogonal array, and the signal and error factors were allocated to the outer array. An example of the experimental data corresponding to the seventh row of the orthogonal array is illustrated in Table 2. Using these data, we calculated SN ratios and sensitivities as zero-point proportional dynamic characteristics through the origin by following the next procedure, as shown in Table 3:

$$S_T = 12.50^2 + 12.53^2 + 24.90^2 + \cdots + 40.25^2 = 162{,}302 \qquad (f = 98) \tag{3}$$

$$r = (2)\{[(1.2)(0.5)]^2 + [(1.2)(1.0)]^2 + \cdots + [(0.4)(4.0)]^2\} = 336.35 \tag{4}$$

Table 1
Control factors and levels

Control Factor	Signal 1	2	3
C: exposure time	Short	Middle	Long
D: focusing depth	Standard	Deep	Deeper
G: developing time	Short	Middle	Long
H: descum time	No	Yes	—

$$S_\beta = \frac{[(1.2)(0.5)(12.50 + 12.53) + \cdots + (0.4)(4.0)(41.98 + 40.25)]^2}{r} = 160{,}667 \qquad (f = 1) \tag{5}$$

$$S_e = S_T - S_\beta = 162{,}302 - 160{,}667 = 1635 \qquad (f = 97) \tag{6}$$

$$V_e = \frac{S_e}{n - 1} = \frac{1635}{98 - 1} = 16.86 \tag{7}$$

SN ratio:

$$\eta = 10 \log \frac{(1/r)(S_\beta - V_e)}{V_e} = 10 \log \frac{(1/336.35)(160{,}667 - 16.86)}{16.86} = 10 \log 28.3 = 14.52 \text{ dB} \tag{8}$$

Sensitivity:

$$S = 10 \log \frac{1}{r}(S_\beta - V_e) = 10 \log \frac{1}{336.35}(160{,}667 - 16.86) = 10 \log 477.63 = 26.79 \text{ dB} \tag{9}$$

3. Optimal Configuration

Based on the SN ratios and sensitivities illustrated in Table 3, the level-by-level computed averages of the SN ratio and sensitivity are as shown in Table 4 and in the factor effect diagram (Figure 3). According to Figure 3, the optimal configuration is $C_3D_1G_3H_2$. We estimated the process average by selecting two effective factors, *C* and *D*.

SN ratio:

$$\eta = \overline{C}_3 + \overline{D}_1 - \overline{T} = 8.92 + 10.37 - 6.18 = 13.11 \text{ dB} \tag{10}$$

Since the control factors and levels for our experiment did not include the values for the current, configuration, we conducted an extra experiment for the current, whose results are shown at the bottom of Table 3. The SN ratio of the current configuration is

$$\eta_0 = 8.29 \text{ dB} \tag{11}$$

The optimal configuration, $C_3D_1G_3H_2$, matches that of experiment 7, whose SN ratio is

$$\eta = 14.52 \text{ dB} \tag{12}$$

We summarize these calculations in Table 5.

Under the optimal configuration, we improved the gain by 6.23 dB compared with the current configuration. The most influential factors were exposure time and focusing depth, and the levels of standard and long for each factor brought us much improvement. This may be because the variability in wire width or defects of wire would be increased if we made focusing depth deeper and exposure time shorter.

4. Sensitivity Analysis

The resistance of a formed circuit can be expressed as follows with circuit length, *L*, wire width, *M*, wire height, *t*, and resistivity, ρ:

Table 2
Data for experiment 7 (mA)

		M_1^* (0V)	M_2^* (0.5 V)	M_3^* (1.0 V)	M_4^* (1.5 V)	M_5^* (2.0 V)	M_6^* (2.5 V)	M_7^* (3.0 V)	M_8^* (4.0 V)
M_1	Middle	0	12.50	24.90	37.12	49.10	60.71	71.91	92.87
(1.2 μm)	Edge	0	12.53	24.99	37.28	49.30	60.97	72.23	93.32
M_2	Middle	0	10.74	21.41	31.95	42.28	52.34	62.07	80.47
(1.0 μm)	Edge	0	10.77	21.49	32.06	42.44	52.55	62.33	80.77
M_3	Middle	0	9.210	18.38	27.42	36.32	45.01	53.45	69.44
(0.8 μm)	Edge	0	9.246	18.46	27.56	36.51	45.25	53.75	69.84
M_4	Middle	0	8.525	17.00	25.36	33.61	41.65	49.49	64.39
(0.7 μm)	Edge	0	8.528	17.00	25.37	33.62	41.68	49.51	64.43
M_5	Middle	0	7.746	15.46	23.09	30.61	37.96	45.14	58.82
(0.6 μm)	Edge	0	7.762	15.48	23.11	30.63	37.99	45.18	58.88
M_6	Middle	0	6.864	13.71	20.48	27.15	33.70	40.11	52.36
(0.5 μm)	Edge	0	6.824	13.61	20.32	26.96	33.46	39.82	52.00
M_7	Middle	0	5.461	10.91	16.30	21.65	26.90	32.05	41.98
(0.4 μm)	Edge	0	5.222	10.43	15.61	20.73	25.77	30.71	40.25

Table 3
Assignment and analysis of control factors (dB)

	Column and Factor					
No.	1 *C*	2 *D*	3 *G*	4 *H*	SN Ratio	Sensitivity
1	1	1	1	1	8.13	24.69
2	1	2	2	2	4.34	24.18
3	1	3	3	1′	−1.60	21.29
4	2	1	2	1′	8.46	25.02
5	2	2	3	1	8.46	25.23
6	2	3	1	2	1.15	25.39
7	3	1	3	2	14.52	26.79
8	3	2	1	1′	8.12	26.44
9	3	3	2	1	4.11	25.03
Current configuration					8.29	25.22

Table 4
Level-by-level averages of SN ratio and sensitivity (dB)

	SN Ratio			Sensitivity		
Factor	**1**	**2**	**3**	**1**	**2**	**3**
C	3.62	6.01	8.92	23.39	25.21	26.10
D	10.37	6.96	1.22	25.50	25.28	23.92
G	5.80	5.64	7.11	25.50	24.76	24.44
H	5.94	6.67	—	24.62	25.45	—
Average		6.18			24.90	

$$R = \frac{\rho L}{tM} \tag{13}$$

When $\rho = 2.2 \times 10^{-5}\ \Omega \cdot \text{mm}$, $L = 1.12$ mm, and $t = 0.0005$ mm, the resistance is

$$R = \frac{0.004928}{M} \tag{14}$$

If the wire width, $M = 1.0$ μm and the voltage, $M^* = 1.0$ V, the current is

$$y = \frac{M^*}{R} = \frac{1.0}{(0.004928)(0.001)} = 0.02029 \text{ A} = 20.29 \text{ mA} \tag{15}$$

Therefore, the target value of the sensitivity is

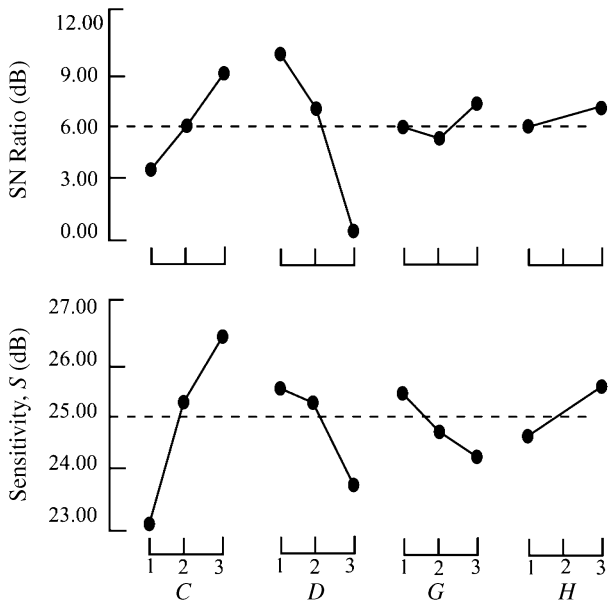

Figure 3
Response graphs

Table 5
SN ratio comparison of optimal and current configurations (dB)

	Configuration		
	Optimal	**Current**	**Gain**
Estimation	13.11	—	—
Configuration	14.52	8.29	6.23

$$S = 10 \log 20.29^2 = 26.15 \text{ dB} \quad (16)$$

Under the optimal configuration the sensitivity is

$$S = \overline{C}_3 + \overline{D}_1 - \overline{T} = 26.10 + 25.50 - 24.90$$
$$= 26.70 \text{ dB} \quad (17)$$

This reveals that the target and optimal values of sensitivity are consistent. Although we concluded that we do not need to adjust the sensitivity, when needed we can regulate using the exposure time, C, which affects sensitivity relatively more than the SN ratio does.

This study revealed that we can develop manufacturing conditions to form wires of fine width with little variability and confirm a fundamental principle for stabilizing voltage and current as basic functions of a circuit. This also demonstrates that it is possible to evaluate two signal factors of patternability β and functionality β^* at the same time, whereas traditionally each has been analyzed separately.

Reference

Yosuke Goda and Takeshi Fukazawa, 1993. Parameter design of fine line patterning for IC fabrication. *Quality Engineering*, Vol. 1, No. 2, pp. 29–34.

This case study is contributed by Takeshi Fukazawa and Yosuke Goda.