6

ELECTRONIC DEVICES: DIODES, BJTs, AND MOSFETs

6.1 INTRODUCTION TO ELECTRONIC DEVICES

Diodes, bipolar junction transistors (BJTs), and metal oxide field effect transistors or MOSFETs are the most common and most important electronic devices in use today. The junction field effect transistor or JFET is the predecessor of the MOSFET. Due to space reasons we will not address the JFET. This chapter presents to the reader the most basic and important considerations from a circuit analysis point of view of how to deal with diodes and transistors in the most common hardware applications. Some of such applications are: how do basic single-stage amplifiers work; how can we calculate the correct value of a resistor to correctly turn on a light-emitting-diode or LED; what are open collector and open drain outputs; why do we need them; how do we calculate the correct pull-up resistor value; and how do we increase the current drive capability of an integrated circuit output that needs to drive multiple chips or other discrete circuits. This chapter focuses on the characteristics and use of the three devices of our chapter title, their behavior, and their use in the most basic circuits that scientists and engineers need to know. It is not within the scope of this book to study electronic devices semiconductor physics concepts. Only a minimum of semiconductor physics will be addressed in particular when we cover MOSFETs. We generally take an approach of studying the

Electrical, Electronics, and Digital Hardware Essentials for Scientists and Engineers, First Edition. Ed Lipiansky.

electronic device, knowing its current–voltage relationship and its small signal model for AC analysis.

6.2 THE IDEAL DIODE

The diode is the simplest and most fundamental electronic device. Its idealized model describes the diode as a two-terminal device that acts like a mechanical switch. When the switch is closed, the ideal diode has a *zero-ohm* forward resistance. When the switch is open, the ideal diode has an infinitely large reverse resistance. Figure 6.1a shows the electronic symbol of a diode, indicating its two terminals, the *anode* (*A*) and the *cathode** (*K*). When the current through the diode flows from *anode* to *cathode*, the diode is said to be forward biased or *ON*. When a diode is forward biased, an external element in the circuit, such as a series resistor, is responsible for limiting the amount of current that flows through the turned-on diode. When the current through the diode intends to flow from *cathode* to *anode*, the diode is said to be reversed biased or *OFF*. Figure 6.1b shows the model of an ideal diode turned *ON*. While Figure 6.1c shows the model of an ideal diode turned *OFF*. Figure 6.1d depicts the ideal diode model *I-V* (current–voltage) characteristics. The bold positive current shown in Figure 6.1d represents the diode operating in a forward biased mode, that is the current flows through the diode from *anode* to *cathode*; this means that the *anode* is at a *higher* potential than the cathode. The external circuit must limit the forward current that flows through a forward biased diode; otherwise the diode would get destructed if such current was not limited. This portion of the forward biased region also indicates to us that the ideal diode forward voltage drop is zero. When the diode is in reverse biased mode, no current flows through the diode. The external circuit also limits the voltage across a reverse biased diode.

The diode *I-V* characteristic is nonlinear, thus the diode is a nonlinear element. Figure 6.1d shows the nonlinear characteristic formed by two linear segments; it is also appropriate to refer to such characteristic as piecewise linear. When the diode is used at a particular operating point, although the diode is a nonlinear device, it is possible and accurate to analyze the diode as a linear circuit element for such application.

Figure 6.2a shows a forward biased ideal diode. The current through this ideal diode equals the voltage applied divided by the series resistance, in our case 10 V/100 Ω = 1 mA. The forward biased diode has a zero *ON* or *forward resistance*.

The reverse biased diode of Figure 6.2b does not allow any current flow, and it has a –10 V reverse voltage applied across its *cathode* and *anode*. The

* Cathode derives from the Greek word “Kathodes”, that is why it is traditionally abbreviated with the letter “K.”

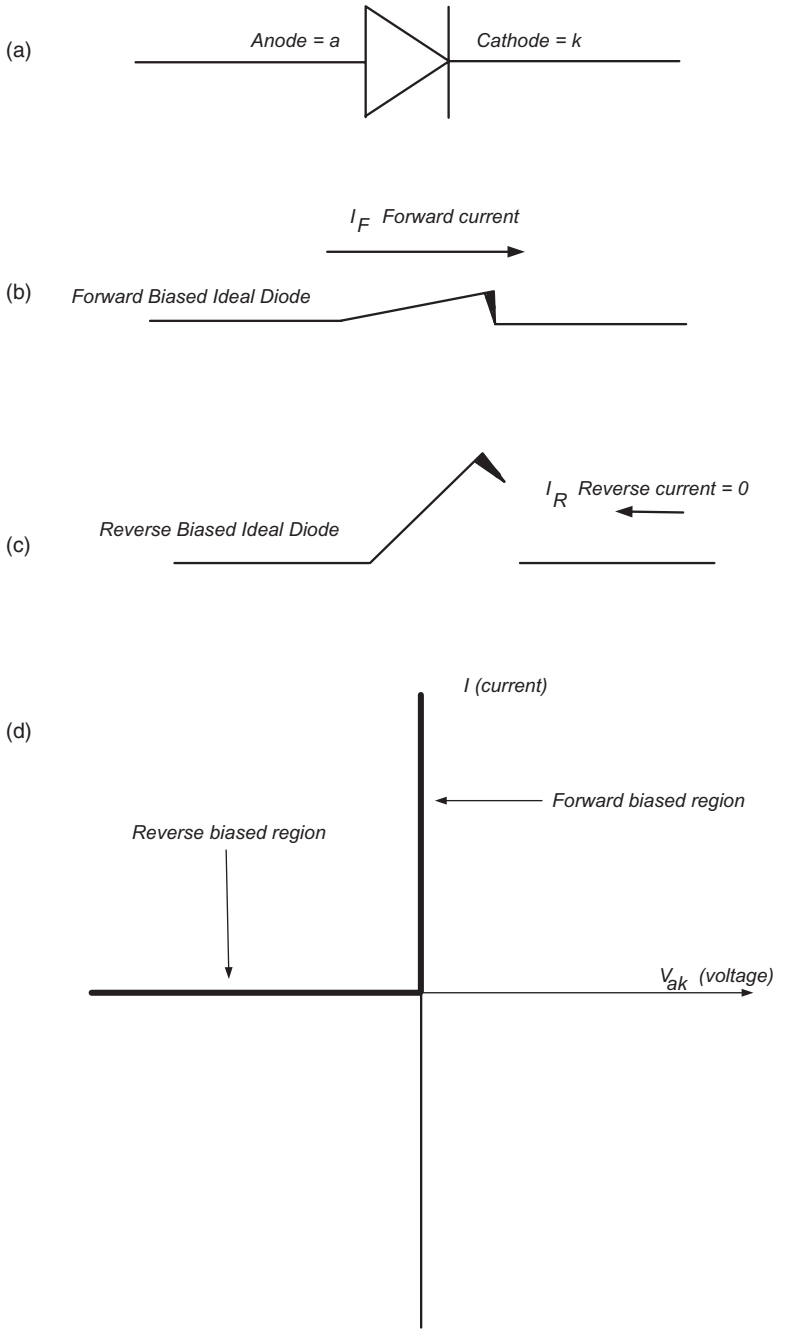

Figure 6.1 The ideal diode: (a) diode circuit symbol; (b) ideal diode turned *ON*; (c) ideal diode turned *OFF*; (d) ideal diode I-V characteristic.

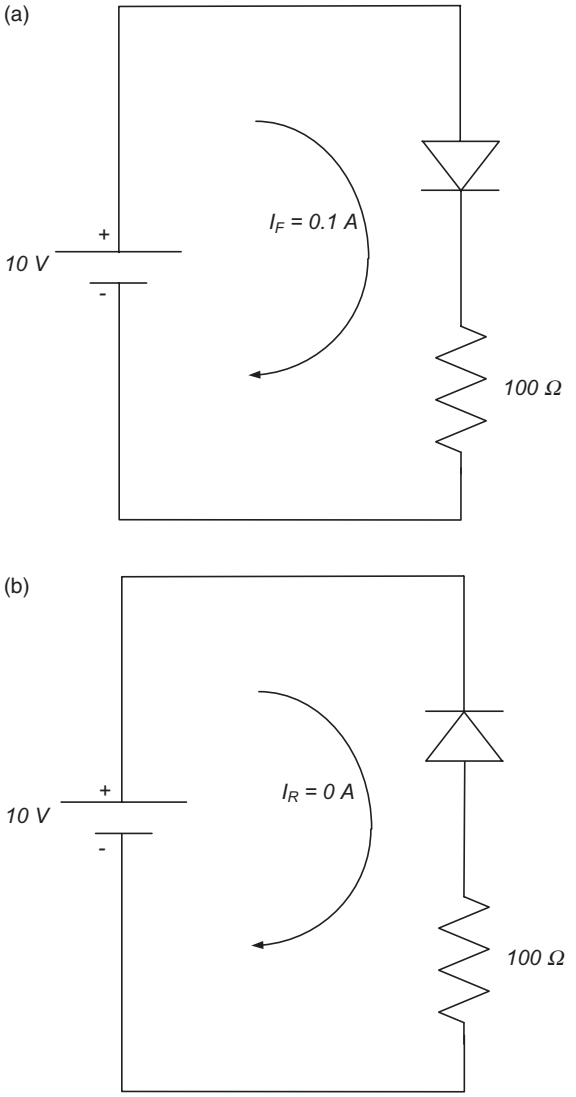

Figure 6.2 (a) Forward biased ideal diode; (b) reverse biased ideal diode.

reverse biased diode has an infinite resistance so that no current can flow through the circuit under those conditions.

6.2.1 The Half-Wave Rectifier

A half-wave rectifier consists of a diode and a resistor in series; a sinusoidal input waveform is applied between the diode anode and the free end of the resistor. The output voltage is taken across the resistor. Figure 6.3a shows

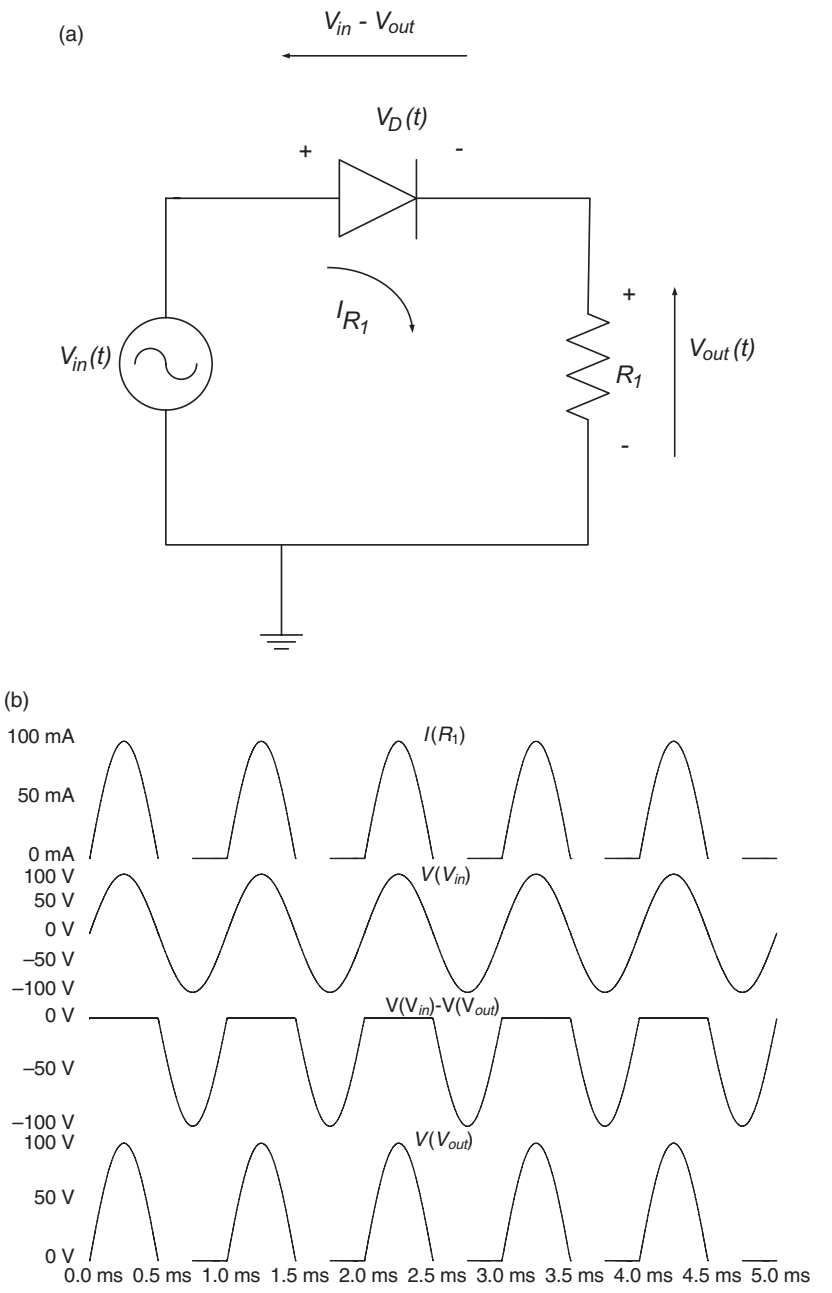

Figure 6.3 (a) Half-wave rectifier; (b) half-wave rectifier waveforms: $I_R(t)$, $V_{in}(t)$, $V_{out}(t)$, and $V_D(t) = V_{in}(t) - V_{out}(t)$.

a half-wave rectifier circuit. Figure 6.3b depicts the current $i(t)$ through the circuit, the sinusoidal input voltage waveform $V_{in}(t)$; the voltage $V_D(t)$ the *anode-to-cathode* voltage across the diode; the voltage $V_R = V_{out}(t)$ across the resistor

Let us describe how the circuit of Figure 6.3a works. Let us refer to the waveforms of Figure 6.3b. When the sinusoidal input voltage $V_{in}(t)$ is greater than zero, the diode becomes forward biased; this occurs for input phase angle ranges: 0 to π, 2π to 3π, 4π to 5π, which according to Figure 6.3b respectively correspond from 0 to 0.5 ms, 1 to 1.5 ms, 2 to 2.5 ms, and so forth. Note that for our specific waveform, its period 2π equals 1 ms. When the ideal diode is forward biased, the voltage drop across it is zero; refer to waveform $V_D(t) = V_{in} - V_{out}$, for time segments from 0 to 0.5 ms, 1 to 1.5 ms, 2 to 2.5 ms, and so forth. When $V_{in}(t)$ is negative, the diode is an open circuit because it becomes reverse biased; the voltage $V_D(t)$ across the diode is the negative cycle of the input sine-wave for phase angles of 1π to 2π, 3π to 4π, 5π to 6π (equivalently 0.5 to 1 ms, 1.5 to 2 ms, 2.5 to 3 ms), and so forth. The output voltage $V_{out}(t)$ across resistor R is equal to the positive half cycle of the input for phase angle ranges: 0 to π, 2π to 3π, 4π to 5π (equivalently for 0 to 0.5 ms, 1 to 1.5 ms, 2 to 2.5 ms), and so forth. For phase angles: 1 to 2π (0.5 to 1 ms), etc., the voltage across resistor R is zero. Finally, the current through the circuit has to have the same shape as the voltage across the resistor, because the resistor is a linear component. Now let us recall Kirchhoff's laws from earlier chapters. By inspection of the circuit of Figure 6.3a, Kirchoff's voltage law (KVL) affirms that

$$V_{in}(t) = V_D(t) + V_R. \tag{6.1}$$

Carefully examining the waveforms of Figure 6.3b, it is easy to verify that Equation (6.1) is met. This tells us that both linear and nonlinear circuits meet KVL. This is a very powerful statement, particularly since diodes did not exist during Kirchhoff's times.

Once more note the shapes of the current $i(t)$ and the voltage $V_{out}(t)$'s first and last waveforms of Figure 6.3b have the same shape. Current $i(t)$ is unidirectional and positive. If we eliminated the diode with a short-circuit current $i(t)$ would be sinusoidal, because only the source and the resistor are present in the circuit. We are just one simple next step away from obtaining a DC voltage level across resistor R. This is achieved by placing a capacitor of the appropriate value across load resistor R. Figure 6.4 shows the output waveform across the load resistor for capacitance values of: 5 μF, 10 μF, and 50 μF. Note that the larger the capacitor, the smoother is the DC waveform obtained. In all cases, the DC waveform is not a perfect horizontal straight line, it is rather a waveform that exhibits ripple. One can reduce the ripple by incrementing the capacitor size; however, the ripple cannot be completely eliminated.

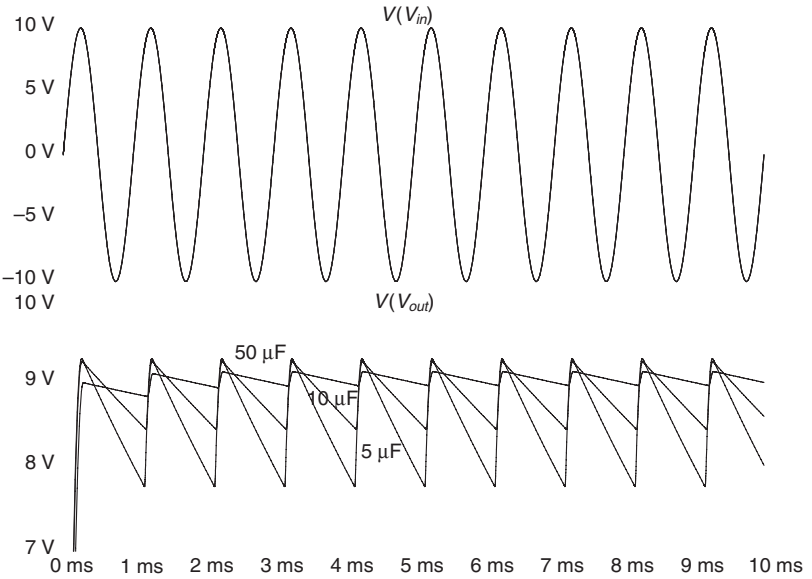

Figure 6.4 Half-wave rectifier with smoothing capacitor to reduce ripple.

6.2.2 The Full-Wave Bridge Rectifier

The circuit of Figure 6.3a rectifies only half of the sinusoidal input waveform. This means that only the positive half of the sinusoidal cycle is preserved, the negative half cycle becomes zero at the load resistor; this is assuming that there is no filtering capacitor across resistor R. The circuit of Figure 6.5a shows a four-diode bridge excited by a sinusoidal input V_{in} and the load resistor R across terminals V_{out} and V_{out_Ret}.

The circuit works as follows: when V_{in} is positive, signs in Figure 6.5a apply, diodes D_1 and D_2 conduct current through the circuit established between a positive V_{in}, D_1, R, and D_2. D_1 and D_2 are at this time forward biased, since for ideal diodes, the forward voltage drop is zero, drops across D_1 and D_2 are zero during this first half-period. Diodes D_3 and D_4 remain reversed biased at this time. The current through resistor R flows from terminal V_{out} to V_{out_Ret}, thus V_{out} is at a higher potential than V_{out_Ret}. The difference V_{out}-V_{out_Ret} is another form of referring to the voltage across resistor R where node V_{out} is more positive than node V_{out_Ret}. When V_{in} is negative, signs are opposite to those shown in Figure 6.5a, diodes D_3 and D_4 are forward biased, while D_1 and D_2 are reversed biased. The current flows from V_{in}, through D_3, R, and D_4. Note that this time, the current through R also flows from node V_{out} to V_{out_Ret}. The waveform obtained across resistor R terminal is referred to as a full-wave rectified sine wave. Figure 6.5b shows waveforms V_{in} and V_{out}-V_{out_Ret} the voltage across resistor R.

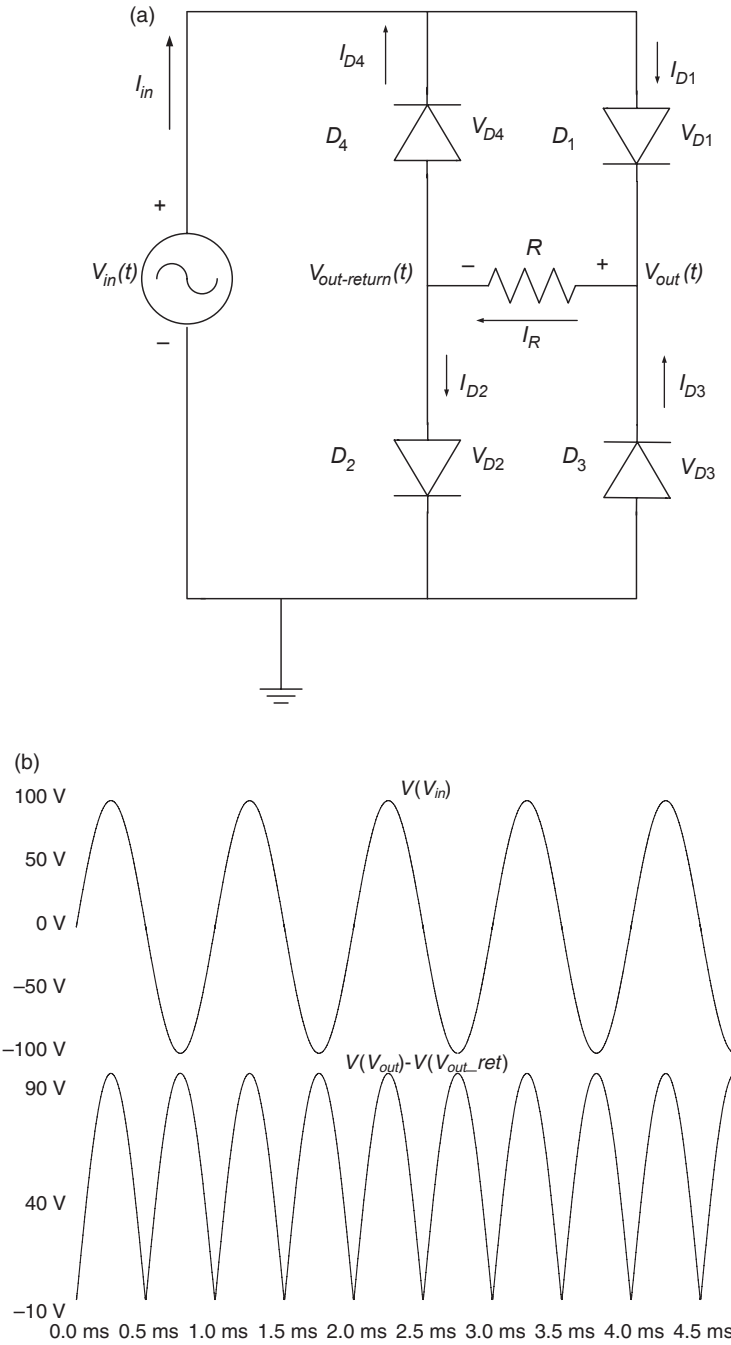

Figure 6.5 (a) Full wave rectifier; (b) voltage waveforms: V_{in} and $V_D = V_{out} - V_{out\_Ret}$; (c) current waveforms through four diodes: I_{D1}, I_{D2}, I_{D3}, I_{D4} and load current I_R.

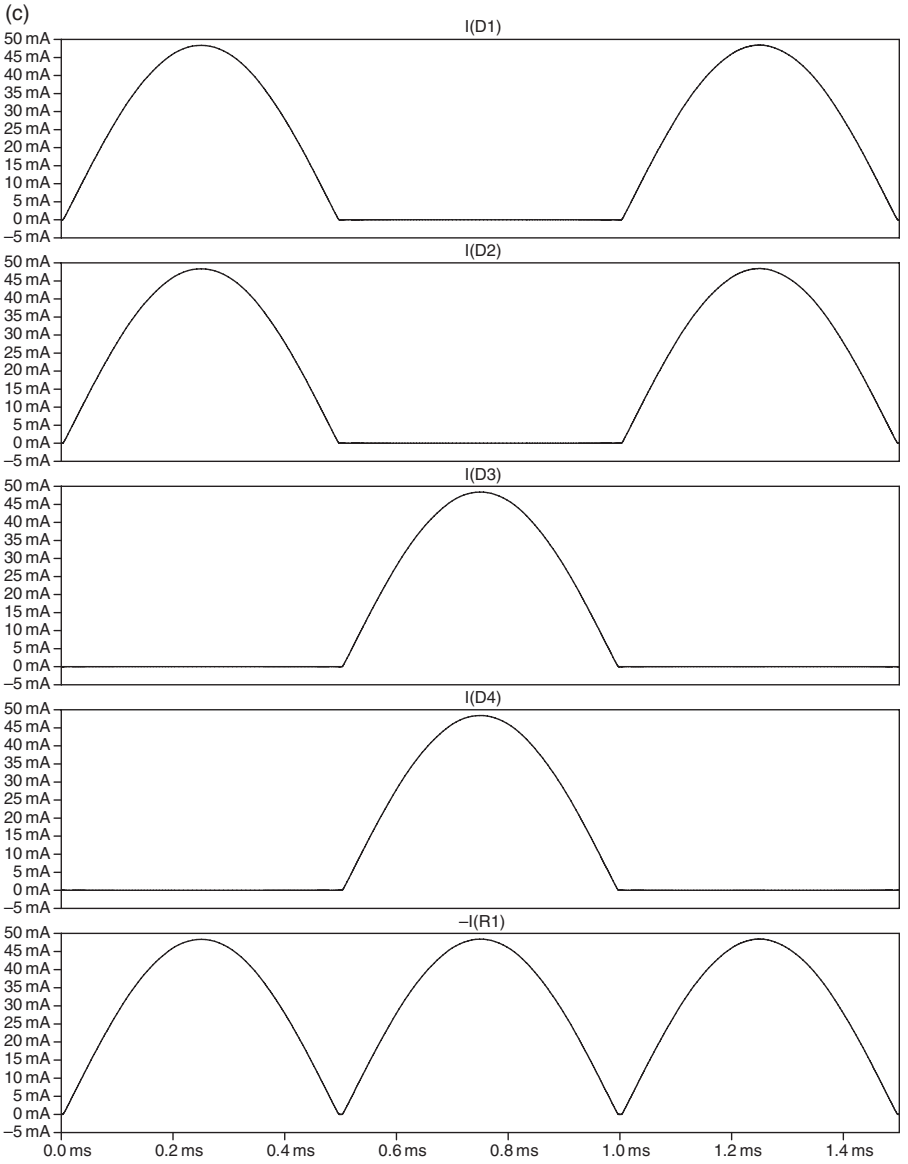

Figure 6.5 (*Continued*)

Continuing to look at the four-diode bridge circuit, we now take a look at the currents that flow through everyone of the circuit elements, the input voltage source, each of the four diodes, and load resistor R. Figure 6.5c shows the current waveforms through each diode I_{D1}, I_{D2}, I_{D3}, and I_{D4}, and the current waveform on load resistor R, I_R. It is very interesting again to find that all the

currents comply with Kirchoff's current law (KCL). Similarly, it can be shown that the voltages across every one of the circuit elements also comply with KVL.

Carefully observe the current waveforms of Figure 6.5c: I_{D1}, I_{D2}, I_{D3}, $I_{D4,}$ and I_R. It is important to refer to the circuit of Figure 6.5a to observe the direction of every current every diode and load resistor. Plot the current waveform I_{in} of the sinusoidal input source V_{in}.

Example 6.1 Draw all the voltage waveforms for the full wave rectifier circuit of Figure 6.5a. Such waveforms are: V_{in}, V_{D1}, V_{D2}, V_{D3}, $V_{D4,}$ and V_R. Figure 6.6 presents all the waveforms requested. Note that at every node on the circuit, KVL is met. For example:

$$V_{in} = V_{D1} - V_{D3}$$

which is also equivalent to:

$$V_{in} = V_{D1} + V_R + V_{D2}.$$

Note that in Figure 6.6:

$V_{D1} = V_{in} - V_{out}$: is the voltage across diode 1
$V_R = \mathrm{V_{out}} - \mathrm{V_{out\_ret}}$: is the voltage across load resistor R
$V_{D2} = V_{out\_ret} - \mathrm{GND} = V_{out\_ret}$: is the voltage across diode 2
$V_{D3} = -V_{out}$: is the voltage across diode 3
$V_{D4} = V_{out\_ret} - V_{in}$: is the voltage across diode 4

Voltages across diodes have been defined as the difference between the anode and the cathode voltages.

The reader is encouraged to graphically add the appropriate waveforms to verify the validity of KVL. Beware of the plotted waveform polarites.

6.2.3 The Real Silicon Diode *I-V* Characteristics: Forward-Bias, Reverse-Bias, and Breakdown Regions

A real diode has an *I-V* characteristic as depicted by Figure 6.7. On the first quadrant, for positive anode-to-cathode voltage and current, the diode does not start conducting in its forward biased region until the forward voltage exceeds approximately 700 mV. After this voltage level is exceeded the diode conducts, and the diode external circuit only limits the current through it. In many cases, this external circuit is a resistor in series with the diode. The equation that models the behavior of the current through a diode as a function of its voltage is

$$\mathrm{i}_D(t) = I_S(\mathrm{e}^{V_D/nV_T} - 1) \tag{6.2}$$

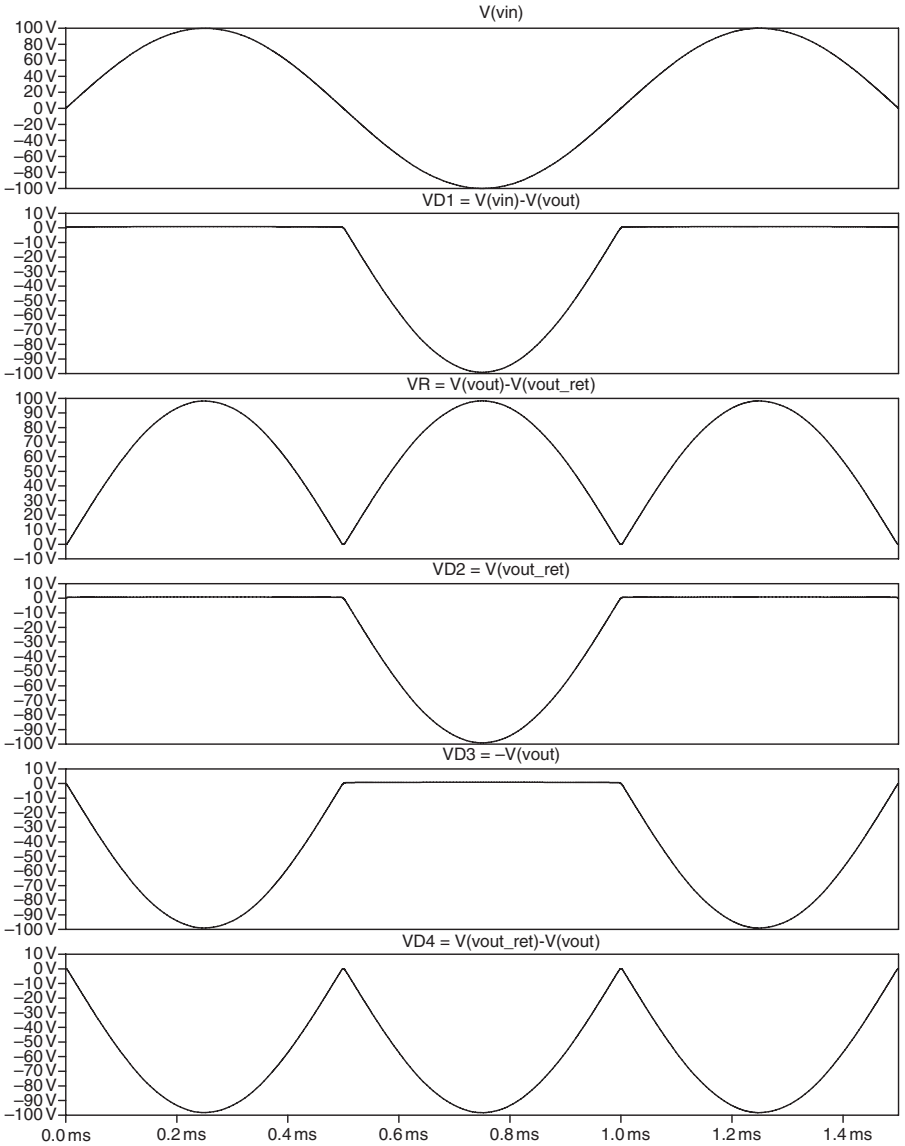

Figure 6.6 Voltage waveforms in full-wave rectifier: input voltage, voltages across four diodes, and voltage across the load.

Equation (6.2) describes the current through the diode. I_S is the diode saturation current, V_D is the anode-to-cathode voltage across the diode, n, the emission coefficient is a constant that is usually 1 for integrated circuit diodes and $n = 2$ for discrete diodes. V_T, the thermal voltage is defined from physical considerations as:

$$V_T = \frac{kT}{q} \tag{6.3}$$

where

k = Boltzmann's constant = 1.38×10^{-23} J/K
T = the absolute temperature in kelvin = 273 + temperature in °C
q = the magnitude of electronic charge = 1.60×10^{-19} C.

The thermal voltage V_T is approximately 26 mV at a room temperature of 300 °K.

The diode forward voltage drop has a negative temperature coefficient, which is

$$\frac{\Delta V_D}{V_T} = -2 \text{ mV} / °\text{C}. \tag{6.4}$$

Equation (6.4) tells us that for every degree C in temperature rise of the diode junction, its forward voltage drop decreases by 2 mV. This property of Silicone diode junctions is typically used to know the internal temperature of integrated circuits.

Referring again to Figure 6.7, we see that the forward current of the diode is negligible for voltages below about 0.5 V.

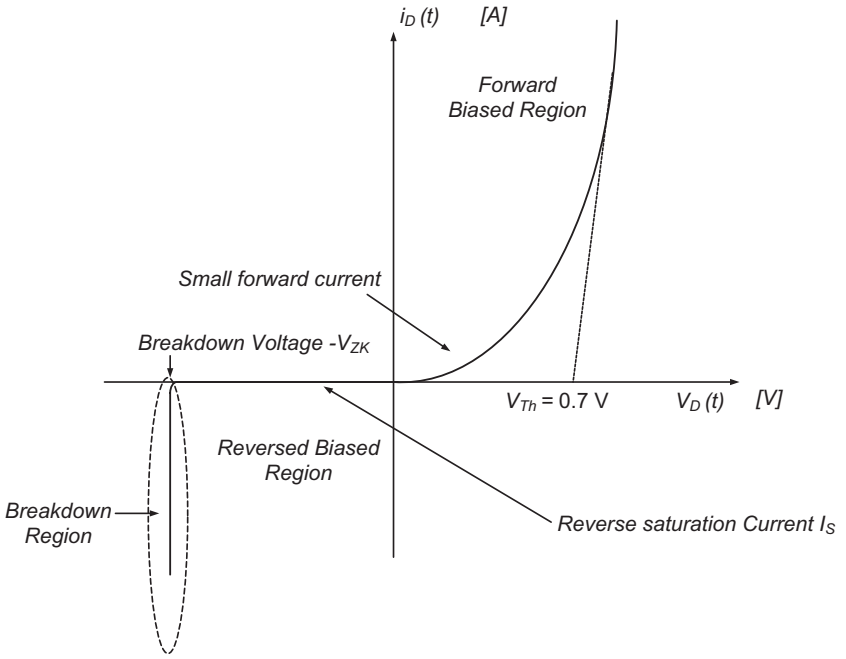

Figure 6.7 Diodes: three regions of their *I-V* characteristics:
For $V_D > 0$ the diode is in the forward-bias region, conducts significant current once $V_D > V_{Th}$
For $-V_{ZK} < V_D < 0$ the diode is in the reverse-bias region
For $V_D < -V_{ZK}$ the diode is in the breakdown region.

The current starts having significant value once a diode forward voltage threshold of approximately 0.6 V–0.7 V is reached.*

When the diode voltage V_D is negative the exponential term in Equation (6.2) becomes very small compared to the constant 1, thus Equation (6.2) becomes

$$i_D(t) \cong -I_S \tag{6.5}$$

where I_S is also referred to as the reverse bias saturation current. Current I_S has a positive temperature coefficient and it approximately doubles for every 10°C of temperature rise. This current is quite constant as the reverse bias voltage varies, and the temperature does not change (see Fig. 6.7, reverse-bias region). I_S can be in the order of 10^{-14} to 10^{-15} A. As V_D continues to decrease (i.e., becomes larger in magnitude but negative in sign) the diode enters the breakdown region. The voltage $-V_{ZK}$ is denoted the Zener voltage knee. Regular diodes are not designed to be operated in the breakdown region; however, another type of device, the Zener diode, is purposely designed to operate in the breakdown region. At a reverse voltage of $-V_{ZK}$, the diode characteristic is a virtual straight line (Fig. 6.7) so that means that within a range of reverse current, the voltage remains practically within a very small variation. Zener diodes are particularly used in voltage regulators.

Example 6.2 A silicon diode has the following characteristics:

Reverse saturation current at 20 V and 25°C = 25 nA.

Using Equation (6.2), determine the diode forward voltage drop for forward diode currents of (a) 5 mA, (b) 10 mA, (c) 20 mA, (d) 100 mA, and (e) 300 mA. This diode is fabricated so that it can conduct safely a current as high as 300 mA. Assume that the diode emission coefficient n is 2.

Using Equation (6.2) and a thermal voltage of 26 mV at 25°C we find:

(a) At 5 mA, $V_D = 2 \times 0.026 \ln [5 \times 10^{-3}/25\ 10^{-9}] = 0.630$ V
(b) At 10 mA, $V_D = 2 \times 0.026 \ln [10 \times 10^{-3}/25\ 10^{-9}] = 0.670$ V
(c) At 20 mA, $V_D = 2 \times 0.026 \ln [20 \times 10^{-3}/25\ 10^{-9}] = 0.710$ V
(d) At 100 mA, $V_D = 2 \times 0.026 \ln [100 \times 10^{-3}/25\ 10^{-9}] = 0.790$ V
(e) At 300 mA, $V_D = 2 \times 0.026 \ln [300 \times 10^{-3}/25\ 10^{-9}] = 0.850$ V

Note that for forward currents of 5 mA up to 300 mA, the increase in current is by a factor of 60 or 6000%, the diode forward voltage drop just increases by 220 mV or by 35%.

Why? The answer is to be provided by the reader.

* Power diodes, which are larger than general purpose and signal diodes, may have significantly higher forward drop voltages. It is not uncommon to see 1 V or more of forward voltage drop on a power diode.

6.2.4 Two More Realistic Diode Models

We have seen that the *I-V* characteristic of the diode is very steep when the diode forward voltage drops exceeds 600 mV. Thus, a better model than the ideal diode model can be produced taking into account the 600 mV forward diode drop. Figure 6.8a shows a circuit that models the diode with more realism than the idealized model of Figure 6.1. The 600 mV DC source in series with the diode, opposes the flow of current until the diode anode voltage is strictly greater than 600 mV with respect to the negative terminal of the 600 mV DC source. Figure 6.8b depicts the current–voltage characteristics of such diode model. This model is better than the ideal diode model because it takes into consideration a voltage forward drop of 600 mV. Let us remember that one of the most realistic equations used to model the real diode was the one given by Equation (6.2). Such equation takes into account thermal voltage, diode forward voltage drop, emission coefficient n, reverse saturation current I_S, which is used for the forward and reverse-bias regions.

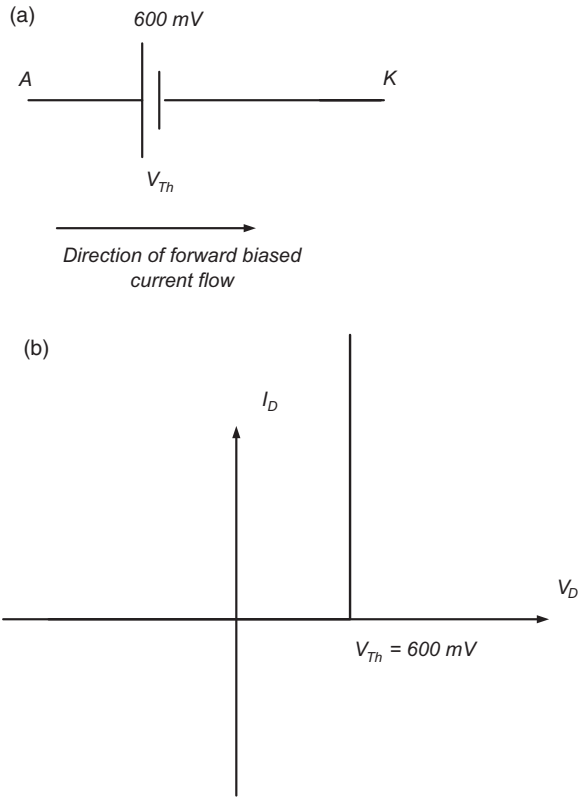

Figure 6.8 (a) A better ideal diode model including the forward voltage drop; (b) *I-V* characteristics of such diode model.

An even better model than the one presented in Figure 6.8 is one that models the forward voltage drop with a line that starts at zero current at 600 mV and has a positive slope that mimics the diode finite inverse of its forward resistance ($1/r_D$).

Figure 6.9a shows the circuit model including the 600 mV forward drop and diode forward resistance. Figure 6.9b depicts the *I-V* characteristics of such model. Such model is called the diode piecewise linear model. For the diode in reversed bias mode, the model is still an open-switch, not shown in Figure 6.9.

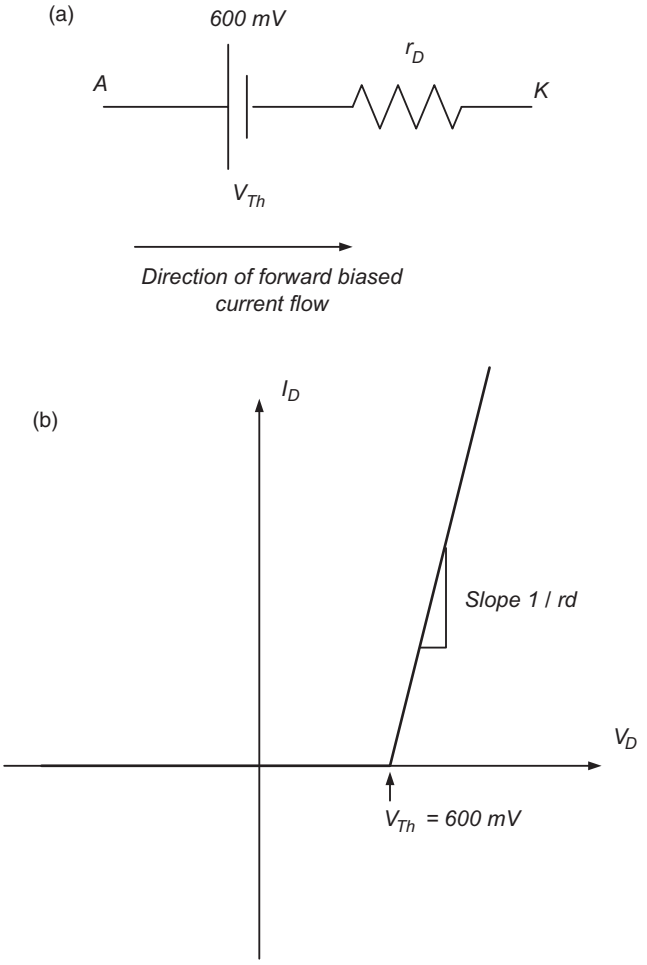

Figure 6.9 (a) Forward biased diode model including forward drop and forward resistance; (b) diode model *I-V* characteristics.

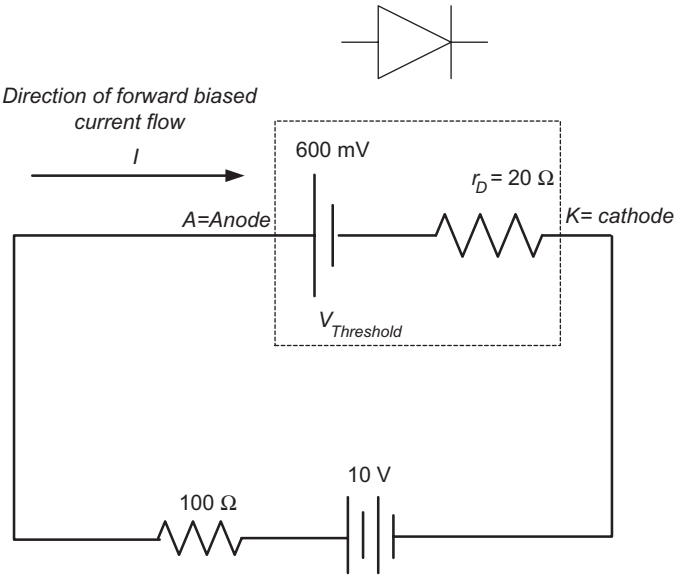

Figure 6.10 Circuit for Example 6.3: DC source in series with diode model.

Example 6.3 Assuming the diode model of Figure 6.9 find the forward current of the diode that has the following characteristics: $r_D = 20\ \Omega$, forward voltage modeling source 600 mV. Use the circuit of Figure 6.10.

From Figure 6.10 we can state the following circuit equation:

$$V_{in} - V_D = \mathrm{I}r_D + IR. \tag{6.6}$$

Using the numerical values from the circuit we obtain:

$$10 - 0.6 = \mathrm{I}(20 + 100). \tag{6.7}$$

From Equation (6.7) we obtain $I = 0.078$ A.

6.2.5 Photodiode

An incident light on a reverse-biased photodiode causes a flow of current through the photodiode. Basically a photon of sufficient energy hitting the photodiode causes an electron to become mobile, causing a photocurrent.

The symbol of a photodiode is presented in Figure 6.11.

6.2.6 Light Emitting Diode (LED)

An LED basically works in the opposite way a photodiode works. A forward current flowing through an LED causes the LED to emit photons or light.

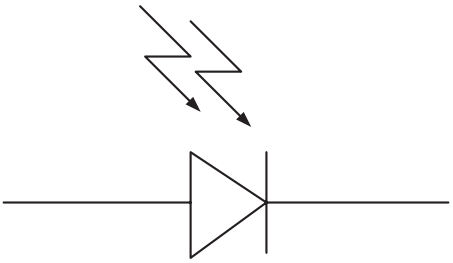

Figure 6.11 Symbol of a photodiode.

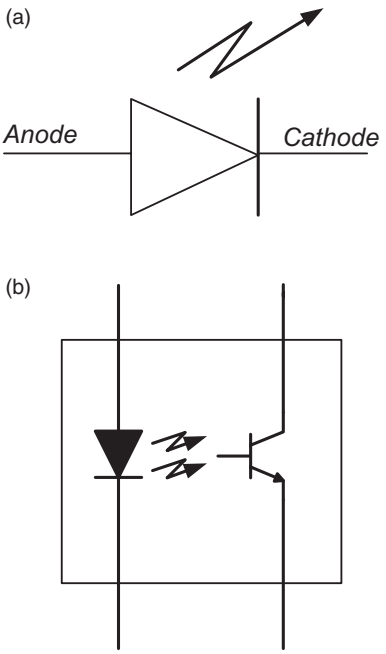

Figure 6.12 (a) LED symbol; (b) optoisolator symbol.

Figure 6.12a depicts the circuit symbol of an LED. A combination of a photodiode and an LED in the same integrated circuit package constitutes what is referred to as an optoisolator. The LED part of the opto converts an electrical signal into light. The photodiode portion receives the light emitted by the LED and produces an electrical signal. Figure 6.12b shows the circuit symbol of a typical optoisolator. This device is suitable to perform electrical-isolation between the input and output of the optoisolating device. This can be done to reduce electronic noise from propagating from one electronic stage to another, or for safety reasons such as in the case of medical instruments. The optoisolator can also be used to reduce the propagation of electromagnetic interference (EMI) in a communication system.

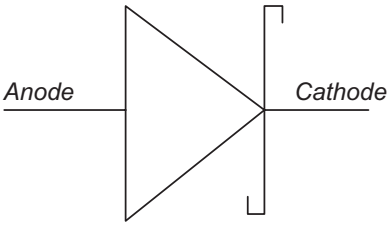

Figure 6.13 Circuit symbol of a Schottky-barrier diode.

6.2.7 Schottky-Barrier Diode

The Schottky-barrier diode is formed by making a metal to *n*-type semiconductor junction. This is unlike a regular junction diode that consists of a semiconductor-to-semiconductor junction formed with *n*-type and *p*-type material. The metal part of the Schottky works as the anode, while the semiconductor part is the cathode. A very distinct characteristic of Schottky-barrier diodes is their much lower forward voltage drop, usually around 200–300 mV. However, there is penalty for using a Schottky diode, their reverse saturation current is two to three orders of magnitude larger than that of their junction diode counterparts. Figure 6.13 shows the circuit symbol of a Schottky-barrier diode.

6.2.8 Another Diode Application: Limiting and Clamping Diodes

Junction and Schottky diodes are good devices to protect integrated circuits inputs. *IC* inputs usually must not be allowed to make voltage levels swings above the *IC* upper power supply rail or below the lower power supply rail. The lower supply rail on cases where the *IC* is only powered by a single positive power supply is the return or ground of that rail.

Example 6.4 Figure 6.14 shows an *IC* powered to a voltage called V_{DD} and V_{SS}. In many cases, V_{DD} can be 3.3 V and V_{SS} 0 V or ground. Diode D_1 protects the input of the *IC* from exceeding a voltage higher than its V_{DD} power supply level. Diode D_2 protects the input from going below the 0 V level. In other words, it prevents the input from going very negative. The purpose of the clamping or limiting diodes is to protect the *IC*. Note that the input line of the protected *IC* may be driven by another *IC* or circuit, the series resistance *R* in line between the input and the common node between diodes D_1 and D_2 is to prevent a large current surge when the input either is well above V_{DD} or well below V_{SS} (ground). Now let us recall that real diodes have a finite and non-zero forward voltage drop. The diode D_1 protection is actually limited to

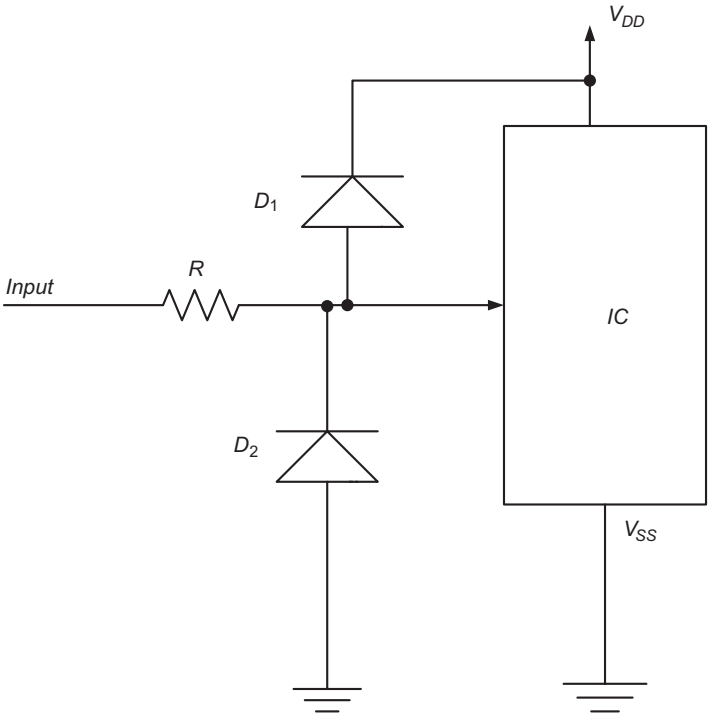

Figure 6.14 Diodes clamping the inputs of an *IC*.

clamping the input to $V_{DD} + V_D$, where V_D is D_1 diode forward voltage drop. Diode D_2 protection is limited to clamping the input to $V_{SS} - V_D$.

Summarizing the upper diode prevents the input signal from going one diode drop above the *IC* V_{DD}. The lower diode prevents the input signals from going more negative than a diode drop below ground.

6.2.9 Diode Selection

The most important parameters of a diode are listed in Table 6.1. They would be advertised by the diode manufacturer as being at one temperature, typically 25°C or valid at a temperature range, for example: 0°C to 70°C.

Upon selecting a diode for an application, none of the specified parameters should ever be exceeded under any conditions. Doing so may not necessarily make the device fail, but it can certainly reduce its useful life. Table 6.1 only lists some of the key parameters; manufacturers also publish curves for some of the parameters to give a better idea to the diode circuit application designer what the limits of the parameters are for slightly different conditions than those published on the table.

Table 6.1 Some diode key parameters

Parameter	Test Condition	Symbol	Min.	Typ.	Max.	Units
Forward voltage	At $I_F = 10\,\text{mA}$	V_F		0.6	1	V
Breakdown voltage	At reverse current $I_R = 100\,\mu\text{A}$	V_R	100			V
Peak reverse current	At $V_R = 75\,\text{V}$	I_R			5	μA
Diode capacitance	$V_R = 0$ Freq = 1 MHz	C_D			4	pF
Reverse recovery time	$I_F = 10\,\text{mA}$ to $I_R = 1\,\text{mA}$ $V_R = 6\,\text{V}$, $R_{LOAD} = 100\,\Omega$	t_{RR}			4	ns
Power dissipation		P_D			0.5	W

Example 6.5 Let us assume that one wants to design a half-wave rectifier that has to operate under the following conditions: Sinusoidal input waveform: 120 V_{RMS}, frequency 60 Hz, and peak load current 1 A. Assume that the accuracy we want for the rectified output is 120 V ± 1%. Determine the *forward voltage, breakdown voltage, peak reverse voltage, reverse recovery time*, and *power dissipation* of a general-purpose diode that you need to select. Since the RMS value of the input waveform is 120 V, the peak voltage is $120 \times 1.41 = 169.2$ V peak. Forward voltage: since 1% of 169.2 V is approximately 1.7 V, any general-purpose Silicon diode that has a forward drop of 0.6–0.7 V will meet our requirements.

Since the sinusoidal input has a ± 169.2 V of peak value, we need to ensure that when our diode is reversed biased, it can tolerate without any stress 169.2 V as its reverse voltage. If we picked a diode with about a 15–20% margin, the reverse voltage rating would have to be 200 V. Let us assume that we want more margin than that to obtain excellent reliability of the diode, so we pick a diode with a 400-V repetitive breakdown voltage. This provides more than a generous 100% margin. A diode that handles a 2-A forward peak current will satisfy the requested conditions. Many general-purpose diodes handle more than 2 A, so this is not a hard find. Since the frequency of operation of the diode is 60 Hz, this means that the period of the 60 Hz signal is 16.67 ms. Within the 16.67 ms period, the diode has to be turned on once and turned off once, so the diode shall have timing margin to handle a signals changing every approximately 8 ms. It is easy to find general-purpose diodes for power supply applications that have switching recovery times in the order of *ns*. So speed wise, we can pick any diode that switches at the speed required.

Since the forward peak current shall not be over 1 A, $1\,\text{A} \times 1\,\text{V} = 1\,\text{W}$ power dissipation. Note that 1 V is the maximum forward voltage drop of the diode, so the diode will not dissipate more than 1 W at maximum current.

Summary:

Forward voltage drop $V_D = 0.7$ V to 0.8 V Typ; Max. $V_D \approx 1.2$ V.

Repetitive breakdown voltage $V_R = 400$ V.

Reverse recovery time t_{RR} = anything considerably faster than 8 ms, any value in the *ns* range is trivial to obtain.

Power dissipation $P_D = 2$ W, this allows a nice 100% margin so that the diode not only dissipates less power than it has to but also may not need to be equipped with a heat-sink to remove the heat energy from the diode.

6.3 BIPOLAR JUNCTION TRANSISTORS (BJT)

Transistors and diodes are devices generally fabricated with silicon (Si). Silicon is one of the most abundant elements on the planet. After considerable processing silicon can be obtained from sand. In the earlier years of transistor fabrication, germanium was also used. However, the use of silicon proved to be superior and easier to manufacture transistors with. Silicon is the predominant material used for the fabrication of electronic devices and integrated circuits today.

6.3.1 Basic Concepts on Intrinsic, *n*-type and *p*-type Silicon Materials

We know that silicon is an element of the periodic table of elements. One of its characteristics is that it has an atomic number of 14; that is, it has 14 electrons that spin around the silicon atom nucleus. The electrons are distributed around the nucleus in different energy levels; these levels used to be referred to as electron shells. Elements can have up to seven energy levels. Such levels are 1 through 7, where 1 is the level closest to the nucleus and energy level 7 is the energy level farthest away from the nucleus. The silicon atom has 2 electrons in energy level 1, 8 electrons in energy level 2, and 4 electrons in energy level 3. Energy levels 1 and 2 are complete, but energy level 3 is complete when it contains 8 electrons. Level 3 is silicon's highest energy level and is also referred to as the *valence shell*. Figure 6.15 depicts the seven electron energy levels 1 through 7, each energy level has a maximum number of electrons that can exist in it. Although there are seven levels, only four of those levels are used by the known periodic table elements.

Element silicon with atomic number 14 has the following electron configuration notation:

$$\text{Silicon Electron Configuration}: 1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^2$$

Silicon atoms have a tendency of uniting with other silicon atoms in order to complete their valence shell with 4 more atoms, so that their *valence shell* becomes complete with 8 electrons. Silicon atoms stick together and each atom has four electrons on its own *valence shell* and four more electrons are shared from neighboring silicon atoms. The sharing of valence electrons between two

(a)

Energy Level	n	Letter
First	1	K
Second	2	L
Third	3	M
Fourth	4	N
Fifth	5	O
Sixth	6	P
Seventh	7	Q

(b)

Sublevel	Electron Possible	Orbitals Possible
s	2	1
p	6	3
d	10	5
f	14	6

Figure 6.15 Electron energy levels.

or more atoms produces a *covalent bond* between such atoms. *Covalent bonds* hold the atoms together, forming a structure denominated a *crystal*. Because every atom in the crystal structure is bonded to four other atoms, the electrons are not free to move within the crystal. Intrinsic silicon refers in simple terms to pure silicon with no other elements in its crystalline structure. Because of the *covalent bonds* just described, silicon and germanium are not good conductors of electricity. Figure 6.16 depicts a small portion of the periodic table of elements. Silicon and germanium are elements that have four electrons in their valence shell. Also present are what we will refer to as dopants: boron (B) and gallium (Ga) are elements that have three electrons in the valence shells. Phosphor (P) and arsenic (As) are elements that have five electrons in their valence shell. When intrinsic silicon is doped with certain amounts of boron or gallium the doped new structure has a deficit of electrons. It is said that the doped silicon is *p-type* material; the absence of an electron is referred to as a

	Group III	Group IV	Group V	
…	Boron (B)	Carbon (C)		…
…	Aluminum (Al)	Silicon (Si)	Phosphorus (P)	…
…	Gallium (Ga)	Germanium (Ge)	Arsenic (As)	…
…				…

Figure 6.16 Small section of the periodic table of elements.

hole, a hole has a positive charge and its magnitude is equal to the magnitude of the charge of an electron. When intrinsic silicon is doped with certain amounts of phosphor or arsenic, the doped structure has excess of electrons. This silicon structure doped with phosphor or arsenic is referred to as *n-type* material. Again pure silicon is called *intrinsic* silicon. When impurities are added to it, it becomes *extrinsic* silicon. When the impurities added to intrinsic silicon are elements from Group III, like boron, these are called *acceptors*, because they can accept extra electrons into the crystal. When the impurities added to the intrinsic silicon are elements from Group V, like phosphor, these impurities are called *donors*, because they can easily loose or donate an extra electron to the crystalline structure.

There is a vast amount of literature that covers semiconductors physics. In this introductory section we have not even scratched the surface of it. The main intent of this section is to provide the reader with the basic concepts behind intrinsic, *n*-type and *p*-type doped silicon. For further details on semiconductors refer to the Further Reading section at the end of this chapter.

6.3.2 The BJT as a Circuit Element

We will study the BJT almost entirely from a circuit behavior point of view. We will be concerned with the voltages across its terminals and its currents, how they change and how they need to be set in order for the transistor to operate as either an amplifier or a linear device, as a switch or a nonlinear device. There are two types of bipolar transistors, the NPN and the PNP. Figure 6.17 shows a simplified diagram of the structure of NPN and PNP transistors.

Bipolar transistors have three terminals, the collector, the base, and the emitter. For an NPN transistor whose schematic symbol is depicted in Figure 6.18, three fundamental voltages and currents are defined: v_{CE}, v_{BE}, and v_{CB} and i_C, i_B, and i_E. Voltage v_{CE} is the collector to emitter voltage drop; this voltage is positive for NPN transistors. v_{BE} is the base to emitter junction voltage, and v_{CB} is the collector to base junction voltage. From KVL it is easy to see that

$$v_{CE} = v_{BE} + v_{CB} \tag{6.8}$$

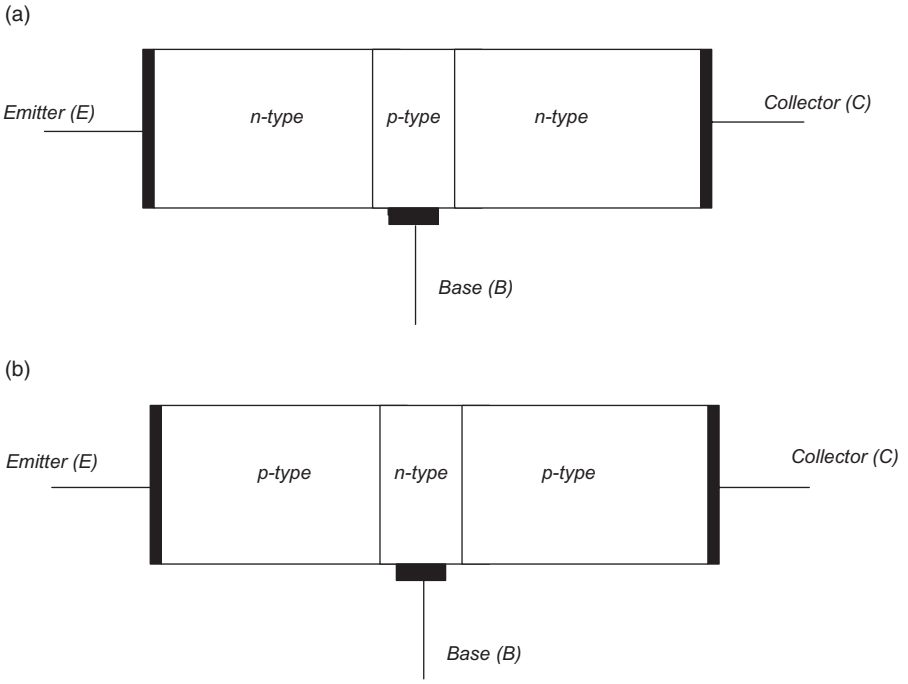

Figure 6.17 Simplified bipolar transistor structures: (a) NPN; (b) PNP.

and from KCL,

$$i_E = i_C + i_B \tag{6.9}$$

where in Equations (6.8) and (6.9) v_{CE} is the collector to emitter voltage drop, v_{BE} is the base to emitter junction voltage drop, v_{CB} is the collector to base junction voltage drop, i_E is the emitter current, i_C is the collector current, and i_B is the base current, respectively.

Note that the differences between voltages and currents in NPN and PNP transistors are that when a voltage is positive in the NPN-type device, the same voltage is negative in its counter part, the PNP device. Similarly, if a current is positive in the NPN, the same current is negative in the PNP.

6.3.3 Bipolar Transistor *I-V* Characteristics

For simplicity we will mostly concentrate describing the NPN transistor first. Later on some material on the PNP will be covered. A family of curves

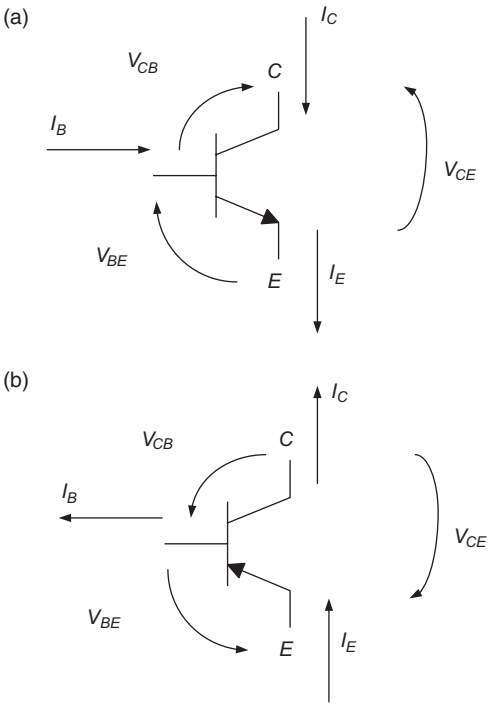

Figure 6.18 (a) Schematics symbols of an NPN transistor, its voltages, and currents; (b) symbol, voltages, and currents for a PNP transistor.

referred to as the current–voltage (*I-V*) characterizes the transistor. Figure 6.19 depicts the *I-V* characteristics of an NPN bipolar transistor.

The transistor *I-V* curves depict collector current versus collector-emitter voltage drop in the horizontal axis. The base current is used as a parameter for collector current versus collector-emitter voltage pairs. If we did not plot the *I-V* curves using the base current as a parameter, we would be forced to use three-dimensional plots, which are much harder to draw and visualize on a flat piece of paper. For the curves depicted in Figure 6.19, $i_{B6} > i_{B5} > \ldots > i_{B1}$.

For example, referring again to Figure 6.19, note that for a base current of 1 mA the collector current starts from zero i_C and zero v_{CE}. i_C ramps up somewhat linearly and then it virtually flattens out with a slight positive slope. We will later see that due to the Early effect, a slight positive slope is observed in the collector current curves. For a base current of 2 mA, i_C versus v_{CE} is plotted somewhat above the curve for 1 mA of base current. The larger is the base current, the higher will be the corresponding $i_C = f(v_{CE})$ curve.

Three key areas of operation are identified in the *I-V* curves of Figure 6.19. The region adjacent to the collector current axis, the vertical axis, is the

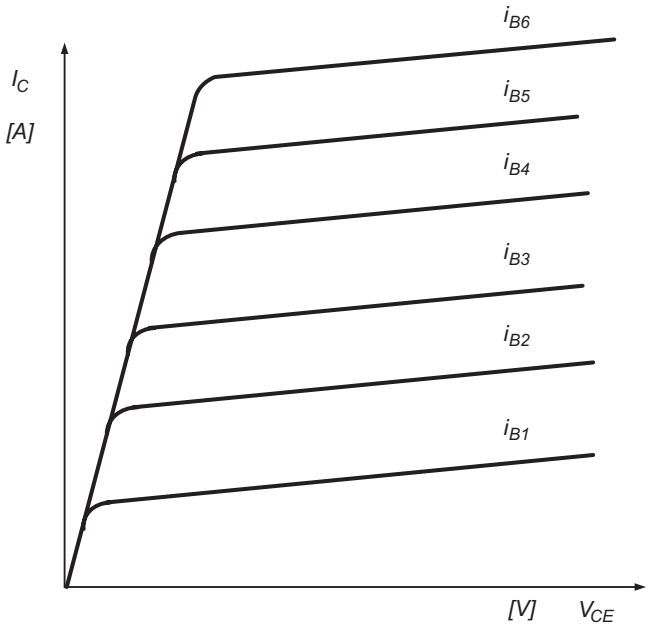

Figure 6.19 *I-V* characteristics curves of an *NPN* transistor.

saturation region; the region adjacent to the horizontal axis or the collector-emitter voltage is the cutoff region. Everything else is basically the so-called active region of the device.

An *NPN* transistor acts as a device that allows collector current, which is almost equal in magnitude to the emitter current; go through the NPN structure. A thin layer of *P* material constitutes the base of the transistor. The voltage that injects current into the base terminal has control over the amount of collector current that goes through the collector to emitter terminals of the device. We have seen that from Equation (6.9), the emitter current is the sum of collector and base current. Practically speaking, the base current is quite small, about two orders of magnitude smaller than the collector and emitter currents. So the approximation:

$$\mathrm{i_E} \cong \mathrm{i_C} \tag{6.10}$$

is valid for many applications. The reader, however, is cautioned not to use Equation (6.10) liberally. It is a good opportunity to introduce the *DC* current gain factor of the transistor, referred to as its β (Greek letter beta). β relates collector and base currents as follows:

$$\mathrm{i_C} = \beta \mathrm{i_B}. \tag{6.11}$$

β is generally a number around 100 (i.e., 20–50) for power transistors, but it is usually 100–500 for signal (small) transistors. Note that β has no units, and it is the transistor current gain factor. β is one of the transistor most important figures of merit. β is also referred to as the static or DC current gain of the transistor, and it is sometimes denoted as h_{fe}; the "h" stands for the transistor hybrid parameters model, which is beyond the scope of our book. The suffix "$_{fe}$" stands for forward and common emitter configuration.

We will explain later in this chapter what a common emitter configuration is.

Using Equation (6.11) in Equation (6.9) we obtain that

$$\mathrm{i_E} = \mathrm{i_C} + \frac{i_C}{\beta}. \tag{6.12}$$

Doing some algebra on Equation (6.12) we arrive at

$$\mathrm{i_C} = \frac{\beta}{\beta+1} \cdot \mathrm{i_E} \tag{6.13}$$

where the term $\beta/(\beta+1)$ is defined as the transistor's *alpha* (α); note that α always is a number slightly smaller than unity. α also is a dimensionless bipolar transistor parameter.

$$\alpha = \frac{\beta}{\beta+1}. \tag{6.14}$$

Example 6.6 Calculate the value of α for a transistor with a β of 200.

Solution: Using Equation (6.14) we obtain that $\alpha = 200/(200 + 1) = 0.995$.

Unfortunately β is not constant, and it varies for different collector currents and transistor temperature. Figure 6.20 depicts how β changes with collector current and with temperature. Notice the bell-shaped curves, the top curve is for a junction temperature of 125°C, the second one is for 25°C, and the bottom curve is for –55°C. Also note that generally β or h_{fe} grows for larger collector currents, but up to a point, beyond which it decays (Fig. 6.20).

It can be proven from semiconductor physics that the collector current equals

$$I_C = I_S \left(e^{\frac{v_{BE}}{v_T}} - 1 \right) \tag{6.15}$$

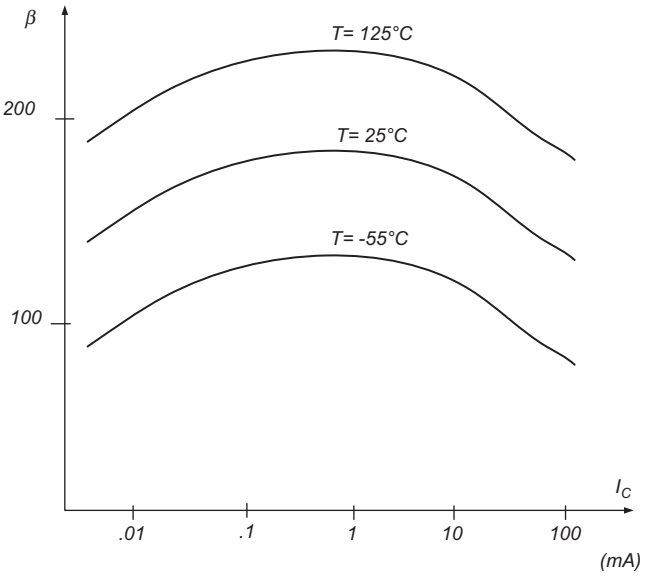

Figure 6.20 β variation with collector current and temperature.

where I_S is the reverse saturation current of the BJT base-emitter junction, v_{BE} is the base-emitter junction forward voltage drop, and v_T is the thermal voltage. v_{BE} typically is 0.6 V or 0.7 V for small signal silicon devices. v_T is the thermal voltage of the junction which at a room temperature of 300 K is approximately 26 mV. Based on the value of exponent $v_{BE}/v_T = 0.6/0.026 \cong 23$ and since $e^{23} >>> 1$ Equation (6.15) is simplified to

$$I_C = I_S e^{\frac{v_{BE}}{v_T}}. \tag{6.16}$$

The junction reverse saturation current is an extremely small current that flows through a reversed biased *pn* junction. For an ideal junction (either a diode junction or a transistor base-emitter junction), the reverse current is zero, for real junctions, it is a finite number typically in the range of 10^{-17} to 10^{-14} A. Using Equation (6.16), knowing the junction temperature, I_S the reverse saturation current of the BJT, and the DC collector current I_C, one can easily find the v_{BE} forward biased voltage drop.

Example 6.7 Assume that the collector current of an NPN transistor is 1 mA, $I_S = 10^{-15}$ A, and the junction temperature is 300 °K, determine the value of the forward biased base-emitter junction voltage drop.

Solution: Using Equation (6.16) we rewrite it as:

$$\frac{I_C}{I_S} = e^{\frac{v_{BE}}{v_T}}. \tag{6.17}$$

Taking the natural logarithm of both sides of the equation, and plugging the values given in the example we obtain that

$$ln\frac{I_C}{I_S} = \frac{v_{BE}}{v_T} \tag{6.18}$$

and rearranging terms,

$$v_{BE} = v_T ln\frac{I_C}{I_S}. \tag{6.19}$$

Plugging $v_T = 0.026$ V, $I_C = 0.001$ A, and $I_S = 10^{-15}$ A into Equation (6.19), it yields

$$v_{BE} = 0.718 \text{ V}. \tag{6.20}$$

6.3.4 Biasing Techniques of Bipolar Transistors

When the bipolar transistor operates as an amplifier, it needs to be biased in the active mode. In the absence of input signals to be amplified, the DC operating point of the transistor must be at point Q shown in Figure 6.21. Q is approximately halfway between the collector-emitter voltage spanned and halfway between the collector current spanned. We will elaborate more on this concept shortly.

For a bipolar transistor to be in the *active* mode or region, the base-emitter junction has to be forward biased, and the collector-base junction must be reverse biased. Referring to Figure 6.21, when both referred junctions are forward biased, the transistor is saturated; under saturation the collector to emitter voltage V_{CEsat} is minimal (typically about 0.2–0.3 V) since the transistor is acting as a closed (turned-on) switch. When both of the junctions are reverse biased, the transistor is said to be cutoff. No collector and no emitter currents flow through it. Finally, when the base-emitter junction is reverse biased and the collector-base junction is forward biased, the transistor is said to be in its reverse active mode of operation. This mode is not shown in Figure 6.21. The reverse active mode of operation is not a preferred mode to operate the transistor because its current gain parameter β is not as large as it is in the active mode. This is due to the fact that neither NPN nor PNP transistors are symmetrical. The emitter is more heavily doped than its collector. The reverse-active mode is seldom used.

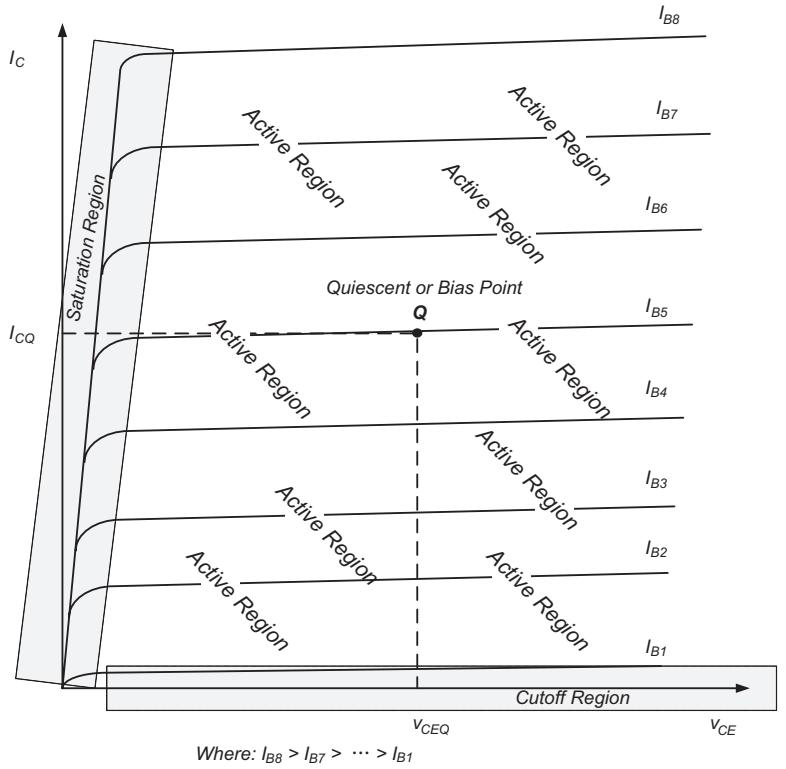

Figure 6.21 NPN transistor operating or quiescent point.

Table 6.2 Bipolar junction transistors mode of operation

Mode of Operation	Emitter-Base Junction	Collector-Base Junction
Active	Forward	Reverse
Reverse-Active[a]	Reverse	Forward
Saturation	Forward	Forward
Cutoff	Reverse	Reverse

[a] Not commonly used.

Table 6.2 shows the four regions of operation of a bipolar transistor. Table 6.2 applies to both NPN and PNP bipolar transistors.

When the BJT is used as a digital element or as a switch, it is mainly used in two modes, either *saturation* or *cutoff*. When the switch or the transistor is *ON*, it is saturated; when the transistor is *OFF*, the transistor is cutoff. When the transistor is used as a switch, it goes from *saturation* to *cutoff* and vice versa. Figure 6.22 depicts an NPN and a PNP BJTs in their active regions. Note

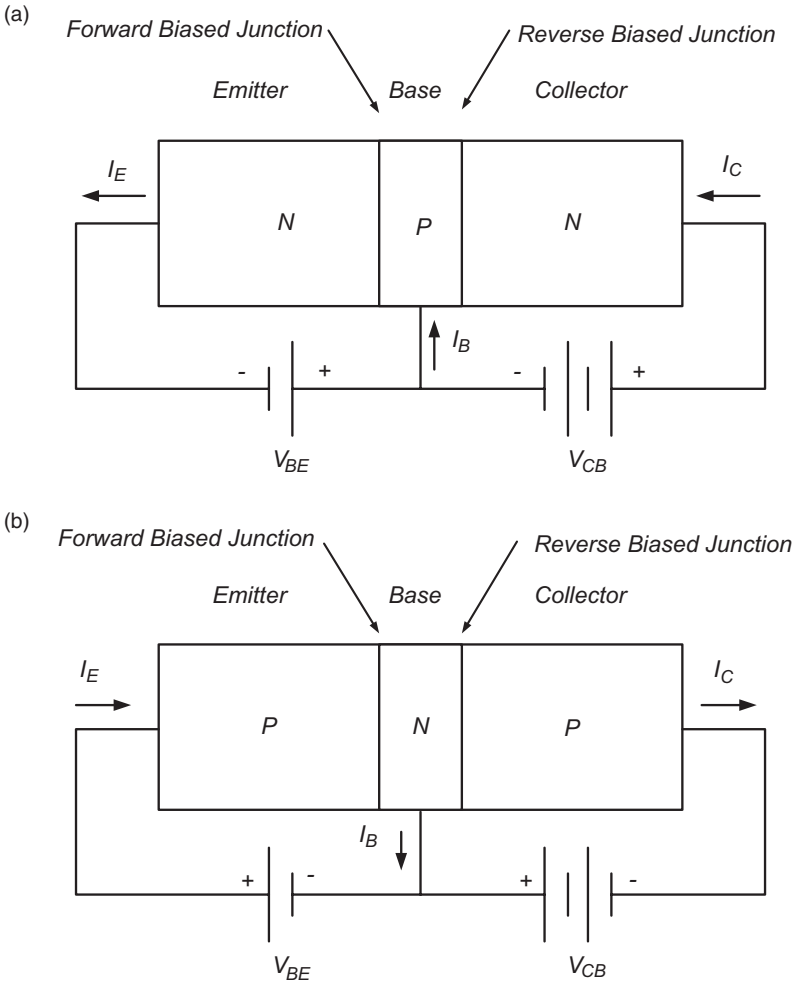

Figure 6.22 (a) NPN BJT in the active region; (b) PNP BJT in the active region.

that the emitter-base junction of both transistors is forward biased, while the collector-base junction of both transistors is reverse biased.

The circuits of Figure 6.22 are just conceptual drawings solely to show the polarities of the transistor junctions; both NPN and PNP transistors comply with the *active* mode described by Table 6.2.

Moreover, circuits of Figure 6.22 are not working biasing circuits.*

The careful observer should note that the NPN BJT of Figure 6.22a has its base-emitter junction forward biased while the collector-base junction is

* Current-limiting resistors should be added, as it will be seen in the following sections on biasing.

reverse biased. Also note that the NPN BJT collector current flows from the collector through the transistor *N* region, the base current flows into the base *P* region. Both collector and base currents get added at the base-emitter junction and out of the emitter terminal flows the emitter current. For the PNP case, note that the voltages are reversed in polarity, and the currents flow in the opposite direction to those of the NPN BJT.

6.3.5 Very Simple Biasing

Now let us look at the transistor circuit of Figure 6.23. We will consider the following values: $R_C = 50\ \Omega$, $R_B = 10\ \text{k}\Omega$, and $V_{CC} = 5$ V. Assume the transistor β is 100 and ignore I_S the reverse saturation current of the transistor.

The biasing circuit of Figure 6.23 is the simplest of all the ones that we will cover. Its purpose is to show the reader two methodologies to solve BJT-based biasing circuits. Our first Example 6.8 will show an approximated method. The second Example 6.9 will show a slightly more accurate method of solving the same problem.

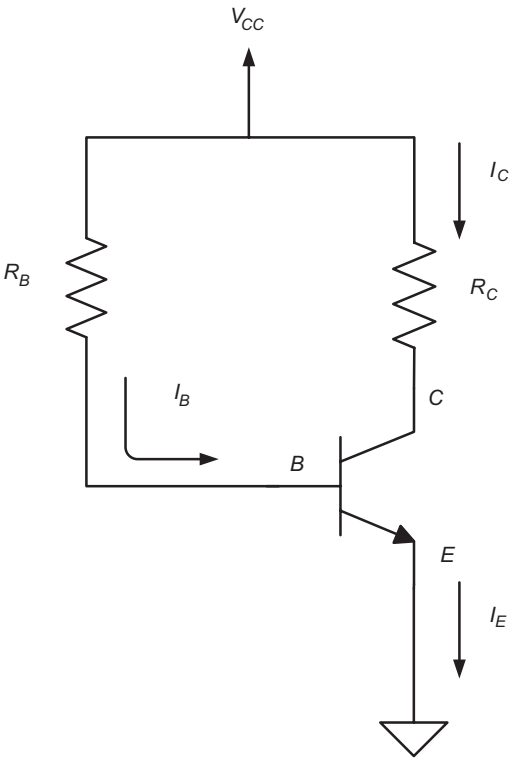

Figure 6.23 Very simple BJT biasing.

Example 6.8 Assume that $V_{CC} = 5$ V, $R_C = 50\ \Omega$, $R_B = 10$ KΩ, and $\beta = 100$. Let us assume that we want to find the collector-to-emitter voltage which also equals the collector-to-ground voltage, since the emitter is grounded. Using the circuit of Figure 6.23 we make an initial guess of the base-emitter junction forward voltage drop. Assuming that $v_{BE} = 0.6$ V (our initial guess), the base current is calculated as follows:

$$I_B = (V_{CC} - v_{BE}) / R_B. \tag{6.21}$$

Plugging the numerical values given into Equation (6.21) we obtain

$$I_B = (5 - 0.6) / 10{,}000 = 440\ \mu\text{A}. \tag{6.22}$$

Since $\beta = 100$, then

$$I_C = 100 \times 440\ \mu\text{A} = 44{,}000\ \mu\text{A} = 0.044\ \text{A}. \tag{6.23}$$

The collector-emitter voltage drop V_{CE} also equal to V_C, because the emitter is grounded, is calculated as follows:

$$V_C = V_{CC} - I_C \times R_C \tag{6.24}$$

Since $R_C = 50\ \Omega$ and $Ic = 0.044$ A from Equation (6.23), then

$$V_C = 5 - 0.044 \times 50 = 5 - 2.2 = 2.8\ \text{V}. \tag{6.25}$$

Example 6.9 Assume the same circuit of Figure 6.23 is used for this example. Assume the same parameters: $V_{CC} = 5$ V, $R_C = 50\ \Omega$, $R_B = 10$ kΩ, and $\beta = 100$. The reverse saturation current is $I_S = 10^{-14}$ A. Check to see if the results obtained for Equations (6.23) and (6.25) become a little more accurate by taking into account I_S.

Using the results given by Equations (6.23) and (6.25) as our initial guess, let us now verify how close to the initial guess of 0.6 V for v_{BE} is. Using Equation (6.19) for v_{BE} we have that

$$v_{BE} = v_T \ln \frac{I_C}{I_S} = 0.026 \ln\left(0.044\ 10^{14}\right) = 0.757\ \text{V}. \tag{6.26}$$

With the new v_{BE} value obtained with Equation (6.26), we reevaluate Equation (6.21) thus:

$$I_B = (V_{CC} - v_{BE}) / R_B = (5 - 0.757) / 10{,}000 = 424.30\ \mu\text{A}. \tag{6.27}$$

Since $\beta = 100$ and $I_C = \beta\, I_B$, then

$$I_C = 42{,}430\ \mu\text{A} = 0.04243\ \text{A}. \tag{6.28}$$

And since $V_C = V_{CC} - I_C R_C$, then

$$V_C = 5 - 0.04243 \times 50 = 5 - 2.1215 = 2.8785 \text{ V}. \tag{6.29}$$

One more time we recalculate the value of v_{BE} using Equation (6.19), thus:

$$v_{BE} = v_T \ln \frac{I_C}{I_S} = 0.026 \ln\left(0.04243\, 10^{14}\right) = 0.756 \text{ V}. \tag{6.30}$$

Since the recalculated value of v_{BE} Equation (6.30) is 155.6 mV off the assumed $v_{BE} = 0.6$ V. If we are satisfied with the result we do not iterate. Otherwise, we iterate the calculations again for a more accurate approximation. The solutions to our example are Equations (6.27) through (6.30).

6.3.6 Resistor Divider Biasing

The biasing scheme seen in the previous section is very sensitive to the variations of β. Since it is common for transistors of the same type and characteristics, to have a wide range of β, which could easily be from 100 to 200, the very simple biasing scheme of Figure 6.23 is not very practical or useful. We will investigate a circuit whose biasing is less sensitive to β variations. Referring to Figure 6.24a we see that the base-emitter voltage v_{BE} is established by the resistor divider formed by R_1 and R_2 if the base current is significantly smaller than the current that flows through the divider top resistor R_1. Thus:

$$v_{BE} = \frac{R_2}{R_1 + R_2} V_{CC}. \tag{6.31}$$

However, if the base current is comparable to the resistor divider current, a more accurate method of calculating the v_{BE} than Equation (6.31) must be used. What we do is apply Thévenin's Theorem to the left of the base node labeled with a "B," Figure 6.24a. The parallel of resistors R_1 and R_2 produces the Thévenin resistance:

$$R_{Thev} = \frac{R_1 R_2}{R_1 + R_2}. \tag{6.32}$$

The Thévenin voltage to the left node B, with the right-hand side of the circuit removed, is calculated with the following expression, and referring to Figure 6.24b,

$$V_{Thev} = \frac{R_2}{R_1 + R_2} V_{CC}. \tag{6.33}$$

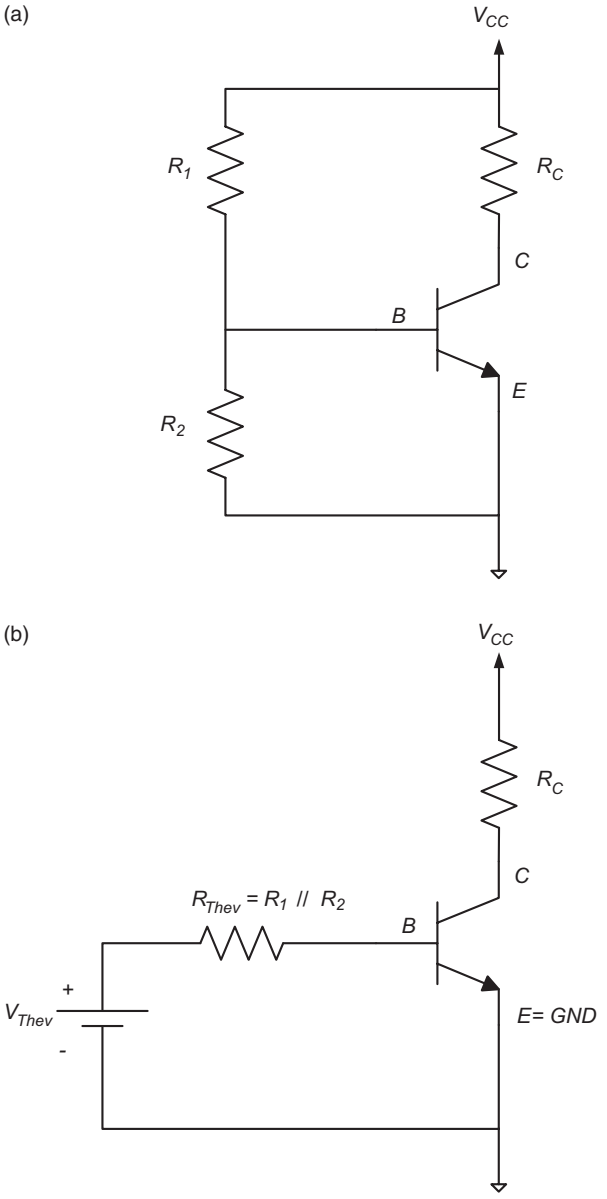

Figure 6.24 Resistor divider biasing method.

Using Equations (6.32) and (6.33) and referring again to Figure 6.24b, we write

$$V_{Thev} = I_B R_{Thev} + v_{BE}. \tag{6.34}$$

Using Equations (6.32) and (6.33) in Equation (6.34) and rearranging terms we obtain

$$v_{BE} = \frac{R_2}{R_1 + R_2} V_{CC} - I_B \frac{R_1 R_2}{R_1 + R_2}. \tag{6.35}$$

Recalling Equation (6.16) which is repeated below for the reader's convenience,

$$I_C = I_S \mathrm{e}^{\frac{v_{BE}}{v_T}}. \tag{6.36}$$

Finally, combining Equations (6.35) and (6.36) yields

$$I_C = I_S \exp\left(\frac{V_{Thev} - I_B R_{Thev}}{v_T}\right). \tag{6.37}$$

Rewriting Equation (6.37) to express the base current we obtain

$$I_B = \left(V_{Thev} - v_T \ln \frac{I_C}{I_S}\right).\left(\frac{1}{R_{Thev}}\right), \tag{6.38}$$

where in Equation (6.38) I_B is the base current, V_{Thev} is given by Equation (6.33), I_C is the collector current, I_S is the reverse saturation current, and R_{Thev} is given by Equation (6.32).

Example 6.10 Using the circuit of Figure 6.24, assume that $R_1 = 65$ kΩ, $R_2 = 15$ kΩ, $R_C = 2$ kΩ, $V_{CC} = 5$ V, $\beta = 100$, and $I_S = 10^{-17}$ A. Calculate I_B, I_C, v_{BE}. Make your first v_{BE} guess equal to 0.8 V, verify that your final v_{BE} is within 40 mV or less than the initial guess. You may have to iterate the process more than once to achieve the result wanted. Once the final value of v_{BE} is computed, find the collector-emitter voltage of the BJT and the voltage drop across resistor R_C.

We will go over this example a little faster since it is similar to the previous one.

We compute V_{Thev} in the usual way:

$$V_{Thev} = \frac{R_2}{R_1 + R_2} \mathrm{V_{CC}} = \frac{15}{15+65} 5 = 0.9375 \text{ V}. \tag{6.39}$$

$$R_{Thev} = \mathrm{R_1 // R_2} = 12{,}188\ \Omega. \tag{6.40}$$

Using the values found in Equations (6.39) and (6.40) and assuming $v_{BE} = 0.8$ V in Equation (6.34) we get

$$I_B = (V_{Thev} - v_{BE}) / R_{Thev} = (0.9375 - 0.8) / 12{,}188 = 11.282\ \mu\text{A}. \quad (6.41)$$

Then, since

$$I_C = \beta I_B = 100 \times 11.282\ \mu\text{A} = 1128.2\ \mu\text{A}. \quad (6.42)$$

And using the value of I_C from Equation (6.42) in Equation (6.19) copied right below for the reader's convenience,

$$v_{BE} = v_T \ln \frac{I_C}{I_S} = 0.026 \ln\left(1128.2\ 10^{-6}\ 10^{17}\right) = 0.8412\ \text{V}. \quad (6.43)$$

The result for v_{BE} is close, but not as close as the example requirements, so we recalculate Equations (6.41), (6.42), and (6.43) using $v_{BE} = 0.8412$ V. Thus,

$$I_B = (V_{Thev} - v_{BE}) / R_{Thev} = (0.9375 - 0.8412) / 12{,}188 = 7.9\ \mu\text{A}. \quad (6.44)$$

Then, since

$$I_C = \beta I_B = 100 \times 7.9\ \mu\text{A} = 790\ \mu\text{A}. \quad (6.45)$$

And using the value of I_C from Equation (6.45) in Equation (6.19) copied right below for the reader's convenience,

$$v_{BE} = v_T \ln \frac{I_C}{I_S} = 0.026 \ln\left(790\ 10^{-6}\ 10^{17}\right) = 0.832\ \text{V}. \quad (6.46)$$

Since 0.832 V is within 40 mV of the initial guess for $v_{BE} = 0.8$ V, we are done with the iterations, but not done with the example.

Since $I_C = 790\ \mu$A,

$$V_{R_C} = I_C R_C = 790\ 10^{-6} \times 2000 = 1.58\ \text{V}. \quad (6.47)$$

Since $V_{CC} = 5$ V, then

$$V_{CE} = V_{CC} - V_{R_C} = 5 - 1.58 = 3.42\ \text{V}. \quad (6.48)$$

The resistor divider method is better than the very simple biasing method; however, there is still dependence of the error obtained calculating the collector current I_C if the resistors vary only a small percentage. This can be numerically validated applying Equation (6.36) to a slight change of collector current. The reason should be clear that the exponential Equation (6.36) converts a small deviation of I_C into a large v_{BE} deviation. So this circuit is still of little practical value.

6.3.7 Emitter Degeneration Resistor Biasing

The circuit used for this method is shown in Figure 6.25. We can appreciate that there is just one difference between the circuits of Figures 6.25 and 6.24. The circuit of Figure 6.25 has an emitter resistor, but Figure 6.24 does not. This resistor will make the circuit more independent of β and v_{BE} if the other circuit parameter values are chosen correctly. It is also important to mention that the emitter of the BJT with the emitter degeneration resistor is *not* grounded, like it is in the case of the circuit of Figure 6.24a.

Let us refer to the circuit of Figure 6.25a, without ignoring the base current. Let us partition the circuit to the left of the base of the BJT. Let us find using Thévenin the equivalent of the circuit formed by resistors R_1 and R_2 powered by V_{CC}. Figure 6.25b shows that the voltage at the transistor base with respect to ground is

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC}. \tag{6.49}$$

Assuming that the current through the resistor divider is at least 10 times larger than the transistor base current (Fig. 6.25),

$$V_B = \frac{V_{CC}}{R_1 + R_2} >>> I_B. \tag{6.50}$$

We can also write for the base-emitter loop:

$$V_B = v_{BE} + I_E R_E. \tag{6.51}$$

Since $I_E = I_B + I_C$ and $I_C = \beta\, I_B$, then

$$I_E = (\beta + 1) I_B. \tag{6.52}$$

Plugging Equation (6.52) into Equation (6.51) leads to

$$V_B = v_{BE} + (\beta + 1) I_B R_E. \tag{6.53}$$

Thus: If $V_B >> v_{BE}$ and the voltage drop across R_E is at least a good fraction of v_{BE}, for example 200 mV, R_E "absorbs" the changes in V_B due to variations of v_{BE}. But there is a drawback; we will see later on that this reduces the gain when the circuit operates as an amplifier. So nothing comes for free.

However, at the same time, we have to be careful about keeping the transistor in its active region, that is, forward biased base-emitter junction and reverse biased collector-base junction. So the value of collector voltage with respect

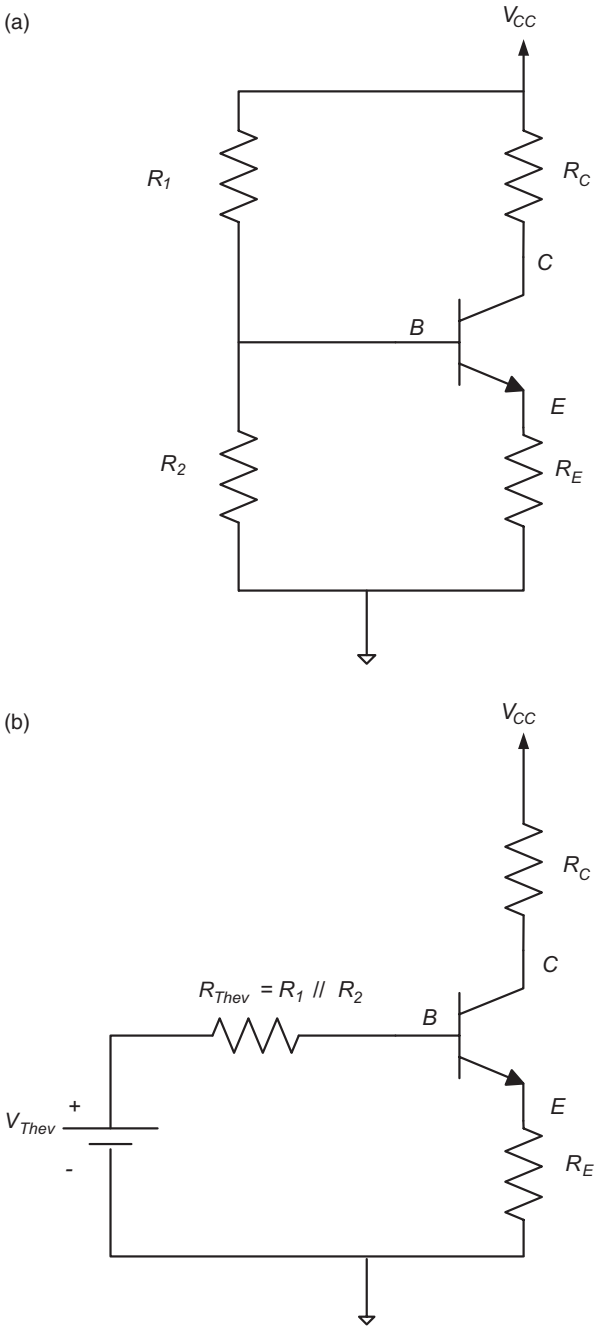

Figure 6.25 (a) Biasing with emitter degeneration resistor; (b) Thévenin equivalent.

to ground shall meet the following requirement for the transistor to be in its active region:

$$V_C = V_{CC} - I_C R_C > V_B. \tag{6.54}$$

Example 6.11 Using the circuit of Figure 6.25a determine the resistor values (R_C and R_E) such that the collector current is 2 mA. Assume that $V_{CC} = 10$ V, $\beta = 70$, and $I_S = 4 \times 10^{-17}$ A all at room temperature: (1) Find suitable values of R_1 and R_2 such that the circuit remains largely insensitive to v_{BE} and β *variations*. (2) Make sure that the transistor is biased and it is in the active region.

We can establish with this example the design criteria for this biasing circuit. In order to have insensitivity to variations of v_{BE} and β, we must design to meet Equations (6.50), (6.52), and (6.54).

First let us calculate v_{BE}:

$$v_{BE} = v_T \ln \frac{I_C}{I_S} = 0.026 \ln\left(2 \times 10^{-3} / 4 \times 10^{-17}\right) = 0.820 \text{ V}.$$

Let us then assume that v_{BE} is 0.8 V.

Since we want to achieve

$$\frac{V_{CC}}{R_1 + R_2} \gg I_B, \tag{6.55}$$

let us make

$$\frac{V_{CC}}{R_1 + R_2} = 10\, I_B. \tag{6.56}$$

Since $I_C = 2$ mA, then $I_B = I_C/\beta = 28.6$ μA and $V_{CC} = 10$ V, plugging these values into Equation (6.56), we obtain that

$$R_1 + R_2 = 34{,}965\ \Omega. \tag{6.57}$$

Since v_{BE} is 0.8 V and imposes a small voltage drop of 0.2 V across R_E, the voltage at the transistor base to ground is thus

$$V_B = \frac{V_{CC} R_2}{R_1 + R_2} = v_{BE} + I_E R_E = \frac{10 R_2}{34{,}965} = 1. \tag{6.58}$$

Thus,

$$R_2 = 3.497\ \text{k}\Omega \quad \text{and} \quad R_1 = 31.469\ \text{k}\Omega.$$

Additionally, using Equation (6.54) repeated below for the reader's convenience,

$$V_C = V_{CC} - I_C R_C > V_B. \tag{6.59}$$

We have to ensure that the transistor collector-base junction is reversed biased.

Let us assume that since $V_B = 1$ V, we want $V_C = V_B + 4$ V = 5 V to meet Equation (6.59).

Using Equation (6.59) where $V_C = 5$ V leads to

$$R_C = 2.5\ \text{k}\Omega.$$

For part (b), since the collector is at 5 V and the base is at 1 V, the collector-base junction is reversed biased. Since we assumed a 0.2 V across R_E, the base-emitter junction is forward biased and has a forward v_{BE} drop of 0.8 V. The BJT is in the active region.

Exercise: Use the circuit from the previous example, that is, $R_2 = 1$ kΩ, $R_1 = 9$ kΩ, $R_C = 3$ kΩ, $R_E = 200$ Ω, $V_{CC} = 10$ V. Replace the transistor with another transistor that has a $\beta = 200$ and $I_S = 10^{-17}$ A. Calculate the collector, emitter and base currents, the collector voltage, the emitter voltage, and v_{BE}.

What conclusions do you obtain when you compare these results with the previous example results?

6.3.8 Self-Biased Staged

The circuit of Figure 6.26 depicts a BJT with a self-biasing resistor R_B.

Note that the collector voltage is

$$V_C = V_{CC} - I_C R_C. \tag{6.60}$$

It is also important to notice that V_C always is larger than the base voltage V_B.

By further inspection of the circuit of Figure 6.26, we can also see that

$$V_C = I_B R_B + v_{BE}. \tag{6.61}$$

Merging the right-hand sides of Equations (6.60) and (6.61) and remembering that $I_C = \beta I_B$, we obtain

$$I_C = \frac{V_{CC} - v_{BE}}{R_C + \dfrac{R_B}{\beta}}. \tag{6.62}$$

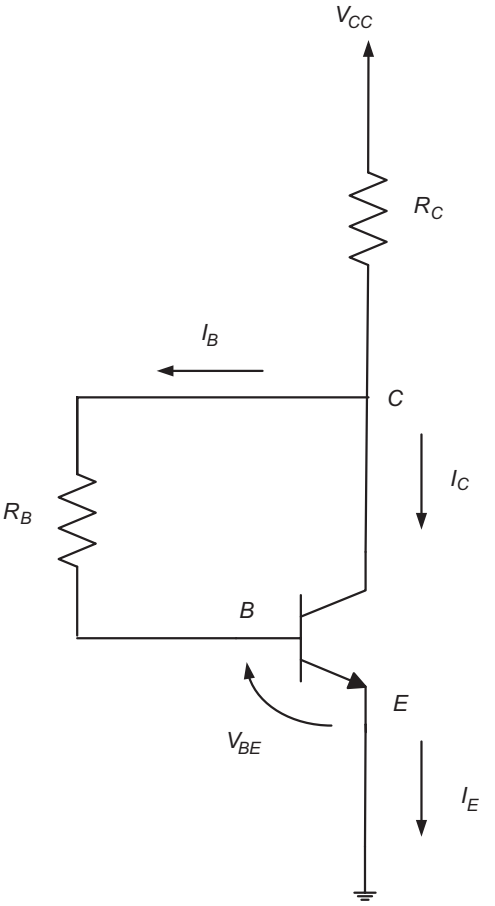

Figure 6.26 Self-biased bipolar transistor.

Example 6.12 Using the circuit of Figure 6.26, assume $V_{CC} = 5$ V, $R_B = 10$ kΩ, $R_C = 1$ kΩ, $\beta = 200$, $V_T = 0.026$ V, and $I_S = 10^{-16}$ A. Determine I_C and v_{BE}.

Using Equation (6.62) and initially assuming that $v_{BE} = 0.8$ V, we obtain

$$I_C = \frac{5 - 0.8}{1{,}000 + \dfrac{10{,}000}{200}} = 4 \text{ mA}. \tag{6.63}$$

Now, using the obtained I_C, let us recalculate the value of v_{BE} using

$$v_{BE} = V_T \ln \frac{I_C}{I_S} = 0.026 \ln \frac{4 \times 10^{-3}}{10^{-16}} = 0.814 \text{ V}. \tag{6.64}$$

Since $v_{BE} = 0.814$ V and the originally guessed value was 0.8 V, we decide not to recalculate the collector current I_C because there is only a 14 mV difference between the initial guess for v_{BE} (0.8 V) and the recalculated v_{BE} (0.814 V).

6.3.9 Biasing Techniques of PNP Bipolar Transistors

Let us take a look at the NPN and PNP transistors voltage and currents. Refer to Figure 6.18a,b, which we repeat here in Figure 6.27 for the reader's convenience.

The NPN transistor, part (a) requires positive v_{BE} for a forward biased BE-junction and a positive v_{CB} for a reversed biased CB-junction. Currents I_B, I_C, and I_E are positive and flow in the direction shown in Figure 6.27a. On the other hand, PNP transistors require a negative v_{BE} for a forward biased BE-junction and a negative v_{CB} for a reversed biased CB-junction. Currents I_B, I_C, and I_E are negative and flow in the opposite direction as shown in Figure 6.27b.

Taking into account the above considerations, biasing a PNP transistor is not much different from biasing an NPN. The biasing techniques studied for NPNs are valid for PNPs. Due to space reasons, we will only mention the circuit of biasing PNP with emitter degeneration resistor. Figure 6.28 shows such circuit mainly for the purpose of showing voltages and currents. Conceptually, all the concepts that are applicable to NPN transistors biasing also apply to PNPs.

Note that the current flows shown in Figure 6.28 are the actual current directions. Remember that on a PNP transistor all the voltages that were positive for an NPN are negative for a PNP. Similarly, the same concept applies to

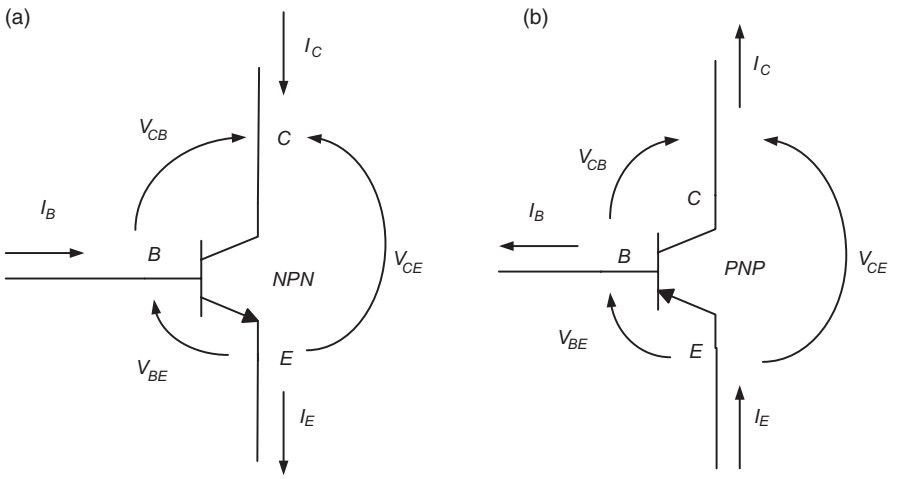

Figure 6.27 Voltages and currents: (a) NPN transistors; (b) PNP transistors.

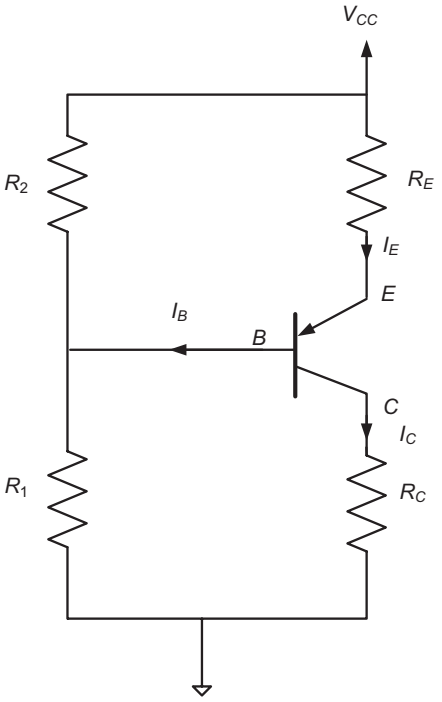

Figure 6.28 PNP transistor biasing with emitter degeneration resistor.

the currents; currents that are positive for the NPN transistors are negative or flow in the opposite direction on the PNP transistors. Carefully compare Figures 6.25a for an NPN and Figure 6.28 for a PNP.

6.3.10 Small Signal Model and Single-Stage Bipolar Amplifier Configurations

In this section we will study the three basic amplifier topologies, the common-emitter, common base, and common collector. In doing so we will use a simple low-to-medium frequency transistor small signal model, called by some authors as the hybrid-π model. Large signal analysis, or amplifier analysis with signals that are comparable in magnitude to the transistor biasing voltages, and multistage amplifiers are beyond the scope of this book.

One of the simplest bipolar transistor models is the one shown in Figure 6.29 even though the model is simple; it is very useful for the understanding of many transistor-based circuits.

The basic model has an input resistance of r_π, between the base and the emitter terminals. The output is modeled with a voltage-controlled current source $g_m V_\pi$, where g_m is the trans-conductance of the transistor and its value

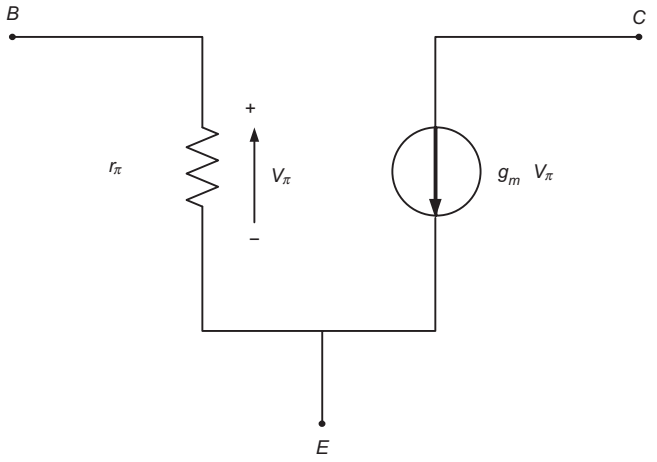

Figure 6.29 Bipolar transistor small signal model.

depends on the bias collector current and the transistor thermal voltage v_T, which is about 26 mV at room temperature of 300 K. Thus,

$$g_m = \frac{I_C}{V_T}. \tag{6.65}$$

So for example, for a 10-mA collector DC current, the transistor transconductance equals

$$g_m = \frac{I_C}{V_T} = \frac{10\text{ mA}}{26\text{ mV}} = 0.385\ \Omega^{-1} = 0.385\text{ S}. \tag{6.66}$$

The voltage V_π, refer one more time to Figure 6.29, is the voltage drop across the input resistance r_π. The input resistance r_π is given by the ratio of β and g_m, that is,

$$r_\pi = \frac{\beta}{g_m}. \tag{6.67}$$

The labels of the model terminals are: B, C, and E, where B stands for base, C for collector, and E for emitter. Finally, it is important to understand that the small signal model is the same whether the transistor is a PNP or an NPN. Table 6.3 summarizes the three key parameters of the BJT small signal model. The output resistance of the model primarily takes into account the fact that the I_C-V_{CE} characteristic curves do not have a zero slope beyond saturation. The characteristic curves of real BJTs have a slightly positive slope even beyond the collector current saturation level. Initially, it is meaningful to

Table 6.3 BJT small signal model: key parameters

Parameter	Parameter Name	Brief Description (only if needed)	Calculation	Units
g_m	Trans-conductance		$g_m = I_C/V_T$	(Siemens)
r_π	Transistor input resistance	Base-to-emitter input resistance	$r_\pi = \beta/g_m$ also: $g_m\, r_\pi = \beta$	(Ω)
r_o	Transistor output resistance	Finite output resistance due to the Early Voltage V_A	$r_o = V_A/I_C$ When the Early voltage is neglected: $r_o \to \infty$	(Ω)

ignore the Early voltage effect in the output resistance r_o, and an infinite r_o may be assumed in parallel with the dependent current source $g_m\, v_\pi$, not shown in Figure 6.26. When greater precision is desired, inclusion of the Early effect finite and non-zero output resistance in parallel with the current source of Figure 6.29 is required.

Small signal models are used to understand the small signal or the AC behavior of the transistor, typically under sinusoidal excitations of small magnitudes within a range of frequencies of interest. How small is a small signal? There are no hard rules, but we can state that a small signal has an amplitude in the order of one-tenth or less of the power supply rail. For example if $V_{CC} = 10$ V, 1-V signals or less are considered small. The purpose of biasing a transistor is to establish a quiescent (Q) or DC operating point. When we analyze an amplifier, under small signal operation, the input signals are applied on top of the DC voltages and currents that bias the transistor. For simplicity and without loss of generality, let us assume that a single sinusoidal signal of one frequency is applied to the input of the amplifier. By the superposition theorem, the signal moves the DC operating point of the amplifier DC voltage and current. Correspondingly, the DC output voltage and current are displaced by some amount that is proportional to the input signal times the gain factor of such amplifier. Let us elaborate more on this in the next section.

6.3.11 Common Emitter (C_E) Configuration

This configuration is the most commonly used stage when designing transistorized amplifiers. The emitter is typically grounded for AC or DC currents. In our example in Figure 6.30, the emitter has an emitter capacitor C_E, whose value is chosen to virtually be a short circuit at the lowest frequencies to be handled by the amplifier. Thus, the emitter is not grounded for DC components because of R_E; however, the emitter is grounded for all *AC* components within

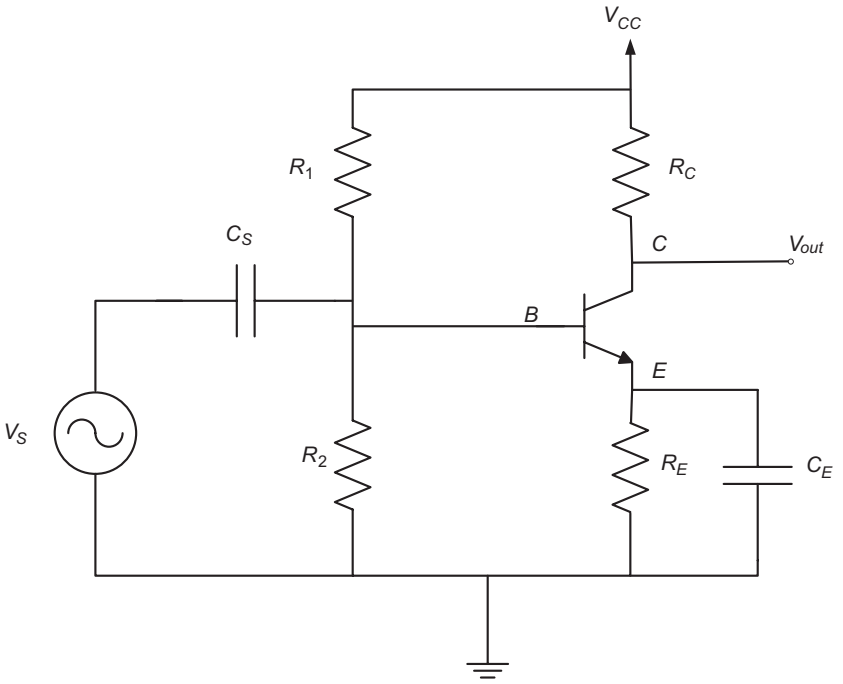

Figure 6.30 Common emitter configuration stage.

the frequency range of interest.* The input signal V_S to be amplified is applied at the base terminal; the amplified output is obtained at the collector V_{out}. Capacitor C_S value is chosen so that the capacitor is a virtual short circuit at the lowest frequency of interest. Figure 6.30 depicts a C_E configuration.

The sinusoidal signal generator is the input signal; the amplified output is obtained at V_{out}. Capacitor C_S AC couples the signal generator into the base of the amplifier, while at the same time the capacitor prevents the DC biasing from being disturbed. Capacitor C_E is a virtual short circuit to AC currents. Thus, the emitter degeneration resistor R_E does not reduce the AC gain of the amplifier. At the same time, R_E provides DC biasing independence from the transistor's β and v_{BE}. Figure 6.31 depicts the AC small signal model of the C_E configuration. The BJT's small signal model has replaced the bipolar transistor in Figure 6.31. The V_{CC} power supply is a short circuit to AC frequencies, thus the collector resistor upper terminal of the model is grounded. Note that capacitor C_S does not appear in the circuit of Figure 6.31 because it behaves as a short circuit to AC frequencies. More interestingly, capacitor C_E and resistor R_E do not show up on the small signal model either, because C_E acts as a short circuit across resistor R_E.

* Note: If a capacitor is a virtual short circuit to some low-frequency signal, it will be an even better short circuit for signals of higher frequency.

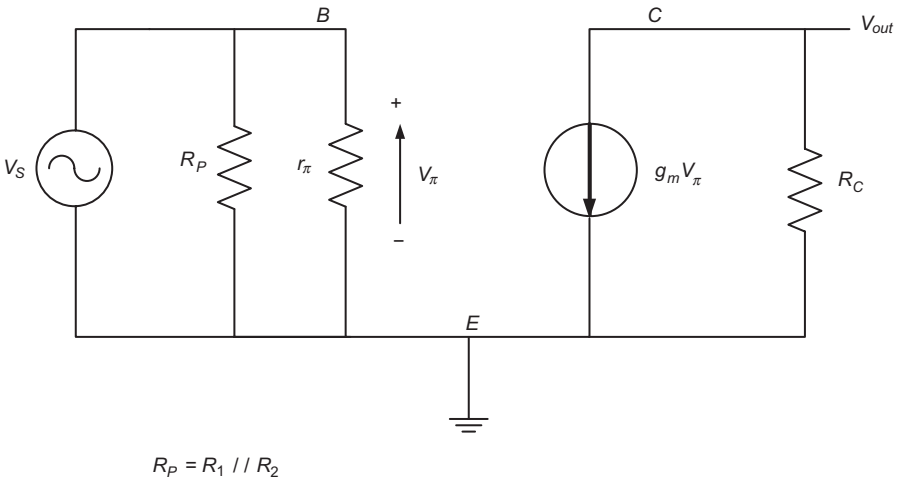

Figure 6.31 Common emitter stage with BJT's small signal model.

Resistors R_1 and R_2 are in effect in parallel with each other and connected between the transistor base and ground because the V_{CC} source is a short to AC frequencies. Now we are ready to start inspecting the circuit of Figure 6.31 to calculate the amplifier gain, its input, and output resistances.

Referring to the small signal common emitter stage of Figure 6.31 we observe that

$$V_{out} = -g_m R_C v_\pi \tag{6.68}$$

Since

$$v_\pi = V_S \tag{6.69}$$

Thus,

$$G_{CE} = \frac{V_{out}}{V_S} = -g_m R_C, \tag{6.70}$$

where in Equation (6.70) G_{CE} is the common emitter stage voltage gain, V_{out} is the stage output or collector voltage, V_S is the input voltage or signal, g_m is the BJT's trans-conductance, and R_C is the collector resistor. Note that the voltage gain has a negative sign; this means that there is a 180° phase shift between the output and the input.

Let us briefly discuss the concepts of input resistance and output resistance of an amplifier. The input resistance of an amplifier is the resistance that a test voltage sees when there is no load at the output of the amplifier. Figure 6.32a depicts the test voltage and the test current applied at the amplifier input with an open-circuited output.

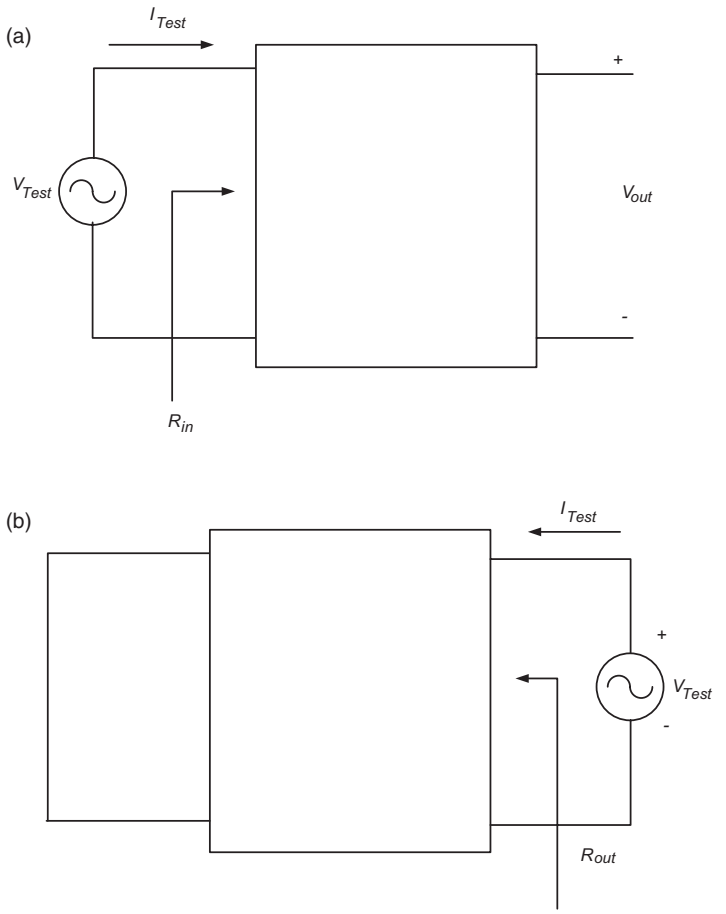

Figure 6.32 (a) Amplifier input resistance; (b) amplifier output resistance.

$$R_{in} = V_{Test} / I_{Test}. \tag{6.71}$$

Using the concept of input resistance from Equation (6.71), we apply it to our circuit of Figure 6.31 and get

$$R_{in} = \frac{r_\pi . R_P}{r_\pi + R_P}, \tag{6.72}$$

where in Equation (6.72) r_π is the BJT's input resistance and R_P is the parallel of resistors R_1 and R_2 in Figures 6.30 and 6.31.

The output resistance of the amplifier is obtained inhibiting sources at the input; since the input source is a voltage source, inhibiting it means to replace it with a short circuit. Then we apply a test voltage at the output of

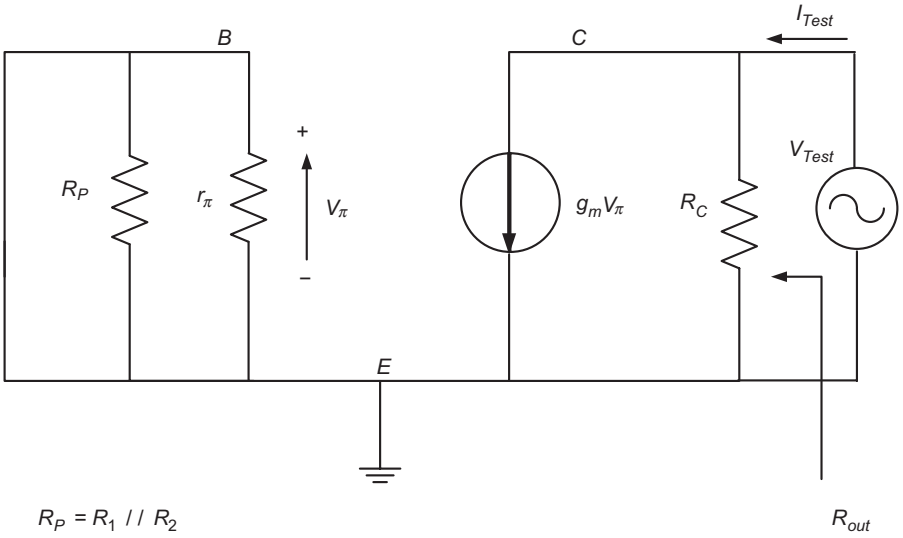

Figure 6.33 Common-emitter output resistance calculation.

the amplifier and the resistance that such test voltage sees is the output resistance of our amplifier. Refer to Figure 6.32b for the conceptualization of output resistance R_{out}.

Now referring one more time to the small signal equivalent circuit of the common emitter configuration of Figure 6.31 we proceed to compute the amplifier output resistance. We first replace the signal generator with a short circuit; we see the results of this in Figure 6.33. Shorting the input source also shorts voltage v_π, then it is easy to see that the current source of the circuit given by $g_m\, v_\pi$ becomes zero; that is to say, there is no current injected by this voltage-dependent current source. After applying the test voltage and current at the output of this stage, the output resistance seen is just R_C. Thus,

$$\frac{V_{Test}}{I_{Test}} = R_{out} = R_C . \tag{6.73}$$

Inclusion of the Early Effect in the Output Impedance Calculation

In Table 6.3 we presented without proof, that the finite output resistance of a transistor, when better accuracies are desired, is computed as follows:

$$r_o = V_A / I_C ,$$

where I_C is the collector bias current and V_A is the Early voltage, a transistor parameter. Equation (6.73) for output resistance of the common emitter amplifier changes to the following when one includes the Early voltage effect:

$$\frac{V_{Test}}{I_{Test}} = R_{out} = R_C \,//\, r_o = \frac{R_C r_o}{R_C + r_o}. \tag{6.74}$$

6.3.12 Common Emitter (C_E) Configuration with Emitter Degeneration

When a resistor is placed between the emitter and ground of the common emitter configuration, the amplifier gain is reduced. This is not necessarily harmful; on the contrary, it benefits the linearity of the amplifier, many times a desirable feature to pay for at the expense of a reduced gain. This common emitter degeneration is applied not only to DC signals but also to AC signals when resistor R_E bypassing capacitor C_E is removed; see Figure 6.31. The gain of the amplifier without common emitter degeneration resistance was addressed by Equation (6.70). Accounting the emitter degeneration resistance in the small signal model (C_E capacitor removed) can be derived from Figure 6.34 recalculating the gain of the amplifier after removing C_E. We just present the result of such gain, which is:

$$G_{CE \text{ with emitter degeneration resistor}} = -\frac{g_m R_C}{1 + g_m R_E} \tag{6.75}$$

which also equals to

$$G_{CE \text{ with emitter degeneration resistor}} = -\frac{R_C}{\frac{1}{g_m} + R_E} \tag{6.76}$$

Another important fact in a common emitter configuration with emitter degeneration is that the amplifier input impedance seen between the base and ground becomes

$$R_{in\ CE \text{ with emitter degeneration resistor}} = r_\pi + (\beta + 1) R_E. \tag{6.77}$$

Equation (6.77) is derived from the circuit presented in Figure 6.34.

The importance of Equation (6.77) is that the total input resistance of the amplifier with emitter-degeneration is that the input resistance can be very large because of the $(\beta + 1)$ factor. It also interesting to mention that from an output impedance point of view, the emitter degeneration resistor does not change the output impedance at all, assuming that the Early effect is neglected. Thus,

$$R_{out\ CE \text{ with emitter degeneration resistor}} = R_C.$$

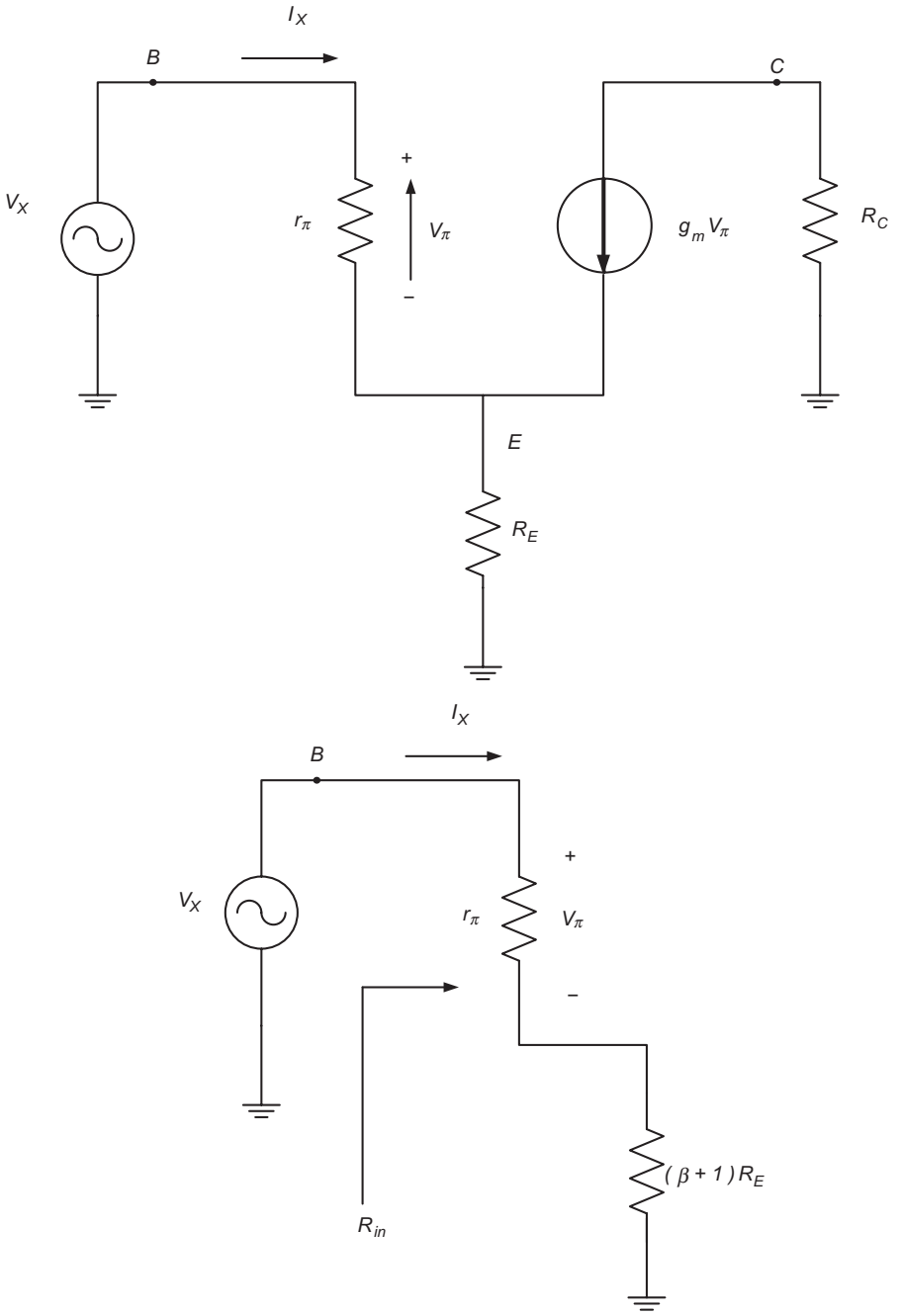

Figure 6.34 Common-emitter amplifier with emitter degeneration resistor.

Example 6.13 Given the circuit of Figure 6.30, assume the following component values: $R_1 = 20$ kΩ, $R_2 = 100$ kΩ, $R_C = 50$ Ω, and $R_E = 100$ Ω, the supply is $V_{CC} = 10$ V. (1) Calculate I_C, I_B, V_{CE},V_{RE}, and β. (2) Also calculate for the found value of β the BJT trans-conductance g_m and r_π of the hybrid-π small signal model. At all times ignore the BJT Early effect; that is, $r_o \to \infty$. Assume the reverse saturation current $I_S = 7.11 \times 10^{-15}$A at room temperature of 300 K and $V_{BE} = 0.763$ V.

Solution to Example 6.13

From Equation (6.16), repeated here for the reader's convenience, we find for $I_S = 7.11 \times 10^{-15}$ A, $v_{BE} = 0.763$ V, and $v_T = 0.026$ V that

$$I_C = I_S e^{\frac{v_{BE}}{v_T}} = 39.5\,\text{mA}. \tag{6.78}$$

Using the above given values in the circuit of Figure 6.30, and applying Thèvenin to the resistor divider on the left of the BJT base node, we obtain

$$R_{Thev} = \frac{R_1 R_2}{R_1 + R_2}; V_{Thev} = \frac{R_2}{R_1 + R_2} V_{CC}. \tag{6.79}$$

Equations (6.79) were obtained just as Equations (6.32) and (6.33) were obtained, using the *resistor divider method*.

For the Thevenized portion of the circuit we can write KVL equations, to find the base current:

$$I_B = (V_{Thev} - V_{BE} - V_E) / R_{Thev} \tag{6.80}$$

where $V_{Thev} = 8.33$ V and $R_{Thev} = 16{,}667$ Ω are calculated from Equations (6.79) using the given values of R_1, R_2, and V_{CC}. Voltage V_E is the voltage drop across resistor R_E. This voltage is approximately equal to $I_C R_E$; a more exact value is $I_E R_E$. *Since* $I_C \approx I_E$, the error in the approximation is small, because $I_C + I_B = I_E$, and the value of base current is quite small. Using the value of $I_C = 39.5$ mA, we get that

$$V_E \approx I_C R_E = 0.0395 \times 100 = 3.95\ \text{V}.$$

Plugging the value of $V_E = 3.95$ *V* into Equation (6.80) we obtain: $I_B = 217$ μA.

Since we calculated the collector current I_C and base current I_B, $\beta = I_C/I_B = 182$. Referring one more time to the circuit of Figure 6.30 we can see that the collector-emitter voltage:

$$V_{CE} = V_{CC} - I_C R_C - V_E.$$

Plugging the corresponding values, we obtain that

$$V_{CE} = 10 - (0.0395 \times 50) - 3.95 = 4.08 \text{ V}.$$

For part b of this example, since $g_m = I_C/V_T$ and $r_\pi = \beta/g_m$, we obtain that

$$g_m = 1.52 \text{ S and } r_\pi = 119\ \Omega.$$

The results for part (a) are regrouped and presented here:

$$I_C = 39.5 \text{ mA}$$
$$I_B = 217\ \mu\text{A}$$
$$V_{CE} = 4.08 \text{ V}$$
$$V_{RE} = 3.95 \text{ V and}$$
$$\beta = 182$$

and for part b):

$$g_\text{m} = 1.52 \text{ S}$$

and

$$r_\pi = 119\ \Omega.$$

6.3.13 Common-Base (CB) Configuration

The common-base configuration has a grounded base, the input signal is applied between the emitter and ground and the output of the amplifier is extracted between its collector and ground. Figure 6.35 walks us through the gain calculation of the CB topology. This topology is simplified since biasing is not fully shown. Note that input voltage V_{in} does not have any resistors in series to bias this stage.

Figure 6.35b allows us to see that the stage gain is

$$G_{CB} = V_{out} / V_{in} = g_m R_C. \tag{6.81}$$

It is very important to realize that the CB topology gain is equal to the absolute value of the CE topology gain. The CE gain has, unlike the CB gain, a negative sign; see Equation (6.70).

Next we will inspect Figure 6.36a,b to do a basic calculation of the input resistance of the CB stage. Note that using KCL at node E

$$I_X = -\left(g_m V_\pi + \frac{1}{r_\pi} V_\pi \right) = -V_\pi \left(g_m + \frac{1}{r_\pi} \right). \tag{6.82}$$

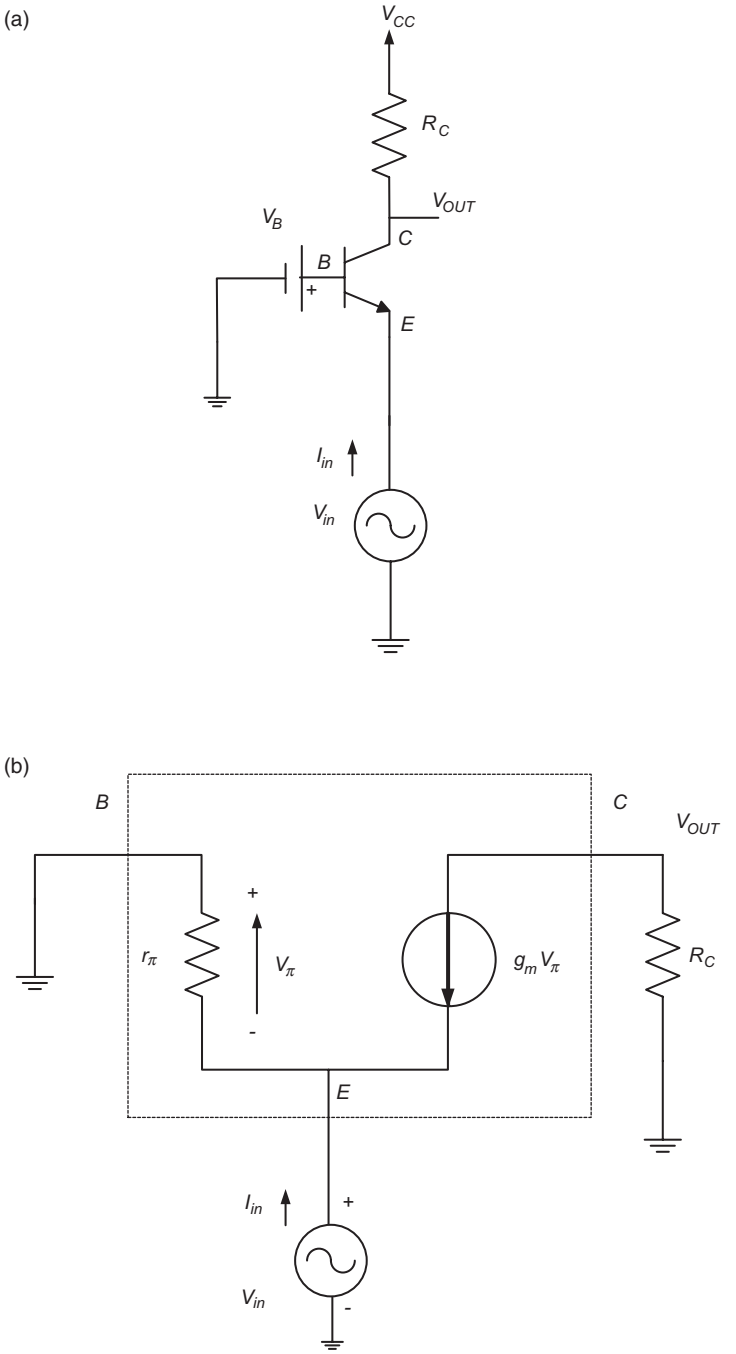

Figure 6.35 (a) CB stage used to calculate the gain; (b) CB stage with the hybrid-π small signal model.

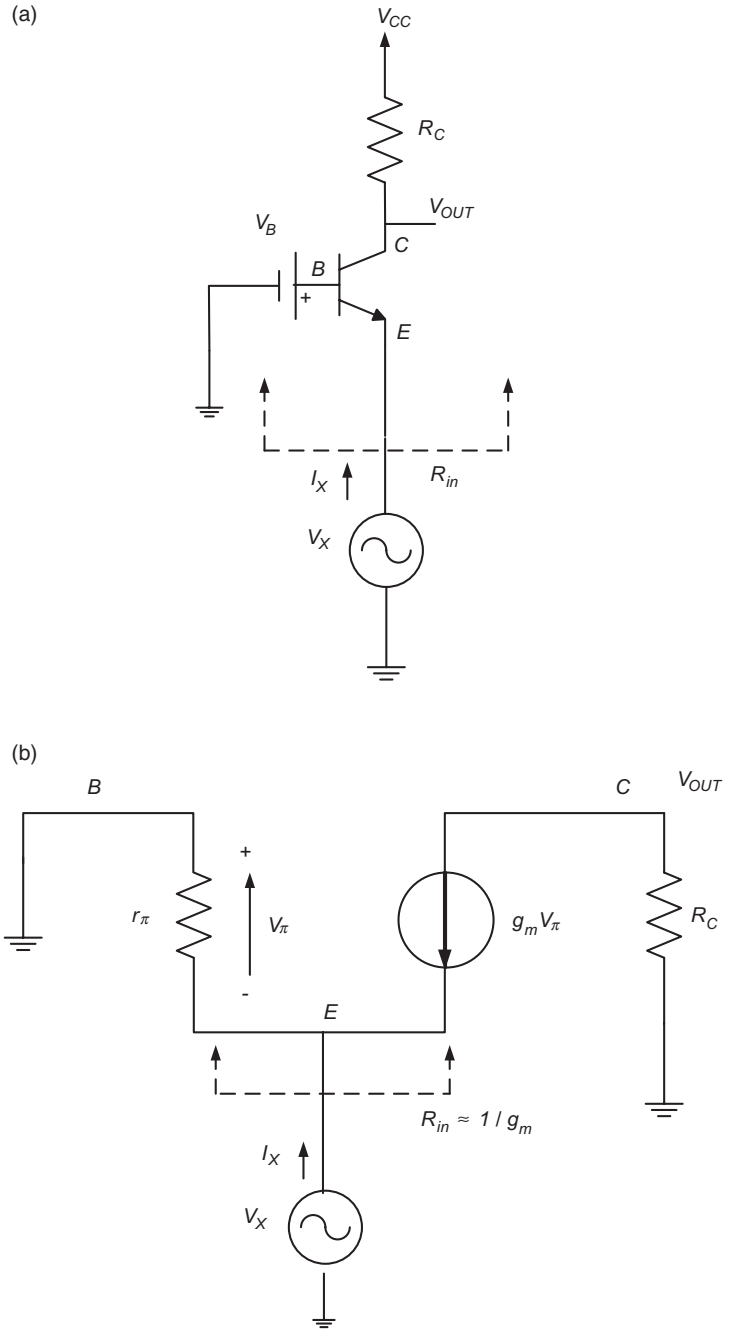

Figure 6.36 (a) Common base stage R_{in} calculation; (b) common base stage with small signal model.

And most importantly and again from Figure 6.36b since:

$$-V_\pi = V_{in}. \tag{6.83}$$

Plugging Equation (6.83) into Equation (6.82) yields

$$R_{in} = V_X / I_X = 1 / \left(g_m + \frac{1}{r_\pi} \right). \tag{6.84}$$

If r_π is large, then $1/r_\pi$ is small and we can approximate Equation (6.84) with

$$R_{in} \approx 1 / g_m. \tag{6.85}$$

Note that it is not unusual for r_π to be about 1 kΩ and for g_m about 50 mA/26 mV ≈ 1.923 S for signal transistors, thus Equation (6.85) is quite accurate. Both Equations (6.83) and (6.84) assume that the Early effect is negligible (i.e., $r_o \to \infty$).

Let us investigate the output resistance of the CB topology. To do that we provide an AC ground to the emitter input, as seen in Figure 6.37a. Then we replace the BJT with its hybrid-π small signal model, apply a test output voltage, which generates a test input current. As usual, R_{out} is given by the ratio of the test voltage and input. It is clear to see from Figure 6.37b that

$$R_{out} = R_C, \tag{6.86}$$

where Equation (6.86) ignores the Early effect, since it assumes that the transistor r_o is infinite. Taking the early effect into account, Equation (6.86) becomes a more accurate expression given by

$$R_{out} = R_C \,//\, r_o = \frac{R_C r_o}{R_C + r_o}. \tag{6.87}$$

The previously seen CB topologies covered so far mainly showed their small signal model, but they lacked their biasing circuitry. The next circuit, Figure 6.38a, depicts a CB topology with its biasing circuitry as well as its AC paths, including DC blocking capacitors.

We will speed up the pace a little bit describing this circuit, because of some similarities with the biasing circuits covered for the *CE* topology. Referring to Figure 6.38a we see that resistors R_1 and R_2 provide a biasing voltage to forward bias the base-emitter junction; R_C and R_E provide the means to reverse bias the collector-base junction and to establish the collector and emitter currents. Now from an AC standpoint the input signal generator (V_{gen}) with its internal resistance (R_{gen}) is AC coupled via C_{in} into the emitter input. The purpose of C_{in} is not to disturb the biasing voltage of the stage. At the base terminal capacitor C_B provides an AC short-circuit path to the base. The base

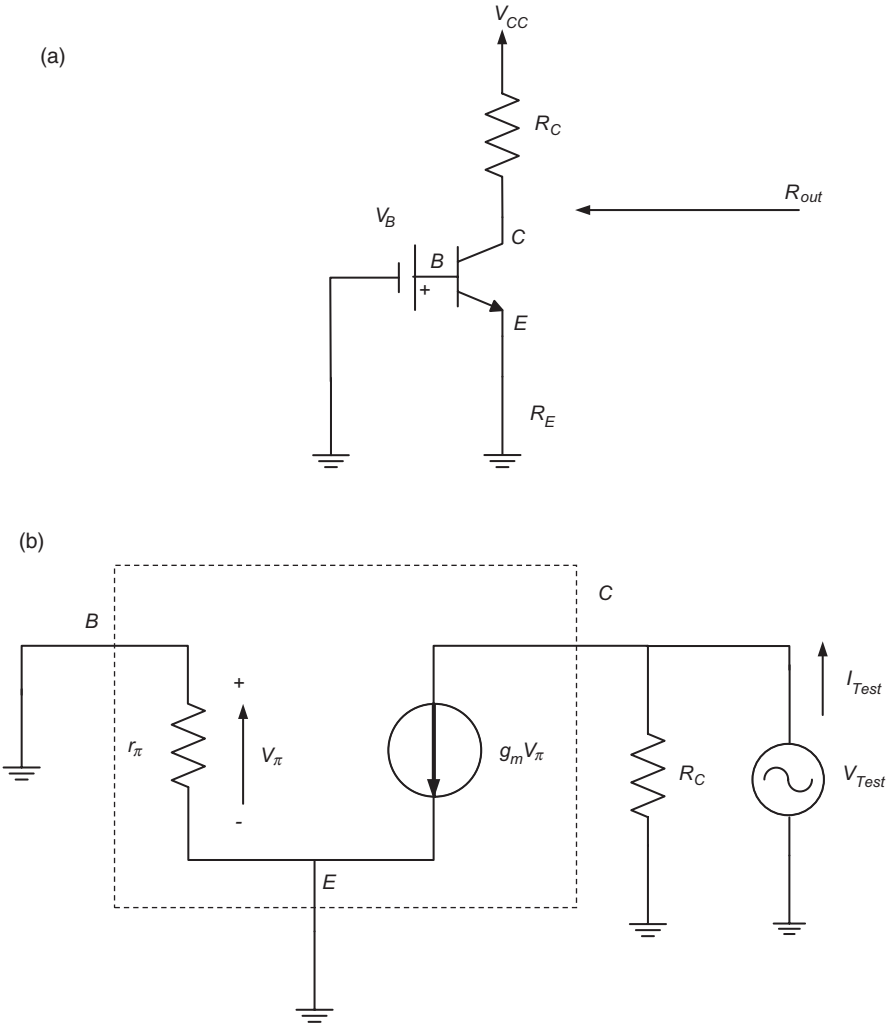

Figure 6.37 (a) CB topology used to calculate the stage output resistance; (b) CB topology after replacing the BJT with its hybrid-π small signal model.

ends up AC grounded as desired. The load resistor R_L that does not participate in the stage biasing is AC coupled via C_L and in effect, it is in parallel with R_C for AC components. It is also important to see that the input resistance seen by the input signal generator is the parallel of the basic CB stage $(1/g_m)$ in parallel with the emitter resistor R_E. Thus, in effect, the CB stage R_{in} becomes

$$R_{in} = (1/g_m)//R_E = \frac{R_E}{1+g_m R_E}. \tag{6.88}$$

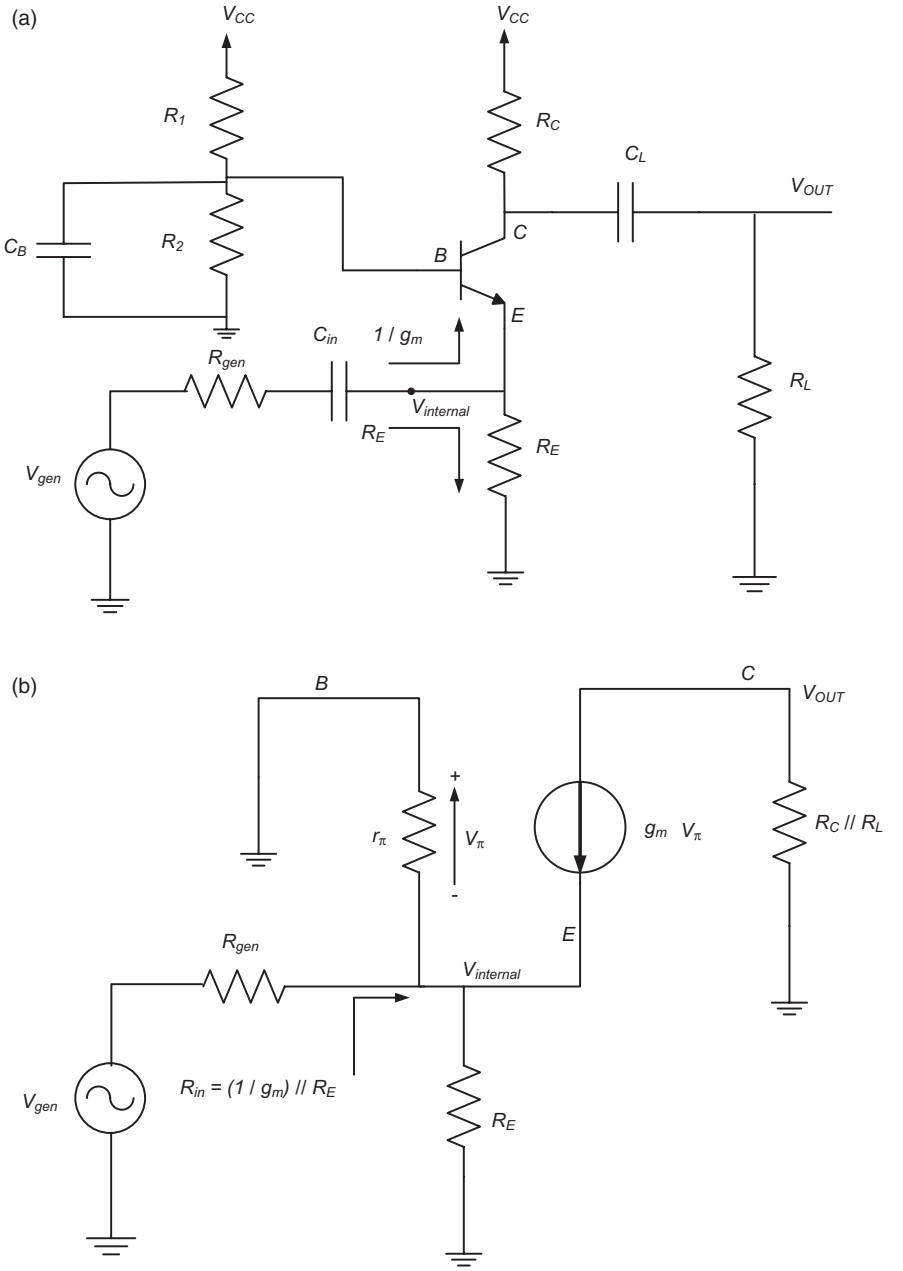

Figure 6.38 (a) CB topology showing biasing circuitry and AC paths; (b) CB topology where the BJT was replaced with its hybrid-π small signal model.

To evaluate the overall voltage gain,

$$G_{CB} = V_{out} / V_{gen} \tag{6.89}$$

We see from Figure 6.38a that voltage $V_{internal}$ equals for AC components to

$$V_{internal} = V_{gen} \frac{R_{in}}{R_{in} + R_{gen}}, \tag{6.90}$$

where R_{in} is the parallel combination of $1/g_m$ and R_E as shown in Figure 6.38b and Equation (6.88).

Since

$$V_{out} / V_{internal} = g_m R_{Par} \tag{6.91}$$

where

$$R_{Par} = \frac{R_C R_L}{R_C + R_L}. \tag{6.92}$$

Combining Equations (6.89) through (6.92) yields

$$G_{CB} = V_{out} / V_{gen} = \frac{1}{1 + (1 + g_m R_E) R_{gen} / R_E} g_m \frac{R_C . R_L}{R_C + R_L}. \tag{6.93}$$

Example 6.14 Let us assume that a 50 Ω coaxial transmission line cable needs to drive the input of amplifier with an input resistance of 10 kΩ. In order to maximize power transfer from one stage to the next, the output impedance of the driving stage, the transmission line in this case, must match the input impedance of the receiving stage, the CB amplifying stage. The output impedance of the CB stage must match the input impedance of the circuit downstream. Figure 6.39a shows this downstream circuit simply as R_{in}. Refer to Figure 6.39a to view the circuit set up. Design a common base amplifier configuration that presents an input impedance of 50 Ω to the coax signals. The amplifier output impedance must be 10 kΩ to match the input impedance R_{in} of the stage that need to be driven.

Solution to Example 6.14

From Equations: (6.86) and (6.88) we know that:

$$R_{out} = R_C .$$

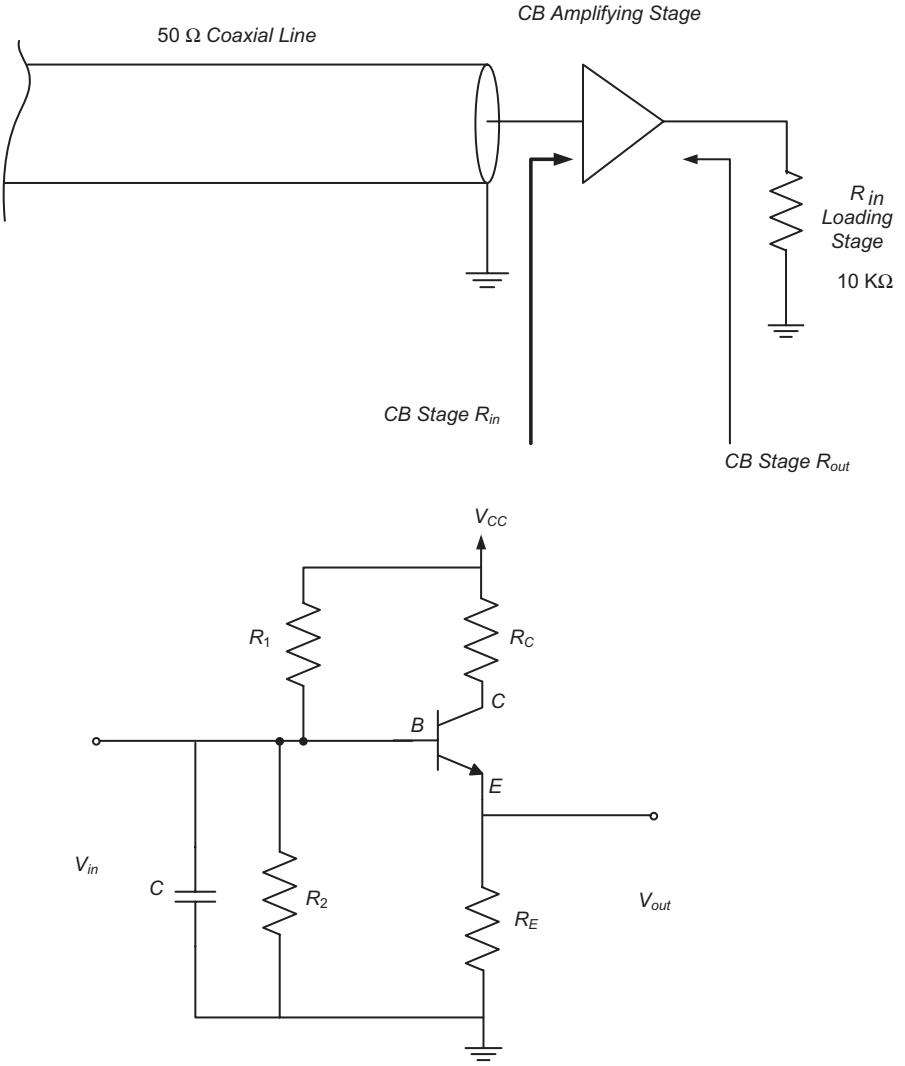

Figure 6.39 Common base (CB) design, Example 6.14, and CB stage.

Ignoring the Early effect of the BJT, and

$$R_{in} = (1/g_m)//R_E = \frac{R_E}{1+g_m R_E}. \tag{6.94}$$

We need the CB stage R_{in} to be 50 Ω, and we need an $R_{out} = 10$ kΩ. Since $R_{out} = R_C$, if we obtain a BJT with a g_m of 1/53 Ω or 0.0188679 S and $R_E = 1$ kΩ, it yields

$$R_{in} = (1/g_m)//R_E = 53//1000 \approx 50\ \Omega.$$

And since we are ignoring the Early effect, $r_o \to \infty$, thus R_{out} simple equals R_C, hence:

$$R_{out} = 10\ \text{k}\Omega.$$

Finally, the CB amplifier needs to be biased such that a g_m of 0.0188679 S is obtained. Since $g_m = I_C/V_T$ and $V_T = 0.026$ V at room temperature, then we need a collector biasing current of

$$I_C = g_m V_T = 0.0188679 \times 0.026 = 0.49\ \text{mA}.$$

The selection of resistors R_1 and R_2 are left as an exercise to the reader.

6.3.14 The Common-Collector (CC) Configuration

The CC configuration is also commonly referred to as emitter follower. This configuration has the BJT's collector AC grounded terminal. The input to this stage is applied between the base and ground, the output is sensed between the emitter and ground. The core circuit of the emitter follower is depicted in Figure 6.40. Note that the collector is tied to V_{CC}, thus its AC signals are effectively grounded.

When the input voltage grows, more base current is injected into the BJT, causing the collector and emitter currents to increase. The output voltage V_{out} is never higher than the input voltage V_{in}. Voltage increments in the base cause increments in the voltage V_{out} across R_E than can never keep up with the base voltage because of the base-emitter voltage drop. Figure 6.41 depicts an emitter follower stage BJT small signal model.

Looking at the small signal model of Figure 6.41 we can state KCL equations at node V_{out} and obtain

$$\frac{V_\pi}{r_\pi} + g_m V_\pi = \frac{V_{out}}{R_E}. \tag{6.95}$$

Doing some algebra on Equation (6.95) and taking into account that: $\beta = g_m r_\pi$ (from Table 6.3),

$$V_\pi = \frac{r_\pi}{\beta + 1} \cdot \frac{V_{out}}{R_E}. \tag{6.96}$$

From the circuit of Figure 6.41 we can see that

$$V_{in} = V_\pi + V_{out}.$$

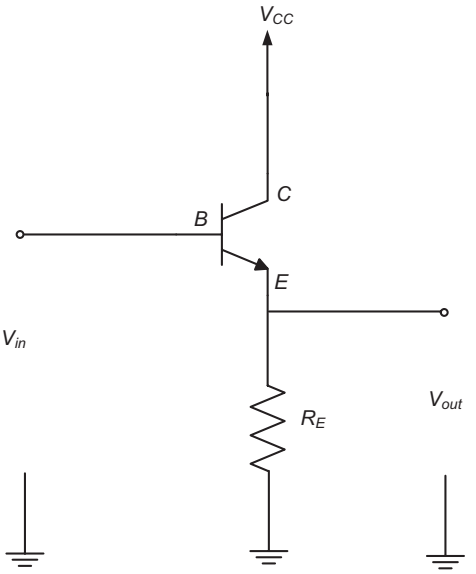

Figure 6.40 Core structure of an emitter follower stage.

Combining V_{in} with Equation (6.96) we obtain

$$G_{CC} = \frac{V_{out}}{V_{in}} = \frac{1}{1 + \frac{r_\pi}{\beta + 1} \cdot \frac{1}{R_E}}, \tag{6.97}$$

and since

$$\frac{r_\pi}{\beta + 1} \approx \frac{r_\pi}{\beta}. \tag{6.98}$$

Using Equation (6.98) in Equation (6.97) yields

$$G_{CC} = \frac{V_{out}}{V_{in}} \approx \frac{R_E}{R_E + \frac{1}{g_m}}. \tag{6.99}$$

From Equation (6.99) it is clear to see that the CC topology voltage gain is always positive and less than *unity*.

Now let us look at the emitter follower stage gain, when fed by an input signal with source resistance (R_S). Figure 6.42a depicts the circuit with the input signal associated with a source resistance. We now proceed to find out

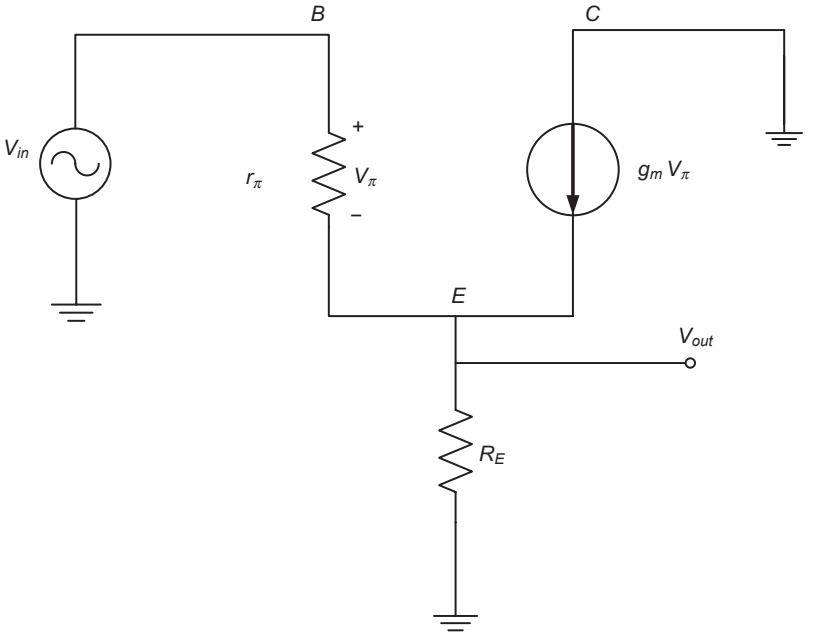

Figure 6.41 Emitter follower stage small signal model.

the gain for this circuit. We apply Thévenin's Theorem to the circuit of Figure 6.42a. We select the emitter resistor to be the element we keep, while we look into replacing the rest of the circuit with its Thévenin's equivalent; as usual we inhibit independent voltage source V_{in}; that is, we replace it with a short circuit. Remember that Thévenin's Theorem does not want you to remove any dependent sources. We calculate the Thévenin resistance injecting a Thévenin voltage source between the emitter and ground nodes. Figure 6.41b depicts the circuit used to calculate the Thévenin's resistance.

Applying KCL at node E to the circuit of Figure 6.42b we obtain

$$\frac{V_\pi}{r_\pi} + g_m . V_\pi = -I_{Thev} . \tag{6.100}$$

By inspection of the circuit we find

$$-V_\pi = \frac{r_\pi}{r_\pi + R_S} V_{Thev} . \tag{6.101}$$

Combining Equations (6.101) and (6.100) it yields

$$Z_{Thev} = V_{Thev} / I_{Thev} = \frac{r_\pi}{\beta + 1} + \frac{R_S}{\beta + 1}$$

and since $r_\pi/(\beta+1) \approx r_\pi/\beta = 1/g_m$ (Z_{Thev}) becomes:

$$Z_{Thev} = V_{Thev} / I_{Thev} = \frac{1}{g_m} + \frac{R_S}{\beta+1}$$

The Thévenin voltage is $V_{Thev} = V_{in}$, and using Z_{Thev} from above according to the circuit of Figure 6.42b, which basically is a resistor divider, leads to

$$\frac{V_{out}}{V_{in}} = \frac{R_E}{R_E + \frac{R_S}{\beta+1} + \frac{1}{g_m}}. \tag{6.102}$$

The input impedance of the emitter follower stage is calculated from the transistor and small signal circuit model of Figure 6.42. A voltage V_X is injected into the input of the stage, a current I_X is produced. The input resistance R_{in} is the ratio of V_X and I_X. Applying KCL at node E of the circuit of Figure 6.42b we obtain

$$V_X = V_\pi + (I_X + g_m V_\pi) R_E. \tag{6.103}$$

Since from Figure 6.43b we have that

$$V_\pi = I_X r_\pi. \tag{6.104}$$

Plugging Equation (6.104) in Equation (6.103) we obtain (see also Fig. 6.44b)

$$V_X = I_X r_\pi + (I_X + g_m I_X r_\pi) R_E \tag{6.105}$$

and since from Table 6.3

$$g_m r_\pi = \beta. \tag{6.106}$$

Plugging Equation (6.106) in Equation (6.105) after a little bit of algebra results to

$$R_{in\ emitter\text{-}follower} = \frac{V_X}{I_X} = r_\pi + (\beta+1) R_E. \tag{6.107}$$

It is important to see that the input impedance of an emitter-follower stage is identical to the input impedance of a common-collector stage with emitter degeneration resistance; refer to Equations (6.107) and (6.77).

Now let us calculate the output impedance of an emitter-follower stage. Figure 6.44c,d depicts the output impedance and its components.

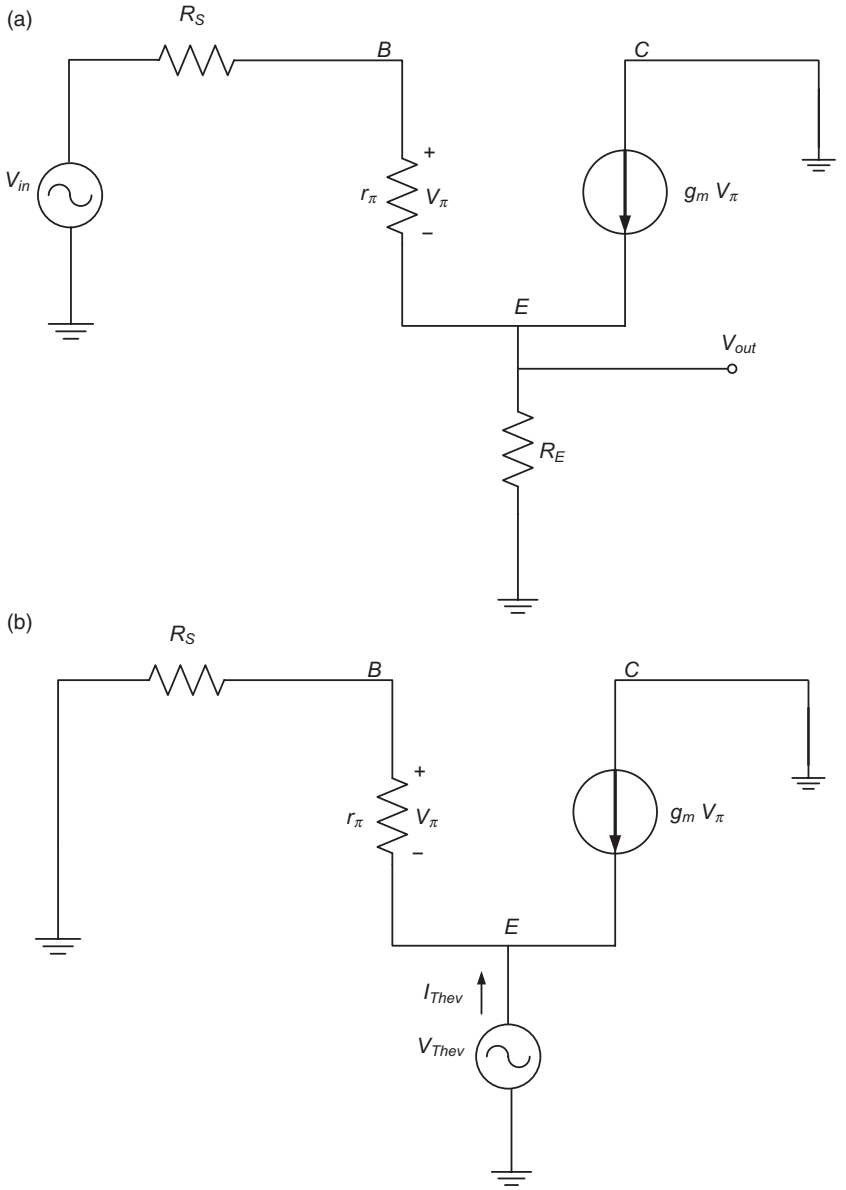

Figure 6.42 (a) Emitter-follower with source resistance small signal circuit model; (b) emitter-follower with source resistance small circuit model used to calculate R_{Thev}.

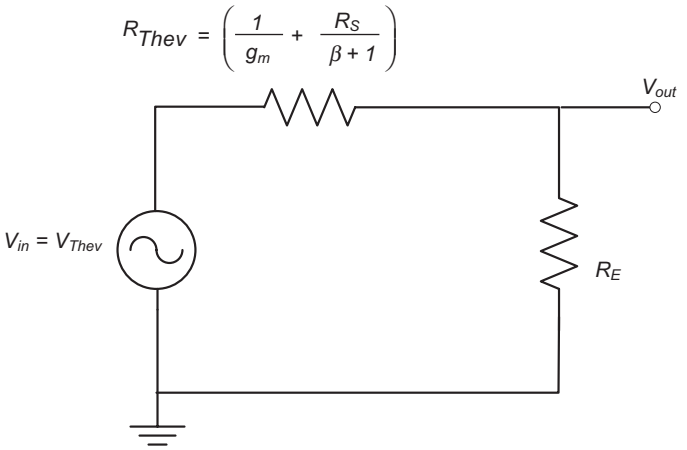

Figure 6.43 Emitter follower gain: input resistance calculation with source resistance using Thévenin's Theorem.

The computation of the emitter-follower output impedance components is performed using Figure 6.44c,d. Referring now to Figure 6.44c,d, the output impedance of the follower stage is simply the parallel of the two output impedance components, hence:

$$R_{out} = \left(\frac{1}{g_m} + \frac{R_S}{\beta + 1}\right) // R_E \tag{6.108}$$

Equation (6.108) ignores the Early effect. Taking this effect into account, the output impedance becomes

$$R_{out} = \left(\frac{1}{g_m} + \frac{R_S}{\beta + 1}\right) // R_E // r_o$$

where g_m is the transistor's transconductance, R_S is the input signal internal resistance also called the source resistance, β is the transistor current gain parameter, R_E is the emitter resistor, and r_o is the transistor model output resistance due to the Early effect.

6.4 METAL OXIDE FIELD EFFECT TRANSISTOR (MOSFET)

The *n-channel* enhancement mode MOSFET, also called an NMOS transistor is discussed next. Later on we will briefly discuss the *p-channel* enhancement mode MOSFET (or PMOS) and the two depletion type MOSFETs (*n-channel* D-MOSFET and *p-channel* D-MOSFET).

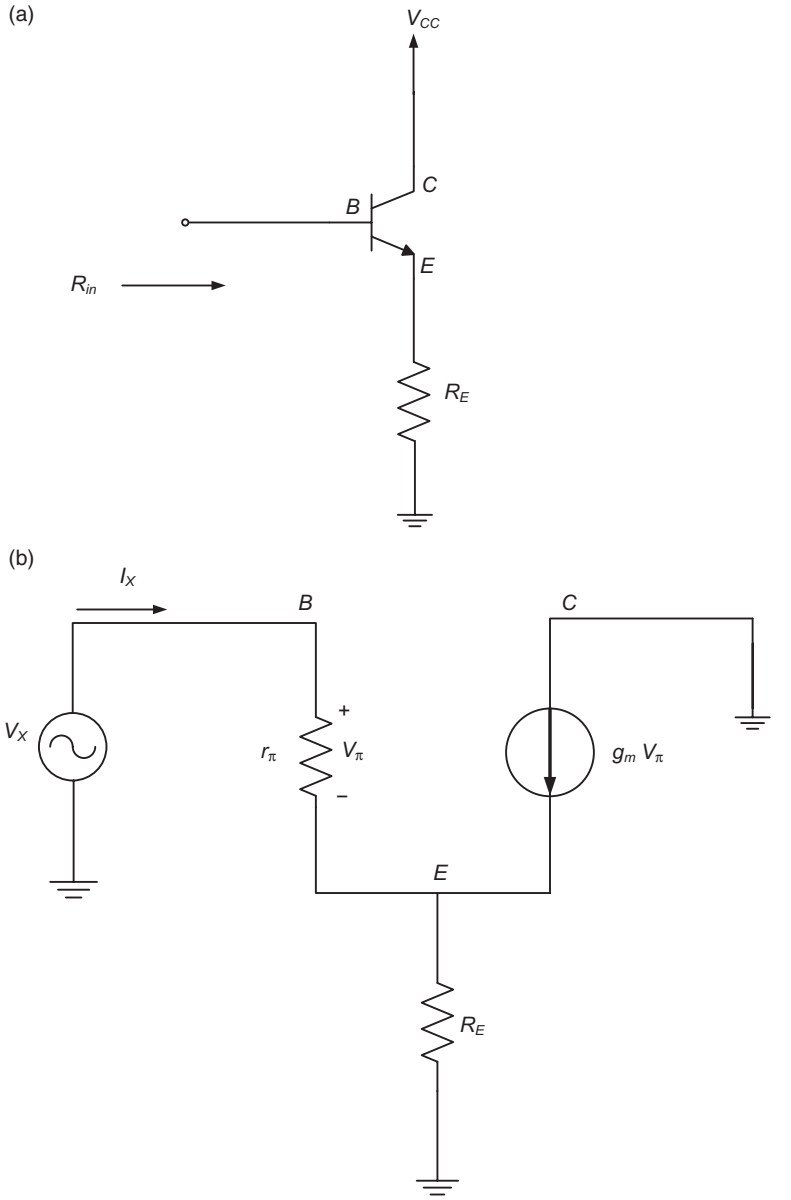

Figure 6.44 (a) Emitter-follower circuit and input impedance calculation; (b) follower small signal model to calculate input resistance; (c) emitter-follower for the calculation of output resistance; (d) emitter-follower with calculated output resistance.

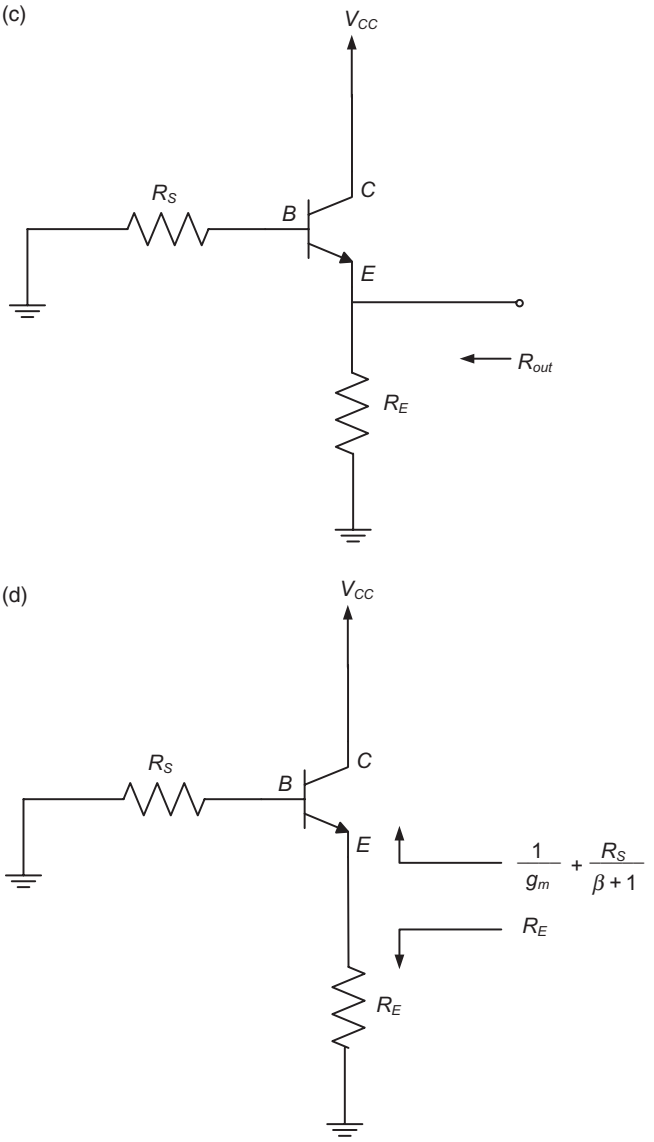

Figure 6.44 (*Continued*)

The enhancement mode *n-channel* MOSFET may conduct an electric current between its *drain* and *source* terminals when a positive voltage is applied to the *gate*. Figure 6.45 depicts the basic structure of an *n-channel* enhancement mode MOSFET. The drain-to-source current is controlled by the magnitude of the gate voltage. For the time being, we are describing the

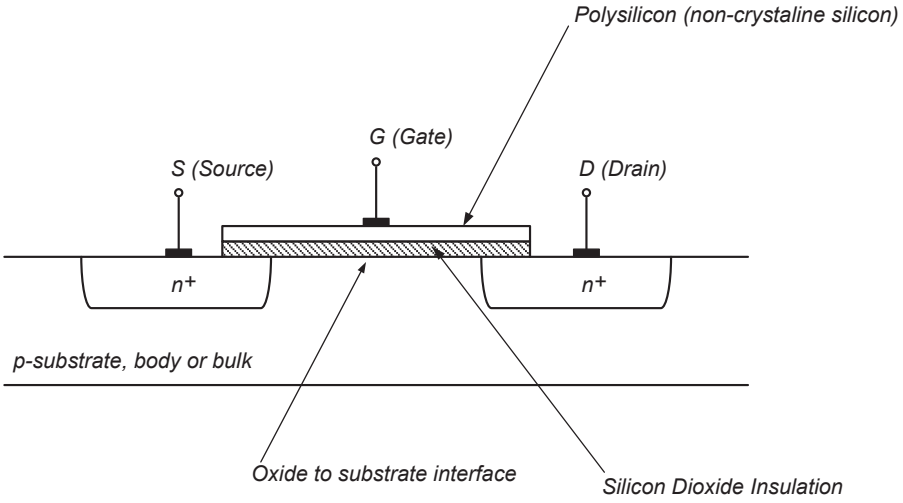

Figure 6.45 Basic MOSFET structure.

Table 6.4 MOSFET types

Enhancement Mode		Depletion Mode	
n-channel Induced channel	*p*-channel Induced channel	*n*-channel Implanted channel	*p*-channel Implanted channel

enhancement mode *n-channel* MOSFET. Table 6.4 lists the four MOSFET types that are available.

MOSFETs have either three or four terminals. *Gate, Drain* and *Source* in all cases and in some cases discrete MOSFETs have a fourth terminal or the body terminal that may be externally connected to the desired voltage. For medium to low frequencies, the MOSFET gate current is zero because the silicon dioxide behaves as an insulator (Fig. 6.45).

Only upon operating the MOSFET at high frequencies there may be a nonzero or significant gate current due to the internal parasitic capacitances within the device structure. Within our coverage of MOSFETs we will not deal with the MOSFET operating at high frequencies. High frequencies are considered those frequencies well above audio frequencies or 20 kHz. For example, in applications where MOSFETs are used at hundreds of kHz, such as in switching power supplies, MOSFET gate currents are not negligible. Unlike the bipolar transistor, which conducts majority as well as minority carriers, MOSFET currents are unipolar and its current consists of majority carriers. *N-channel* MOSFETs conduct currents of electrons while *p-channel* types conduct currents of holes.

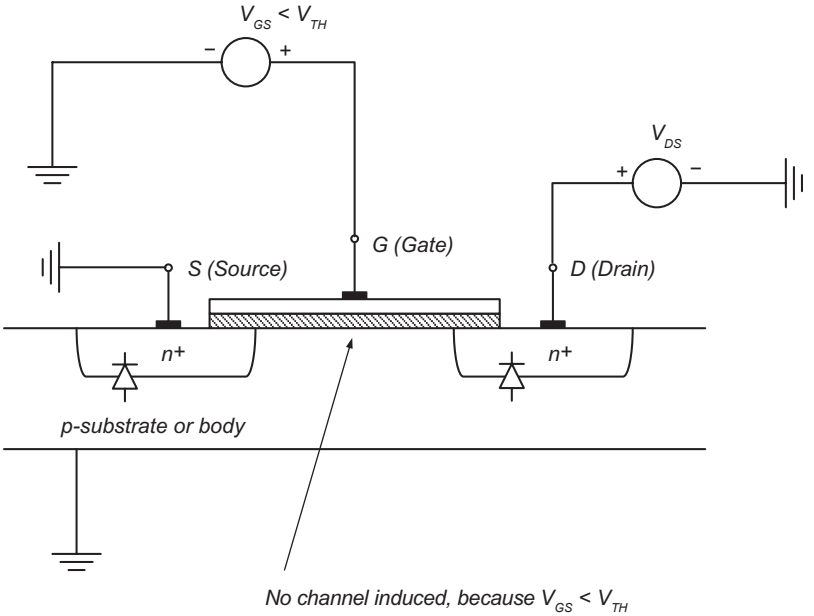

Figure 6.46 MOSFET operating with $V_{GS} < V_{TH}$, $I_D = 0$.

6.4.1 MOSFET *I-V* Characteristics

Let us look into the behavior of the *n-channel* MOSFET from "currents and voltages" point of view. Figure 6.46 depicts an *n-channel* enhancement mode MOSFET with its *source* terminal grounded and a positive voltage V_{DS} applied to its drain. If the *gate* voltage applied is under the so-called MOSFET threshold voltage V_{TH}, no drain-to-source current flows through the MOSFET substrate (Fig. 6.46) and no channel between the *drain* and *source* has been formed yet. More positive charge accumulates on the gate and negative ions form in the substrate with higher positive gate voltages. This is referred to as the depletion region.

The MOSFET is said to be *"off."* As the gate voltage V_G increases beyond the threshold voltage (V_{TH}) free electrons are attracted to the region between the silicon dioxide and the substrate and creates a channel. It is said that the channel is *induced*. When this channel is created, the MOSFET starts conducting a current from *drain* to *source*. The larger V_{GS} becomes, the deeper the channel. Note that the gate never conducts any current (in low and mid-frequencies operation), and the gate acts like a capacitor controlling the channel length and depth. Referring again to Figure 6.46, it is important to note that there are two diodes, one of them between the p-substrate and the drain and a second diode between the p-substrate and the source. It is important not to allow these diodes to conduct any current when the MOSFET is

still off, thus the p-substrate is grounded, preventing such diodes from becoming forward biased and current flowing through them.

The current voltage relationship of the NMOS MOSFET is given without proof and it is

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2]. \tag{6.109}$$

In Equation (6.109) μ_n is the carrier mobility of the electrons in the *n-channel*, C_{ox} is the capacitance formed by the oxide in between gate polysilicon and the p-substrate, this capacitance is greatly controlled by the thickness of such oxide. W is the width of the channel, L is the length of the channel, W/L is referred to as the aspect ratio of the MOS transistor, V_{GS} is the gate to source voltage applied, V_{TH} is the MOSFET threshold voltage, and V_{DS} is the MOSFET drain-to-source voltage. Once a MOSFET technology is chosen, the oxide thickness (t_{ox}) is fixed and cannot be changed, the aspect ratio W/L is under control of the integrated circuit designer.

As the gate voltage is gradually increased, the MOSFET practically acts as a variable resistor. During this region of operation, the drain current (I_D) maintains a linear relationship with respect to the drain-to-source voltage (V_{DS}). The slope of this part of the *I-V* curve equals $1/R_{DSon}$, where R_{DSon} is the drain-to-source on-resistance of the MOSFET. Equation (6.109) is a nonlinear relationship between I_D and V_{DS}. When:

$$V_{DS} \ll 2\,(V_{GS} - V_{TH}) \tag{6.110}$$

Equation (6.109) reduces to

$$I_D \approx \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})V_{DS} \tag{6.111}$$

Since

$$R_{DSon} = V_{DS} / I_D \tag{6.112}$$

Plugging Equation (6.111) into Equation (6.112) we obtain:

$$R_{Dson} = \frac{1}{\mu_n C_{ox}\dfrac{W}{L}(V_{GS} - V_{TH})}. \tag{6.113}$$

Equation (6.113) means that for very small V_{DS} values the parabola given by Equation (6.109) is approximated by the linear behavior of Equation (6.112). By inspection of Equation (6.113), it is interesting to see that the transistor R_{Dson} is directly proportional to the channel length (L) and inversely

proportional to the channel width (W). This should also be an intuitive conclusion. Equation (6.109) is the expression of the drain current for all values of V_{DS}, and it is the equation of a parabola. If we took the first derivative of Equation (6.109), find its zero and then evaluate its second derivative at the same point, which would yield a negative result. So without doing the mathematical derivation, it can easily be stated that Equation (6.109) has a maximum at

$$V_{DS} = V_{GS} - V_{TH}. \tag{6.114}$$

So evaluating Equation (6.109) using the value of V_{DS} from Equation (6.114) we find

$$I_{D,MAX} \approx \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2 \tag{6.115}$$

The maximum value of I_{DS} shown by Equation (6.115) is the value of current when

$$V_{DS} > V_{GS} - V_{TH}. \tag{6.116}$$

When the MOSFET operates under such conditions, that is, Equation (6.116), it is said to be in its saturation region of operation as depicted by Figure 6.47.

It is important to observe that Equation (6.115) is independent of V_{DS}. This says that the curves for the drain current become constant, and independent of V_{DS} after the pinch-off voltage, that is, $V_{DS} = V_{GS} - V_{TH}$. After the MOS transistor reaches the pinch-off voltage, the drain current does not significantly change with V_{DS}. Such statement is true provided that we do not take into account a second-order effect referred to as *channel length modulation*. Figure 6.47a,b describes the different regions of the MOSFET operation given by Equations (6.109) through (6.116).

The channel length moves with the change of V_{DS}. This effect can be visualized in Figure 6.48: (a) shows the induced channel, (b) shows the pinched-off channel, and (c) shows channel length modulation.

The *channel length modulation effect* is accounted for in Equation (6.115) by multiplying it by the factor: $(1 + \lambda V_{DS})$ that yields

$$I_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{TH})^2(1 + \lambda V_{DS}). \tag{6.117}$$

In Equation (6.117), λ is called the channel length modulation coefficient.

The effect that channel length modulation produces on the drain current characteristics is a slight positive slope as shown in Figure 6.49. Another second-order effect is the body effect; this takes place when the substrate potential grows above zero, and this causes the threshold voltage to increase. We will not consider the body effect in this book.

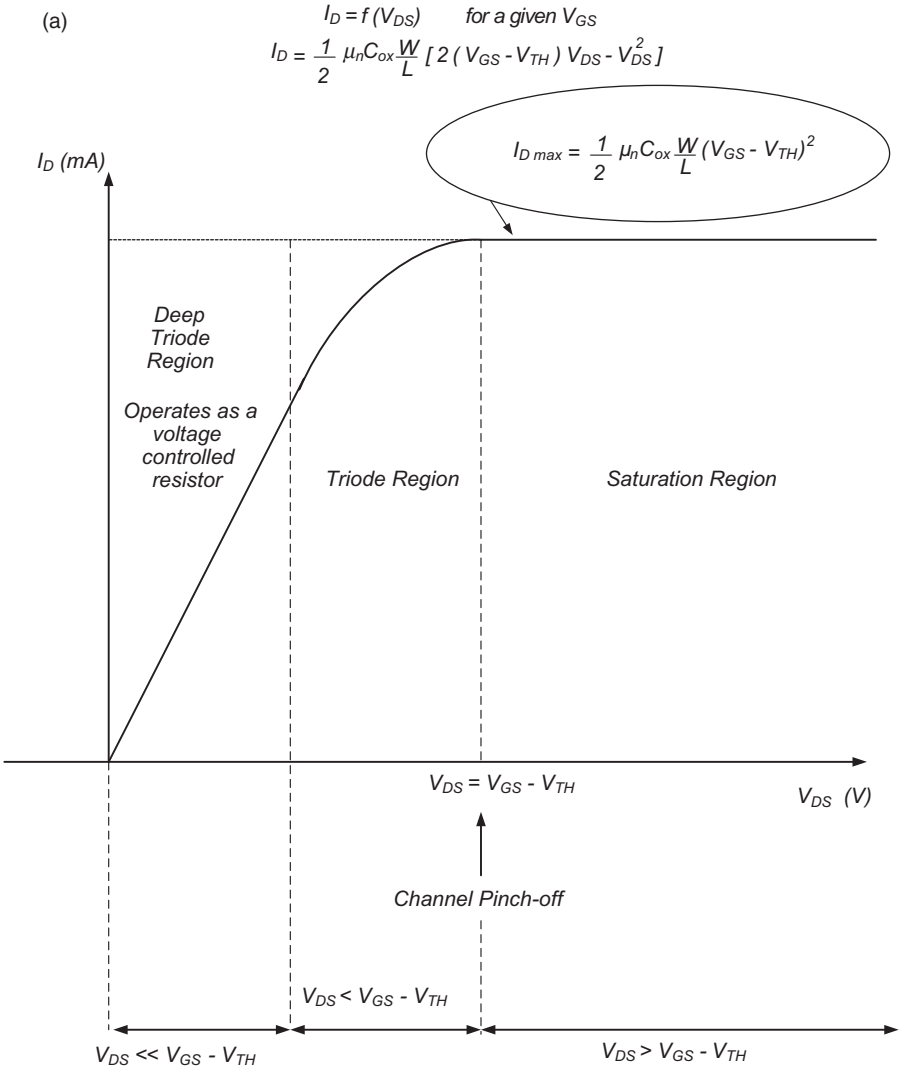

Figure 6.47 (a) MOSFET triode and saturation regions; (b) MOSFET triode region.

6.4.2 MOSFET Small Signal Model

The small signal model of a MOSFET is similar to the small signal model of the bipolar transistor. The basic model consists of a voltage-controlled current source (*VCCS*), its current value is $g_m V_{GS}$, where g_m is the MOSFET *trans-conductance* and V_{GS} is the gate to source controlling voltage. The transistor trans-conductance is given by

$$g_m = \frac{\partial I_D}{\partial V_{GS}}. \tag{6.118}$$

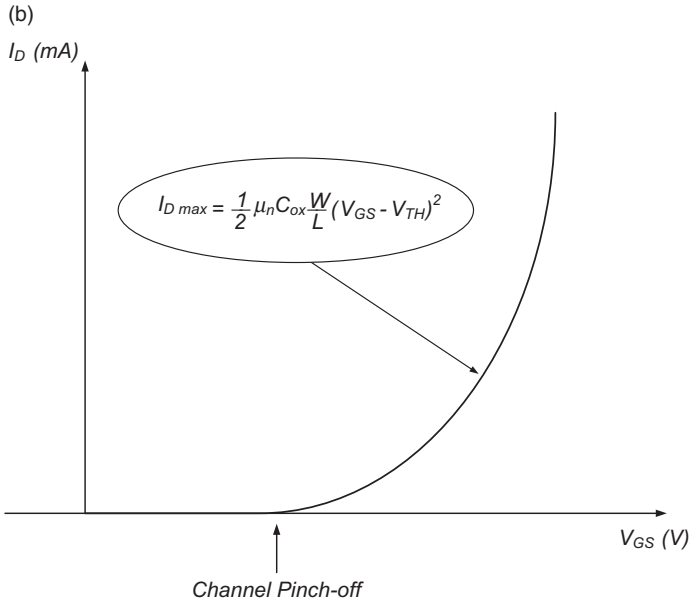

Figure 6.47 (*Continued*)

Using Equation (6.118) for the saturation region without the effect of channel length modulation we obtain:

$$g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH}). \tag{6.119}$$

The accountability of the channel length modulation, that is, the dependence of the saturation current with V_{DS}, is included with the addition of an output resistor r_o, where

$$r_o = \left(\frac{\partial I_D}{\partial V_{DS}}\right)^{-1} = \frac{1}{\frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2\lambda} \approx \frac{1}{\lambda I_D}. \tag{6.120}$$

Figure 6.51 depicts the small signal, low, and medium frequencies equivalent model of a MOSFET.

6.4.3 MOSFET Biasing Techniques

Let us start by pointing out the fundamental differences and similarities between bipolar and MOS transistors at the terminal voltage and current levels. Table 6.5 basically summarizes key differences and similarities between BJTs and MOSFETs. However, Table 6.5 does not address differences and similarities directly pertaining to semiconductor physics.

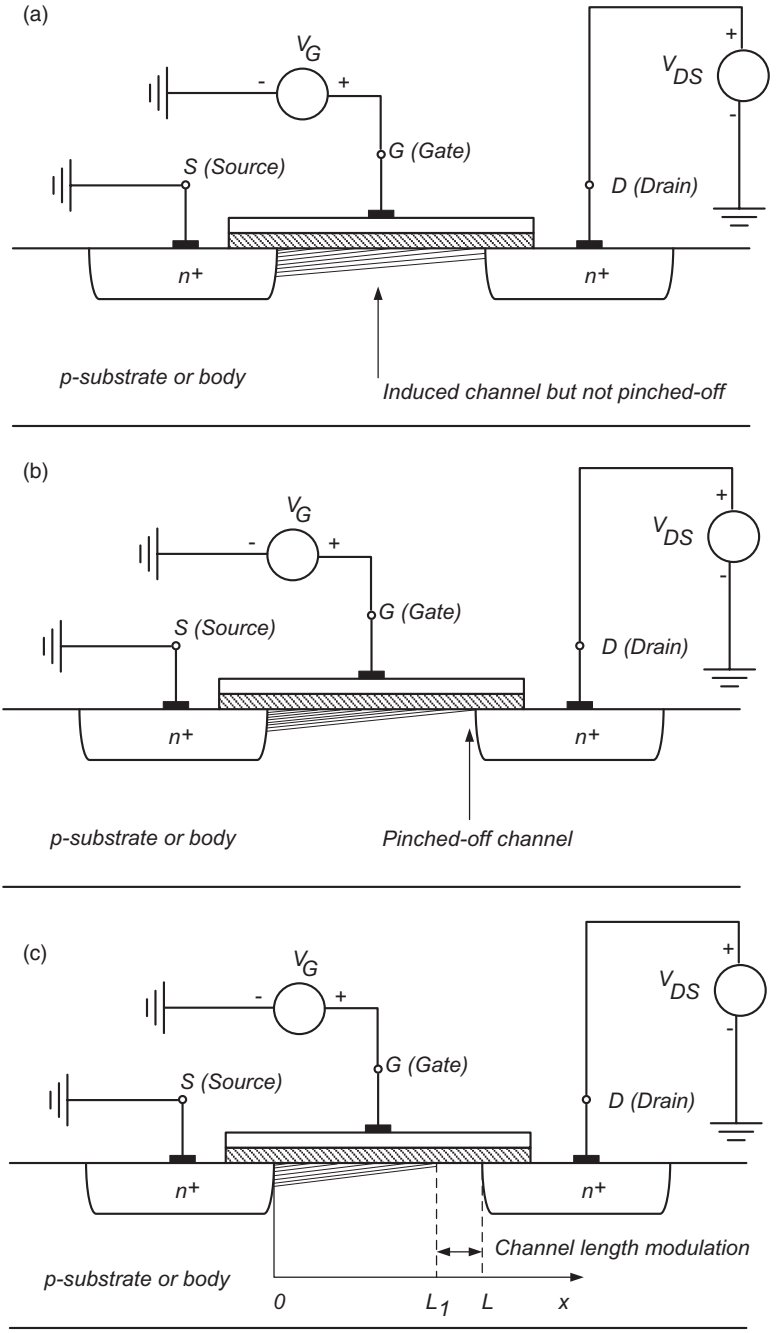

Figure 6.48 (a) Induced channel but not pinched-off yet; (b) pinched-off channel; (c) channel length modulation effect.

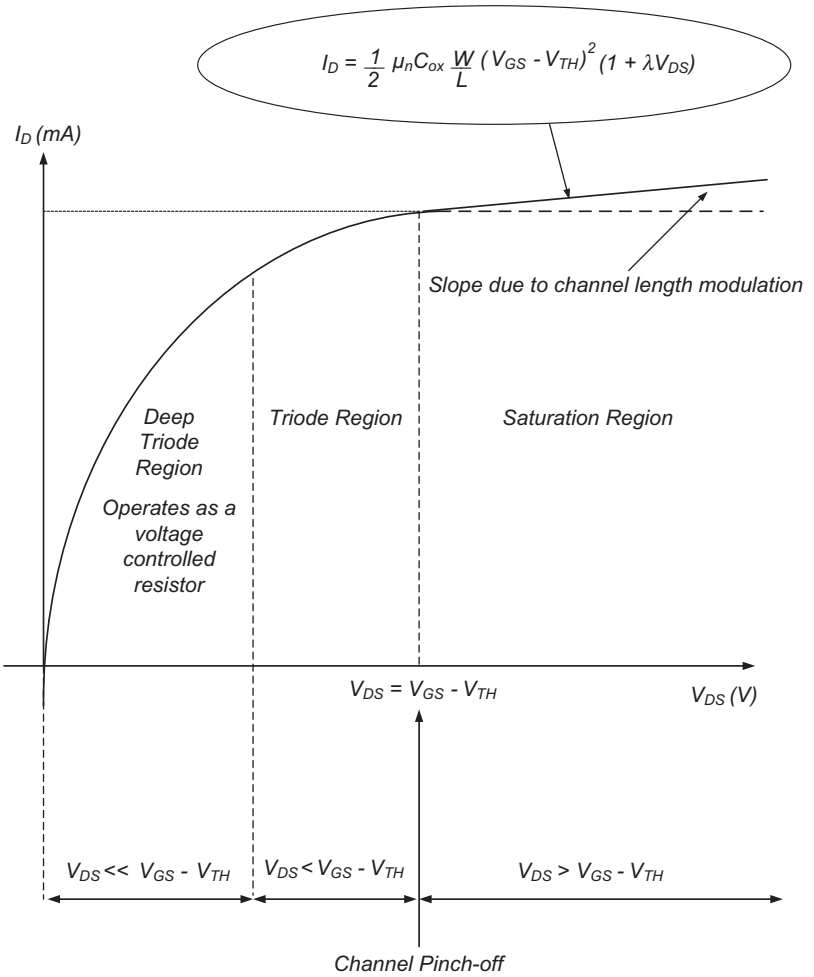

Figure 6.49 N-channel MOSFET: I-V characteristics depicting the effect of channel length modulation.

Taking into account the facts listed in Table 6.5, it is possible to find some similarities as well as differences biasing BJTs and MOSFETs. The remainder of this chapter will leverage on the previously addressed BJT material and is presented in a more speedy fashion.

Let us consider the MOSFET circuit of Figure 6.50; we want to bias the transistor such that it operates in the saturation region. Ignoring channel length modulation we have that

$$V_G = \frac{R_2}{R_1 + R_2} V_{DD}. \tag{6.121}$$

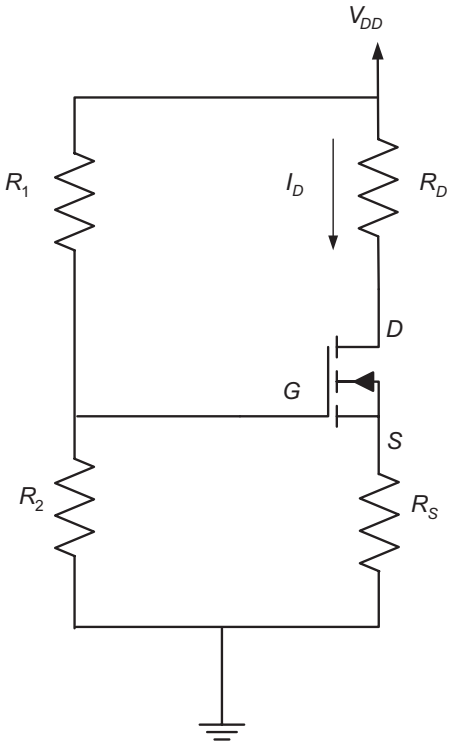

Figure 6.50 N-channel MOSFET biasing.

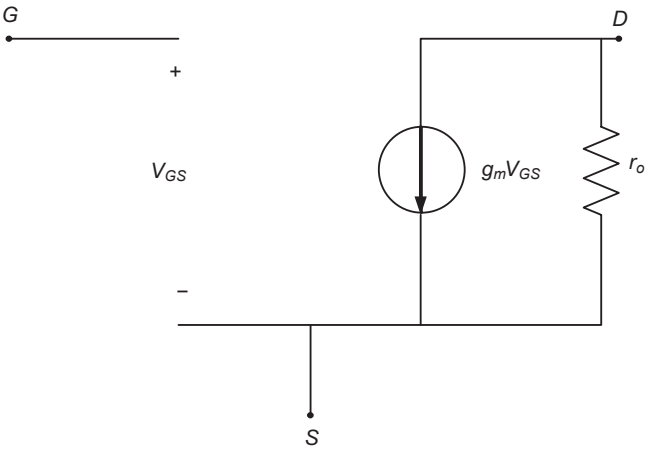

Figure 6.51 MOSFET small signal equivalent model for low and mid frequencies.

Table 6.5 Some fundamental circuit differences and similarities between BJTs and MOSFETs

BJT	MOSFET
Difference: BJT has no body or substrate	Difference: MOSFET has a substrate
Difference: When $V_{BE} = V_{CE}$ BJT is at the edge of the active region	Difference: MOSFET is at the edge of saturation if V_D is below $V_G - V_{TH}$
Difference: Finite (nonzero) base current	Difference: Zero gate current at mid and low frequencies
Difference: Exponential $I_C - V_{BE}$ characteristics	Difference: Square law dependence between I_D and V_{GS}
Difference: Most BJTs have the same I_S reverse saturation current	Difference: MOSFETs have selectable-by-design W/L aspect ratios
Difference: Two BJT types: NPN and PNP	Difference: Four MOSFET types: 2 enhancement mode types: *n*-channel and *p*-channel and 2 depletion mode types: *n*-channel and *p*-channel
Three regions of operation: saturation, active, and cutoff (*)	Three regions of operation: triode (includes deep triode region), saturation, and cutoff (*)
(*) May qualify as a similarity and as a difference	(*) May qualify as a similarity and as a difference
Difference: BJT saturation region is not the same as MOSFET saturation region	Difference: MOSFET saturation region is not the same as BJT saturation region
Similarity: base, collector, and emitter	Similarity: gate, drain, and source
Similarity: Voltage controlled-current source-based small signal model	Similarity: Voltage controlled-current source-based small signal model
Similarity: common emitter amplifier	Similarity: common source amplifier
Similarity: common collector amplifier	Similarity: common drain amplifier
Similarity: common base amplifier	Similarity: common gate amplifier
Similarity: BJT can operate as a switch	Similarity: MOSFET can operate as a switch

It is important to recognize that voltage V_G at node G in Figure 6.50 refers to the gate voltage with respect to ground and not to the gate voltage with respect to the MOSFET source terminal.

From KVL we can see that

$$V_G = V_{GS} + I_D R_S. \tag{6.122}$$

Combining Equations (6.121) and (6.122) we obtain

$$\frac{R_2}{R_1 + R_2} V_{DD} = V_{GS} + I_D R_S. \tag{6.123}$$

Since the saturation current of the MOSFET, from Equation (6.115) is

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2, \tag{6.124}$$

combining Equation (6.123) with Equation (6.124) it yields

$$\left(\frac{R_2}{R_1 + R_2}V_{DD} - V_{GS}\right)\frac{1}{R_S} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2. \tag{6.125}$$

Performing some algebraic operations on Equation (6.125) yields

$$V_{GS} = -(V_a - V_{TH}) + \sqrt{(V_a - V_{TH})^2 - V_{TH}^2 + \frac{2R_2}{R_1 + R_2}V_a V_{DD}} \tag{6.126}$$

$$V_{GS} = -(V_a - V_{TH}) + \sqrt{V_a^2 + 2V_a\left(\frac{R_2 V_{DD}}{R_1 + R_2} - V_{TH}\right)} \tag{6.127}$$

where

$$V_a = \frac{1}{\mu_n C_{ox}\dfrac{W}{L}R_S}.$$

Finally, we must verify that: $V_{DS} > V_{GS} - V_{TH}$ to satisfy the saturation condition.

When we solve problems it will be more straightforward and faster to use Equation (6.115) to calculate drain current. Making initial guesses of V_{GS} to calculate I_D will take longer to converge.

Example 6.15 Using the circuit of Figure 6.50 assume the following values: $V_{DD} = 10$ V, $R_1 = 40$ kΩ, $R_2 = 100$ kΩ, $R_S = 200$ Ω, and MOSFET parameters: $V_{TH} = 0.5$ V, $\mu_n C_{ox} = 100$ μA/V^2, $W/L = 50$, and $\lambda = 0$. Calculate the maximum allowable value of R_D for the MOSFET to remain on the edge of saturation. Assume $V_{GS} = 3$ V.

Solution to Example 6.15

From inspection of Figure 6.50, we can state that

$$V_{GG} = V_{GS} + I_D R_{DS}. \tag{6.128}$$

In Equation (6.128) V_{GG} is the gate voltage to ground. Since the gate current is negligible

$$V_{GG} = \frac{R_2}{R_1 + R_2}V_{DD} = 7.14 \text{ V}. \tag{6.129}$$

And since

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{TH})^2, \tag{6.130}$$

using the values provided by the example, Equation (6.130) yields

$$I_D = 15.63\,\text{mA}.$$

The condition for the MOSFET to be on the edge of saturation is

$$V_{DS} = V_{GS} - V_{TH},$$

and since $V_{GS} = 3$ V and $V_{TH} = 0.5$ V, it yields

$$V_{DS} = 2.5\ \text{V}.$$

By inspection of Figure 6.50, we see that $V_{DD} = R_D I_D + V_{DS} + R_S I_D$. Using the given values in the above equation, $10 = R_D\,0.01563 + 2.5 + 200\,0.01563$. From the above equation we find the value of R_D to be

$$R_D \cong 280\ \Omega.$$

6.4.4 Common Source (CS) Configuration

The MOSFET CS configuration is very similar to the BJT common emitter configuration. The gain of this circuit turns out to be $-g_m R_D$ which is basically the same expression given for the common emitter. Figure 6.52 depicts a common source amplifier and its small signal model. Figure 6.52b shows that the channel length modulation coefficient $\lambda = 0$, thus $r_o \to \infty$, calculation of the voltage gain leads to

$$G_{CS} = -g_m R_D \tag{6.131}$$

ignoring channel length modulation.

Taking into account channel length modulation, that is, finite and nonzero r_o, the voltage gain becomes

$$G_{CS} = -g_m(\mathrm{R_D} /\!/ r_o). \tag{6.132}$$

It is important and interesting to observe that for the CS stage R_{in} approaches infinity,

$$R_{in} \to \infty \tag{6.133}$$

at mid and low frequencies of operation.

The CS stage output impedance is $R_{out} = R_D$ ignoring channel length modulation, or $R_{out} = R_D /\!/ r_o$ do taking into account channel length modulation.

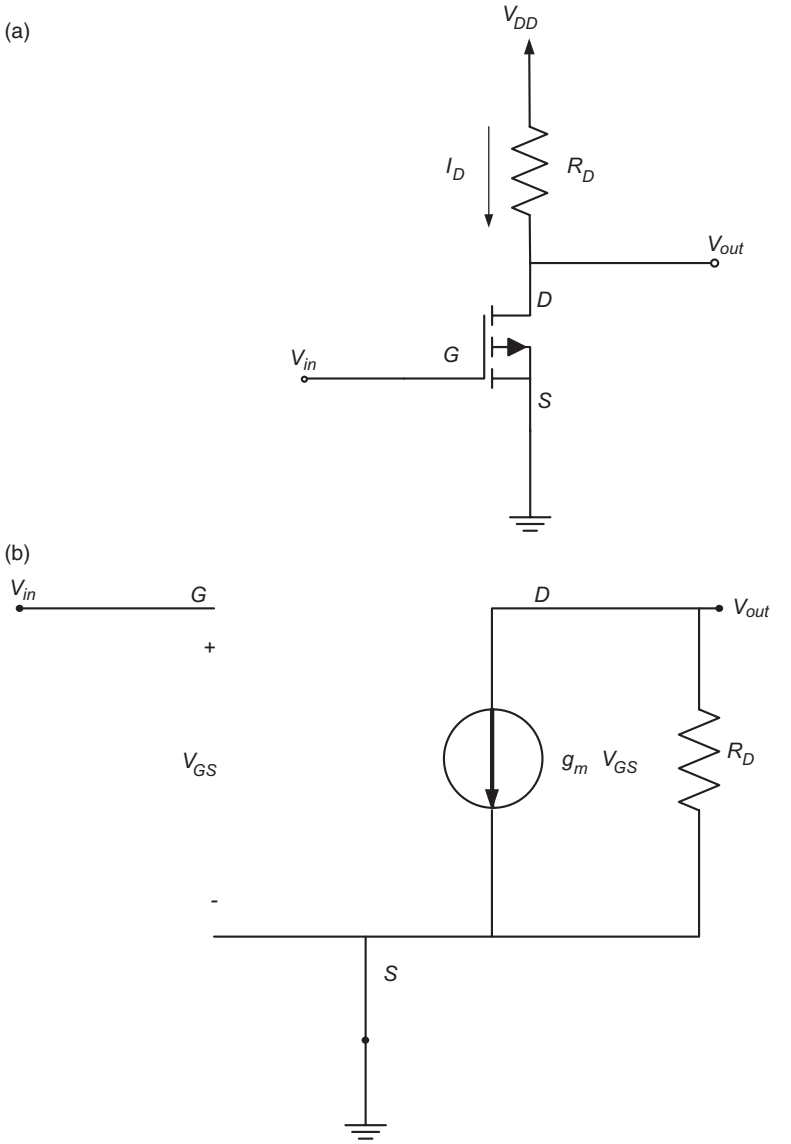

Figure 6.52 MOSFET CS amplifier: (a) MOSFET-based circuit; (b) small signal equivalent model at low and mid frequencies.

6.4.5 Common Source (CS) Configuration with Degeneration

The source terminal degeneration resistor has the same effect in the MOSFET amplifier as it does in the BJT. Figure 6.53 depicts a CS amplifier with emitter degeneration resistor.

From the circuit of Figure 6.53b we have

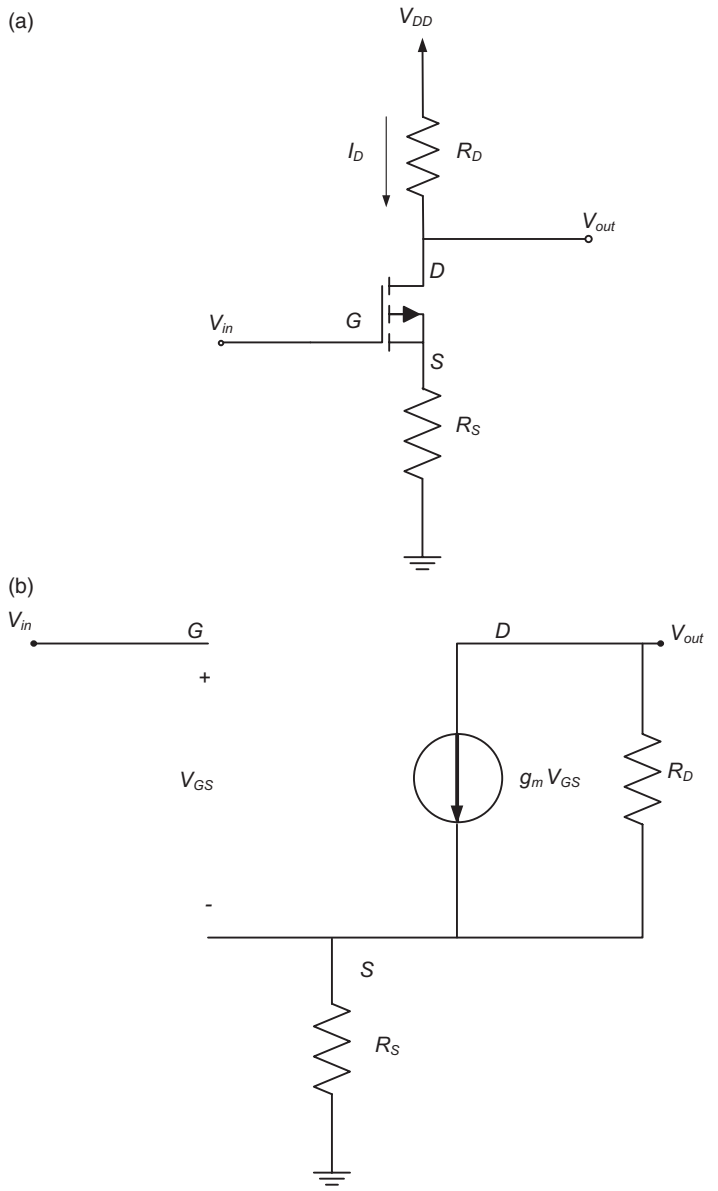

Figure 6.53 CS amplifier with source degeneration: (a) MOSFET-based circuit; (b) small signal equivalent model.

$$V_{in} = V_{GS} + g_m V_{GS} R_S \tag{6.134}$$

Thus,

$$V_{GS} = \frac{V_{in}}{1 + g_m R_S}. \tag{6.135}$$

Since current $g_m V_{GS}$ flows through resistor R_D we have that

$$V_{out} = -g_m V_{GS} R_D \tag{6.136}$$

and

$$G_{CS \text{ with source degeneration}} = \frac{V_{out}}{V_{in}} = -\frac{g_m R_D}{1 + g_m R_S} = -\frac{R_D}{\frac{1}{g_m} + R_S}. \tag{6.137}$$

The reader is encouraged to compare MOSFET Equation (6.137) with the bipolar transistor expression given by Equation (6.76).

6.4.6 Common Gate (CG) Configuration

The MOSFET CG configuration resembles the BJT CB topology. Looking at the circuit of Figure 6.54, the circuit virtually operates like the BJT-based CB. It can easily be seen that the voltage gain of the CG topology is

$$G_{v\text{-}CG} = g_m R_D \tag{6.138}$$

Note that the gain for this topology does not have an inverting sign.

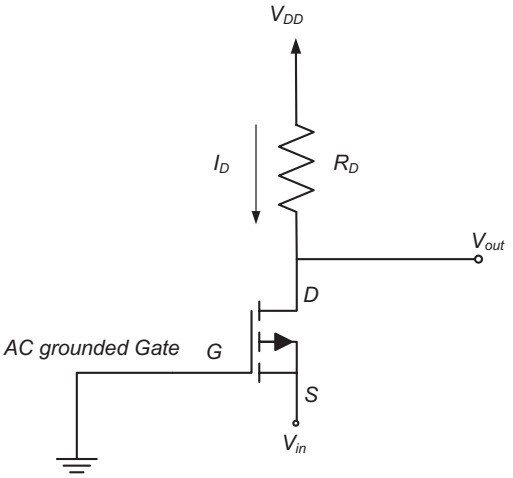

Figure 6.54 MOSFET CG topology.

Let us look at the input and output impedances of the *CG* topology. Neglecting the channel length modulation effect we come up with the small signal equivalent model and apply a voltage V_{Test} at the *source* input, the gate is AC grounded and we find R_{in} of the stage. Similarly we apply V_{Test} at the *drain* output of the stage with both the *gate* and the *source* grounded. This is virtually identical to what we did with the BJT-based CB configuration. Both circuits used to calculate R_{in} and R_{out} are shown in Figure 6.55a,b respectively.

As expected, due to the similarity with the bipolar-based CB circuit, we obtain

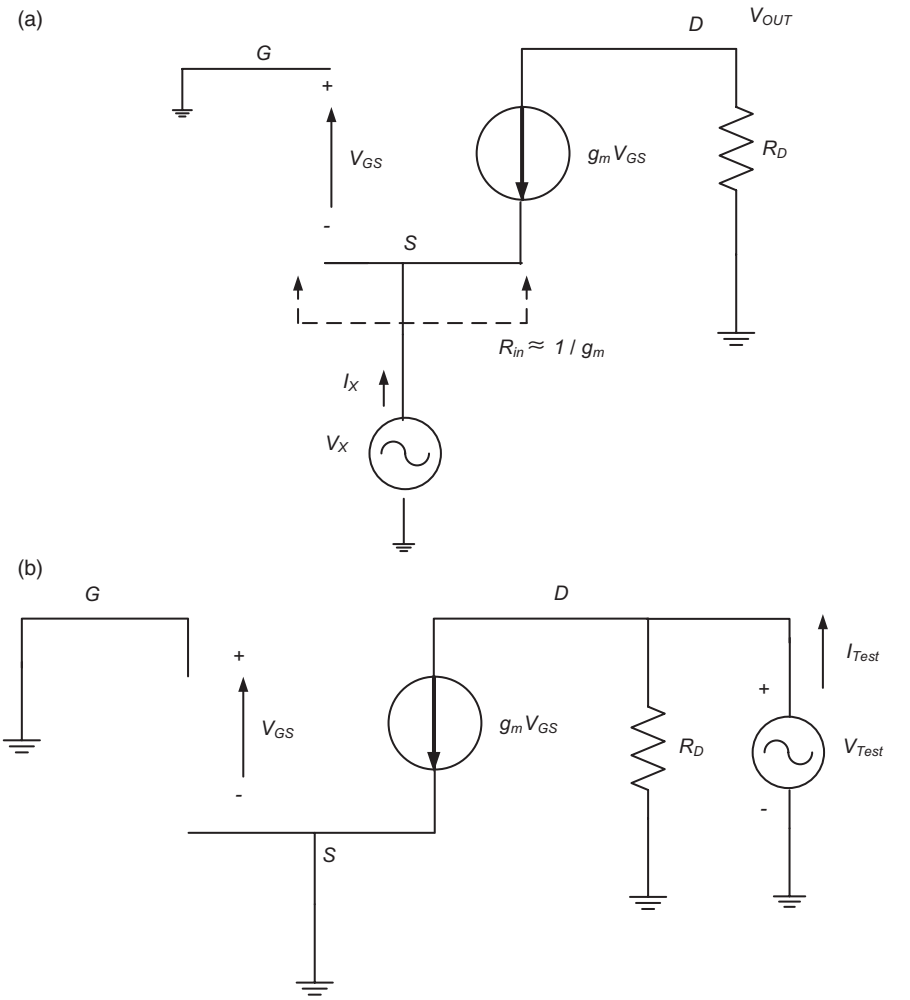

Figure 6.55 (a) CG small signal model to calculate R_{in}; (b) CG small signal model to calculate R_{out}.

$$R_{in} = \frac{1}{g_m} \tag{6.139}$$

and

$$R_{out} = R_D. \tag{6.140}$$

Moreover, when the input voltage applied at the source has a source resistance in series, the gain voltage gain stage is

$$G_{CG \text{ with source resistance}} = \frac{R_D}{\frac{1}{g_m} + R_S}. \tag{6.141}$$

6.4.7 Common Drain (CD) Configuration or Source Follower

The source follower amplifier receives the input signal at the *gate* terminal, and it senses the output signal at the *source* terminal. The *drain* is grounded for AC signals.

The voltage gain of this stage can be derived by inspection of the circuits in Figure 6.56. As expected, the voltage gain of the source follower is by similarity with the BJT follower equal to

$$\frac{V_{out}}{V_{GS}} = g_m(R_S \,//\, r_o) \tag{6.142}$$

$$V_{in} = V_{GS} + V_{out} \tag{6.143}$$

$$G_{CD} = \frac{V_{out}}{V_{in}} = \frac{g_m(R_S \,//\, r_o)}{1 + g_m(R_S \,//\, r_o)} \tag{6.144}$$

6.4.8 Other MOSFETs: Enhancement Mode *p*-Channel and Depletion Mode (*n*-Channel and *p*-Channel)

The enhancement mode *p-channel* MOSFET, also called a PMOS transistor is fabricated on an *n-type* substrate or body. Heavily doped *p*+ regions are created in the substrate to form the *drain* and the *source*. The PMOS device operates just like the NMOS, but some important differences exist. The PMOS transistor operates with negative V_{GS} and V_{DS}. The threshold voltage V_{TH} is negative. The current I_D enters the source terminal and leaves through the drain terminal. A *p-channel* is induced when

$$|V_{DS}| > |V_{GS}| - |V_{TH}| \tag{6.145}$$

The drain saturation current for the PMOS or enhancement mode *p*-channel MOSFET is

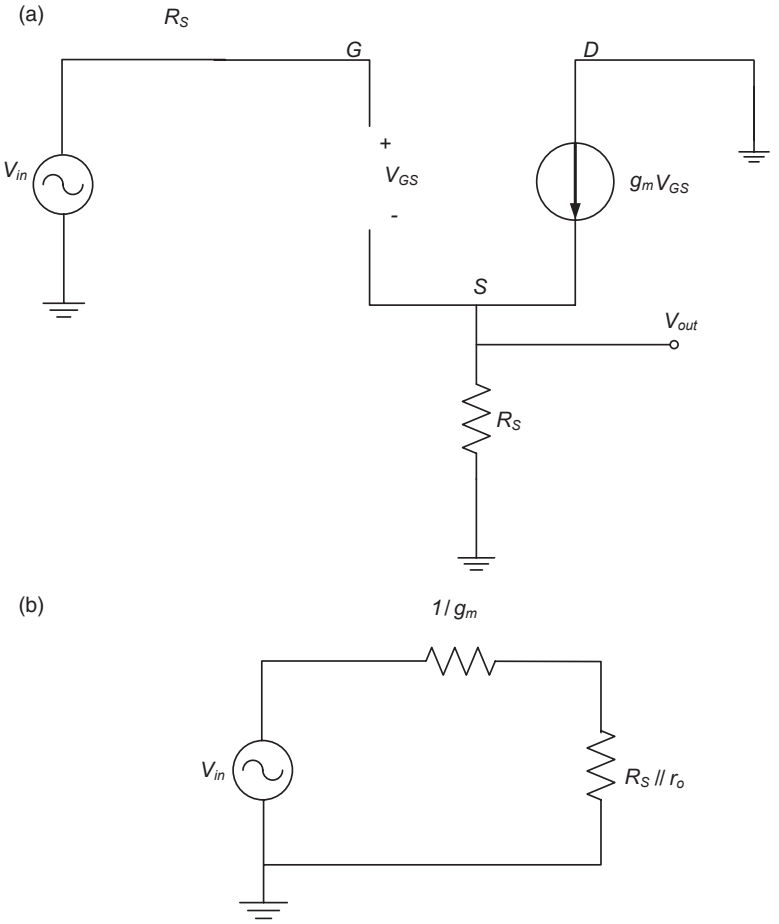

Figure 6.56 Circuits used to calculate the source follower gain and it includes the effects of channel length modulation ($\lambda > 0$).

$$I_{D,Sat} = -\frac{1}{2}\mu_p C_{ox}\frac{W}{L}[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2] \tag{6.146}$$

μ_p in Equation (6.146) is the majority carriers (holes) mobility. Equation (6.146) also assumes that the channel length modulation factor λ is zero.

Now taking into account a nonzero λ channel length coefficient, the PMOS transistor drain current becomes

$$I_{D,Sat} = -\frac{1}{2}\mu_p C_{ox}\frac{W}{L}[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2](1 + \lambda V_{DS}) \tag{6.147}$$

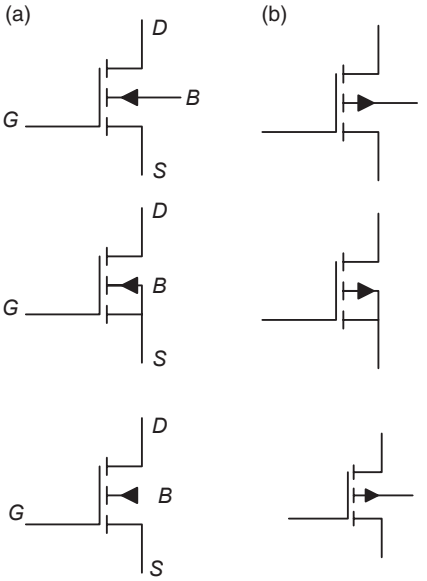

Figure 6.57 Enhancement mode MOSFET symbols: (a) *n-channel*; (b) *p-channel*.

Similarly to the NMOS transistor, the PMOS transistor has a triode region current:

$$I_{D,triode} = -\frac{1}{2}\mu_p C_{ox}\frac{W}{L}[2(V_{GS} - V_{TH})V_{DS} - V_{DS}^2] \tag{6.148}$$

The *p-channel* MOSFET has holes as charge carriers. Remember that the *n-channel* MOSFET has electrons as charge carriers. Symbols for all four MOSFET types listed in Table 6.4 are shown in Figures 6.57 and 6.58. Different authors use slightly different schematic symbols. Figures 6.57 and 6.58 address some of the most common symbols used.

Note in Figure 6.59 the equation for the saturation *drain* current as a function of V_{GS} is also quadratic like the $I_D - V_{GS}$ curve for the NMOS transistor, but it is rotated 180° around the current axis; refer to Figure 6.57b. The reason is that PMOS transistors have negative V_{TH} and negative V_{GS}. Strictly speaking, the current drawn should be negative, but for simplicity of the graphic representation it is not; that is, I_D is drawn as a positive current as it is most commonly done in the MOSFET literature.

All equations for NMOS transistors are applicable to PMOS transistors provided that the *electron mobility* (μ_n) used for *n-channel* devices is replaced with the *hole mobility* (μ_p) for *p-channel* devices. Additionally and hopefully to reduce confusion between positive and negative voltages, one can simply

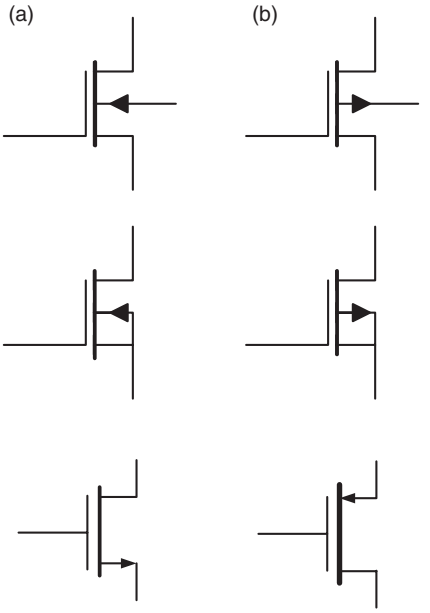

Figure 6.58 Depletion mode MOSFET symbols: (a) *n-channel*; (b) *p-channel*.

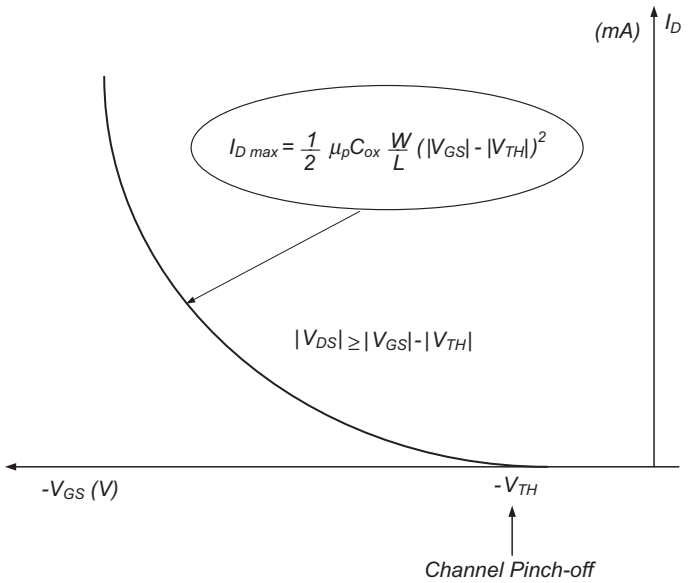

Figure 6.59 Depicts the I_D-V_{GS} transfer curve characteristic of the PMOS transistor.

take the absolute values of voltages V_{DS}, V_{GS}, and V_{TH}, so that the equations basically look the same. The reader is encouraged to rewrite the *n-channel* enhancement mode equations for I_D in both the triode and the saturation regions for the *p-channel* enhancement mode device. In integrated circuits NMOS and PMOS transistors are used, such technology is referred to as Complementary MOS technology (CMOS). CMOS is the most prevalent technology of integrated circuits at the time of this writing. Unfortunately, CMOS technology is well beyond the scope of this book.

Table 6.6 summarizes NMOS and PMOS transistors characteristics.

6.4.8.1 Depletion Type MOSFETs For the sake of completeness we address depletion type MOSFETs; however, they are not as commonly used as enhancement-type devices are. The fundamental difference between the enhancement and the depletion device is that the depletion device does not need a *gate* voltage to induce a channel. Depletion type devices have a *physically implanted channel*. So, for example, when dealing with an *n-channel* depletion device, it just takes a positive V_{DS} voltage to be applied with $V_{GS} = 0$, and the device will conduct current through the implanted channel. Again the channel is not induced like it is for the enhancement-type device. Figure 6.60 depicts the I_D versus V_{GS} transfer characteristic for an *n-channel* depletion device and for an *n-channel* enhancement device. In order not to overlap both curves, the absolute values of the threshold voltages are assumed to be different.

Figure 6.61 depicts the I_D versus V_{GS} transfer characteristic for a *p-channel* depletion device and for a *p-channel* enhancement device.

6.5 SUMMARY

This chapter is quite long and covers key electronic devices from the bottom up. It has been the intent of the author not to cover a great deal of semiconductor physics, but just enough of it to understand circuit-level operation of diodes, bipolar, and MOS transistors. Some of the most important applications with diodes were covered. Biasing and the most common amplifiers configurations were addressed with bipolar and MOS transistors. Because of the similarities of some bipolar and MOSFET-based amplifiers, the MOSFET material heavily relies on having done circuit equations and derivations with the bipolar junction transistor examples. The junction field effect transistor or JFET was not covered because of space reasons. The JFET was a predecessor of the MOSFET. MOSFETs are more heavily used than any other transistor, including bipolars. NMOS and PMOS transistors are used in CMOS technology, the dominating IC technology at this time.

Table 6.6 NMOS and PMOS transistors characteristic

Enhancement Mode *n*-channel (NMOS) characteristics		
1	Drain current for the triode region (no channel length modulation)	$I_{D,\text{triode}} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}[2(V_{GS}-V_{TH})V_{DS}-V_{DS}^2]$
2	Drain current for the triode region for $V_{DS} <<< 2$ $(V_{GS} - V_{TH})$ (no channel length modulation)	$I_{D,\text{triode}} \approx \mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})V_{DS}$
3	Drain current at the beginning of the saturation region for: $V_{DS} = V_{GS} - V_{TH}$	$I_{D,\text{Max}} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2$
4	Drain current in the saturation region including channel length modulation.	$I_{D,\text{Sat}} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1+\lambda \mathrm{V_{DS}})$
5	R_{DSon} For $V_{DS} << 2\ (V_{GS} - V_{TH})$	$R_{DSon} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS}-V_{TH})}$ (see *a*)
6	Turn-on and turn-off conditions	If: $V_{GS} < V_{TH}$, then $I_D = 0$ regardless of the value of V_{DS}
		If: $V_{GS} > V_{TH}$, then $I_D > 0$
	Threshold voltage V_{TH} (is a positive quantity for NMOS)	
7	Transconductance g_m	$g_m = \mu_n \mathrm{C_{ox}}\frac{W}{L}(V_{GS}-V_{TH}) = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D}$
Enhancement Mode *p*-channel (PMOS) characteristics		
1	Drain current for the triode region (no channel length modulation)	$\mathrm{I}_{D,\text{triode}} = -\frac{1}{2}\mu_p C_{ox}\frac{W}{L}[2(V_{GS}-V_{TH})V_{DS}-V_{DS}^2]$
2	Drain current for the triode region for $V_{DS} <<< 2$ ($V_{GS} - V_{TH}$) (no channel length modulation)	$I_{D,\text{triode}} \approx -\mu_p C_{ox}\frac{W}{L}(V_{GS}-V_{TH})V_{DS}$
3	Drain current at the beginning of the saturation region for: $V_{DS} = V_{GS} - V_{TH}$	$I_{D,\text{Max}} = -\frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2$
4	Drain current including channel length modulation)	$I_{D,\text{Sat}} = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{GS}-V_{TH})^2(1-\lambda V_{DS})$
5	r_{DSon} For $V_{DS} << 2\ (V_{GS} - V_{TH})$	$r_{Dson} = \frac{1}{\mu_p C_{ox}\frac{W}{L}(V_{GS}-V_{TH})}$ (see *a*)
6	Turn-on and turn-off conditions	If $V_{GS} < V_{TH}$, $I_D = 0$ regardless of the value of V_{DS}
	Threshold voltage V_{TH} (is a negative quantity for PMOS)	Turn on condition: $V_{GS} > V_{TH}$, $I_D < 0$
7	Trans-conductance g_m	$g_m = \mu_p \mathrm{C_{ox}}\frac{W}{L}(V_{GS}-V_{TH}) = \sqrt{2\mu_p C_{ox}\frac{W}{L}I_D}$

[a] Note that since electron mobility is larger than hole mobility, for a given oxide thickness C_{ox} and aspect ratio W/L an *n*-channel (NMOS) r_{DSon} is smaller than a *p*-channel (PMOS) r_{DSon}, under the same voltage conditions.

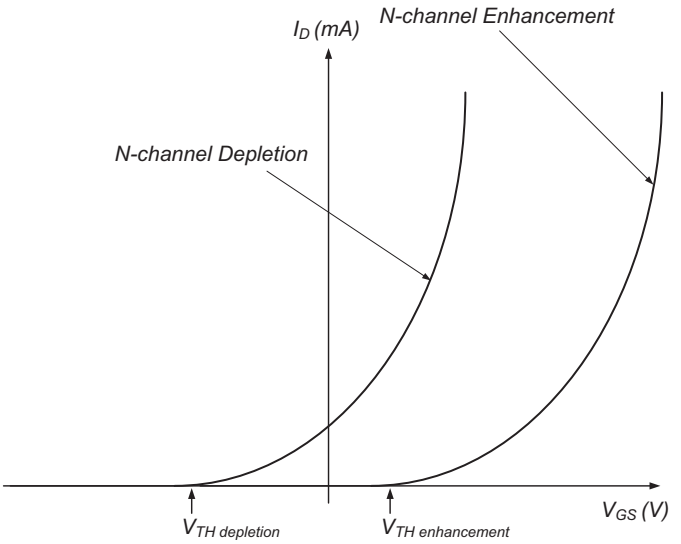

Figure 6.60 *n-Channel* depletion and enhancement MOS transistors operating in saturation.

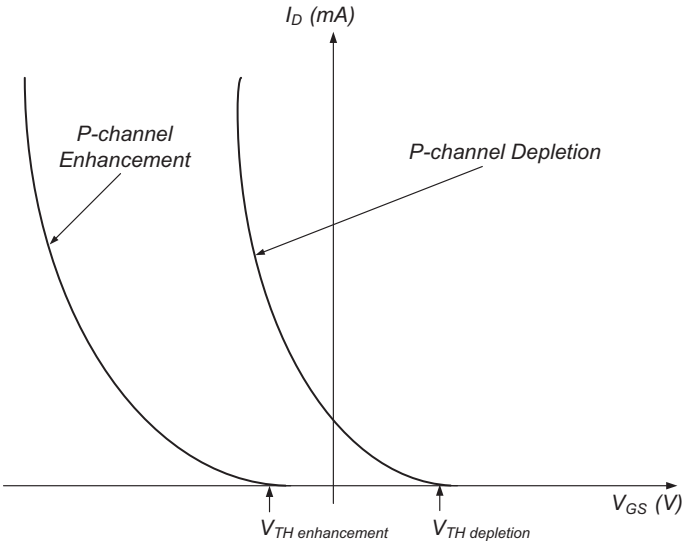

Figure 6.61 *p-Channel* depletion and enhancement MOS transistors operating in saturation.

FURTHER READING

1. Robert F. Pierret, *Semiconductor Fundamentals*, Addison-Wesley Publishing Company, Reading, MA, 1983.
2. T. E. Price, *Introduction to VLSI Technology*, Prentice Hall International (UK) Ltd, Reading, MA, 1994.
3. Behzad Razavi, *Fundamentals of Microelectronics*, John Wiley & Sons, Inc., Hoboken, NJ, 2008.
4. Adel S. Sedra and Kenneth C. Smith, *Microelectronic Circuits*, 5th ed., Oxford University Press, New York, 2007.
5. Jacob Millman and Christos C. *Halkias, Electronic Devices and Circuits*, McGraw Hill, Tokyo, 1967.

PROBLEMS

6.1 The circuit of Figure 6.62 find the following voltages and currents: (a) I_1, (b) I_2, (c) I_{D1}, (d) I_3, (e) I_{D2}, (f) V_{R1}, (g) V_{R2}, (h) V_{R3}. Assume the diode $D1$ forward voltage drop is 0.61 V and $D2$'s forward drop is 0.53 V.

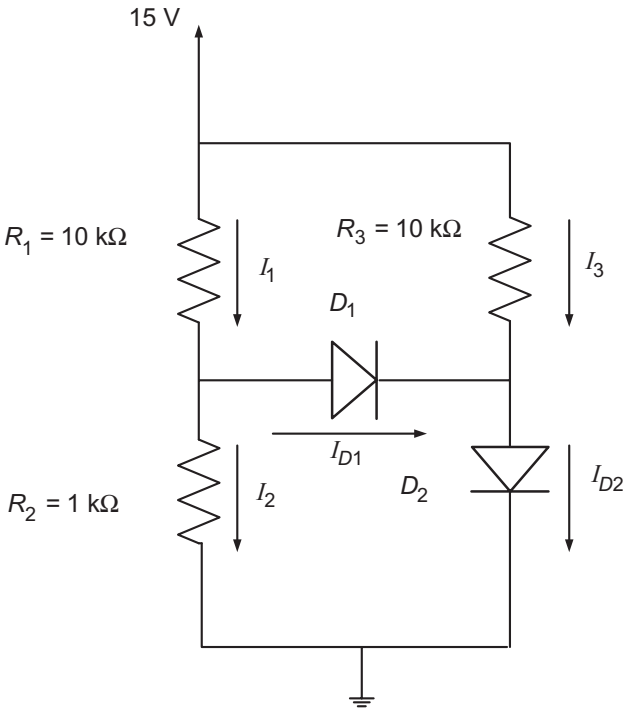

Figure 6.62 Circuit for Problem 6.1.

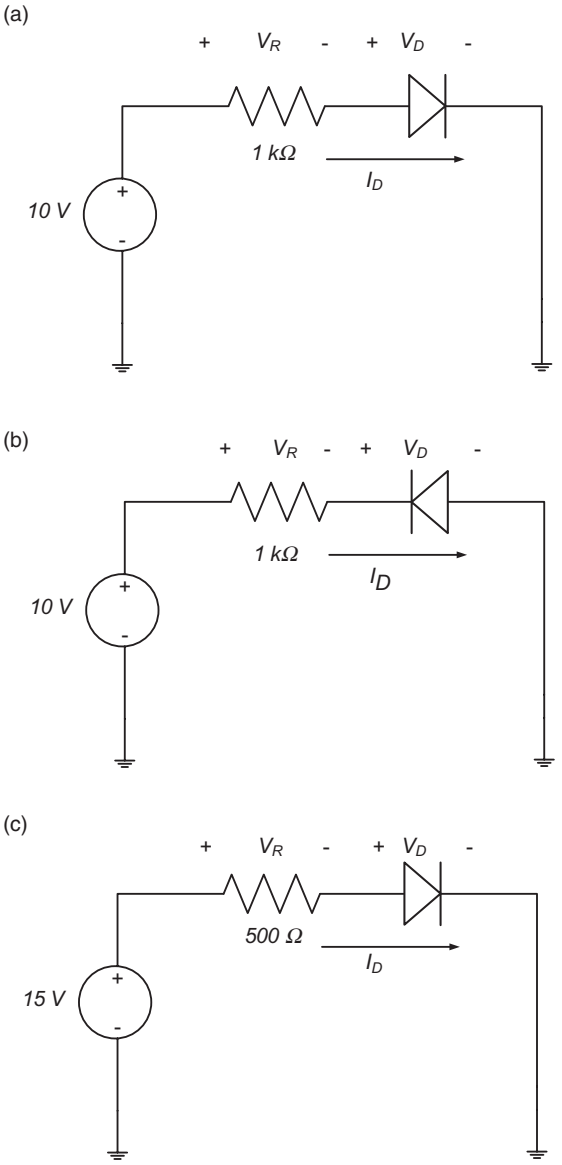

Figure 6.63 Circuits for Problem 6.2.

6.2 Given the circuits of Figure 6.63, assuming all diodes are ideal, determine the voltages V_D, V_R, and currents I_D indicated for circuits (a), (b), and (c).

6.3 For the circuit of Figure 6.64, the square wave V_g is applied to circuit as shown. Assuming that the diodes and op amp are real devices, draw the following waveforms: (a) V_g, (b) I_R, (c) I_{D1}, (d) I_{D2}, (e) V_{in}, and *(f)* V_{out}. Hint: Assume the diode forward drop is 0.6 V and the op amp saturates at ±13 V.

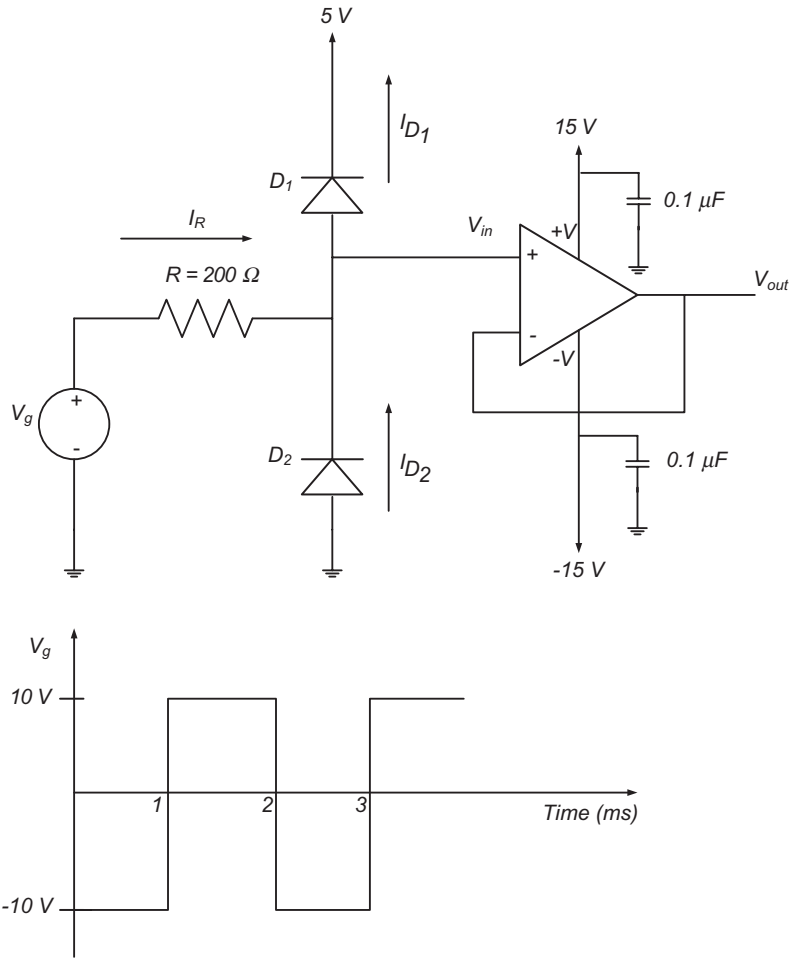

Figure 6.64 Circuits for Problem 6.3.

6.4 For the circuit of Figure 6.65, draw the following waveforms: (a) V_{sig}, (b) I_R, (c) I_{D1}, (d) I_{D2}, (e) V_{in}, and (f) V_{out}. Assume that the op amp is ideal and assume that the diodes forward voltage drop is 600 mV.

6.5 Assume that you have a 2N3904 NPN transistor. Using a biasing circuit topology such as the one presented in Figure 6.26, assume your V_{CC} supply is 10 V. Find the resistor values for R_B and R_C to bias the transistor with a collector current of 10 mA and a V_{CE} of 5 V at a 25°C ambient temperature. Assuming that the resistors have a zero ppm/°C temperature coefficient, and that the 10 V supply does not change due to temperature variations, find: (a) V_{CE} and I_C at –55°C, and (b) V_{CE} and I_C at 123°C. Hint: β, the DC current gain is given as by h_{FE} on the

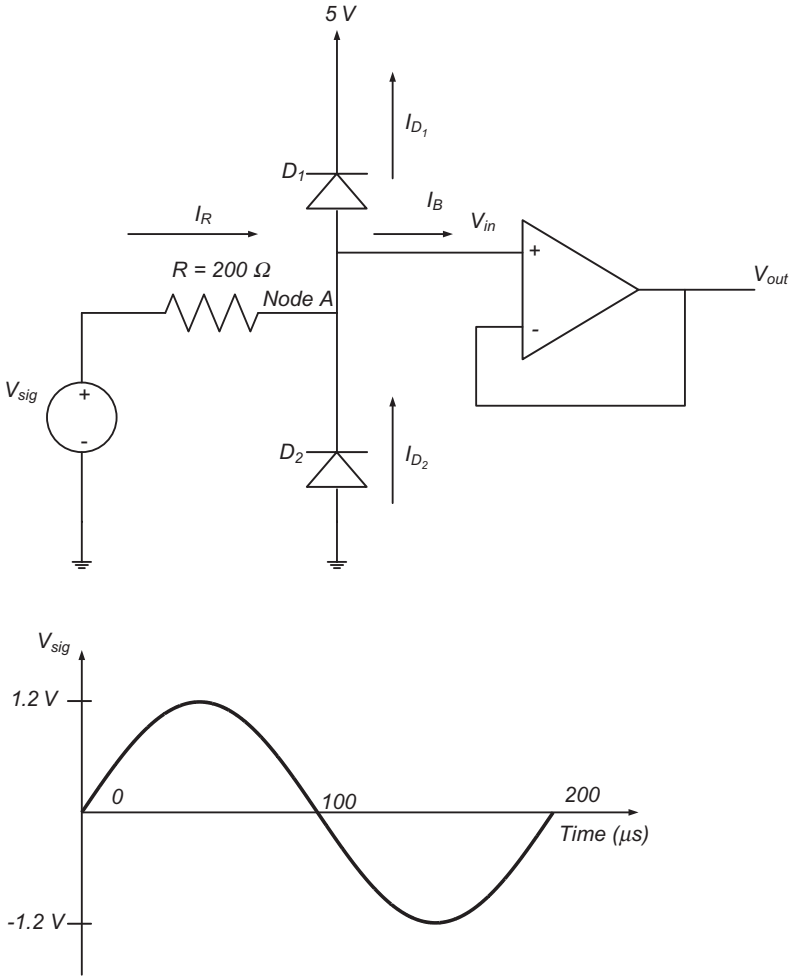

Figure 6.65 Circuits for Problem 6.4.

datasheet. Search for National's, or Fairchild's 2N3904 datasheet to find h_{FE}.

6.6 Assume that you have a 2N3904 NPN transistor. Using a biasing circuit topology such as the one presented in Figure 6.26, assume your V_{CC} supply is 10 V. Find the resistor values for R_B and R_C to bias the transistor with a collector current of 10 mA and a V_{CE} of 5 V at a 25°C ambient temperature. Assuming that the resistors have a 200 ppm/°C temperature coefficient, and that the 10 V supply does not change due to temperature variations, find: (a) V_{CE} and I_C at –55°C, and (b) V_{CE} and I_C at 123°C. Hint: β, the DC current gain is given as h_{FE} on a Fairchild

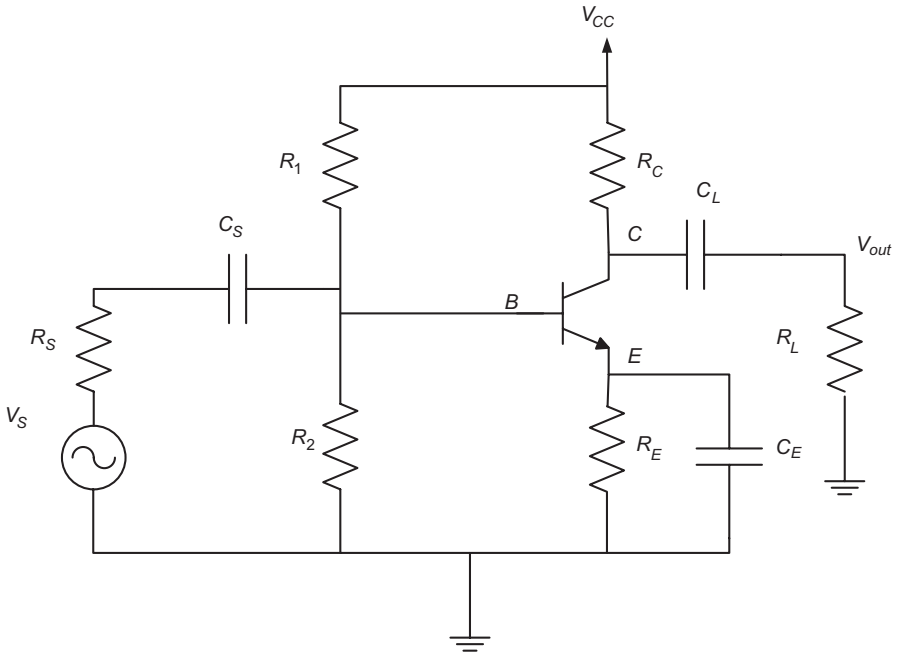

Figure 6.66 Circuit for Problems 6.8, 6.9, 6.10 and 6.11.

Semiconductors bipolar transistor datasheet. Practically speaking β, the DC current gain and h_{FE}, an H-model parameter, are interchangeable.

6.7 Repeat Problem 6.6 using the circuit biasing topology of Figure 6.23.

6.8 Using the circuit topology of Figure 6.66, assume the following values: $V_{CC} = 15$ V, $V_S = 1$ m V peak sine-wave, with 0 DC offset, and 1 kHz frequency, $R_1 = 140$ kΩ, $R_2 = 140$ kΩ, $R_C = 100$ Ω, $R_E = 50$ Ω, $C_S = 10$ μF, $C_L = 10$ μF, and $R_L = 8$ Ω. Assume a transistor $\beta = 300$ and $V_{BE} = 0.74$ V; determine: (a) the transistor operating point Q, that is, V_{CE}, I_B, I_C, and I_E, and (b) the small signal voltage gain of the amplifier circuit.

6.9 Using the circuit of Figure 6.66 calculate the amplifier input impedance. Refer to Figure 6.66.

6.10 Using the circuit of Figure 6.66 calculate the amplifier output impedance.

6.11 Using the circuit of Figure 6.66, establish all the effects that short circuiting the R_E and C_E parallel combination has on: (a) the biasing point of the transistor, (b) the small signal gain of the amplifier. Hint: for part (a) determine the new values of V_{CE}, I_B, I_C, and I_E.

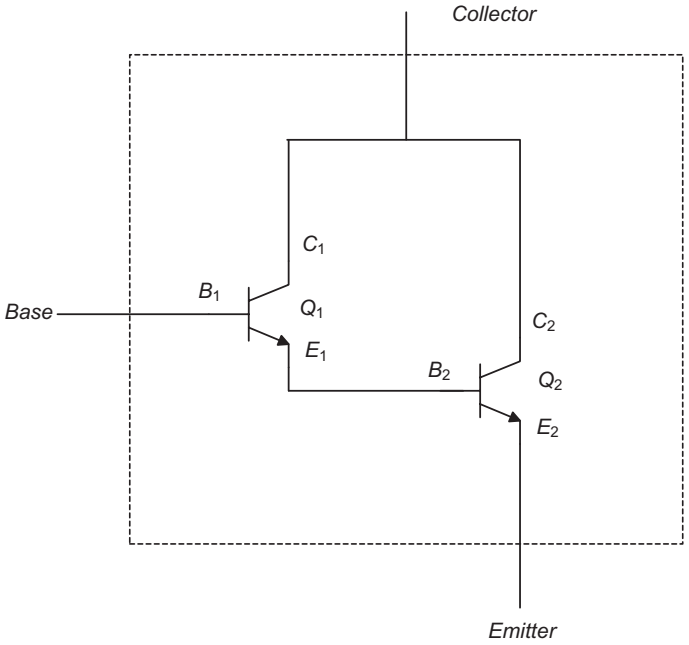

Figure 6.67 Circuit for Problems 6.12 and 6.13.

6.12 The two-transistor circuit depicted by Figure 6.67 is called a Darlington pair configuration. (a) Knowing that the DC current gains for Q_1 and Q_2 are respectively β_1 and β_2 determine the overall DC current gain of the Darlington pair. (b) Determine the Darlington pair base-emitter voltage drop when the pair is in the active region.

6.13 Derive an equivalent Darlington pair configuration using two PNP bipolar transistors. Refer to Figure 6.67.

6.14 The circuit depicted by Figure 6.68 can be used to drive an LED. Let us assume that the base will be driven with a square wave that switches between 0 V and 5 V. Knowing that the LED reaches maximum brightness for 10 mA, determine: (a) the value of resistor $R_{LED,}$ and (b) a reasonable value for resistor R_{BASE}.

Assume that you are asked to use a 2N3904 NPN transistor.

6.15 For the circuit of Figure 6.69, assume $R_1 = R_2 = 550$ kΩ, $R_D = R_S = 4$ kΩ, $V_{DD} = 12$ V. (a) Calculate the drain current I_D and (b) determine in which region the MOSFET operates in. Hint: assume the MOSFET is in saturation and validate this condition, else assume the MOSFET is in its triode region and validate its operation. (c) if the value of resistor R_2 is changed to 0 Ω, determine without using any equations, the operating

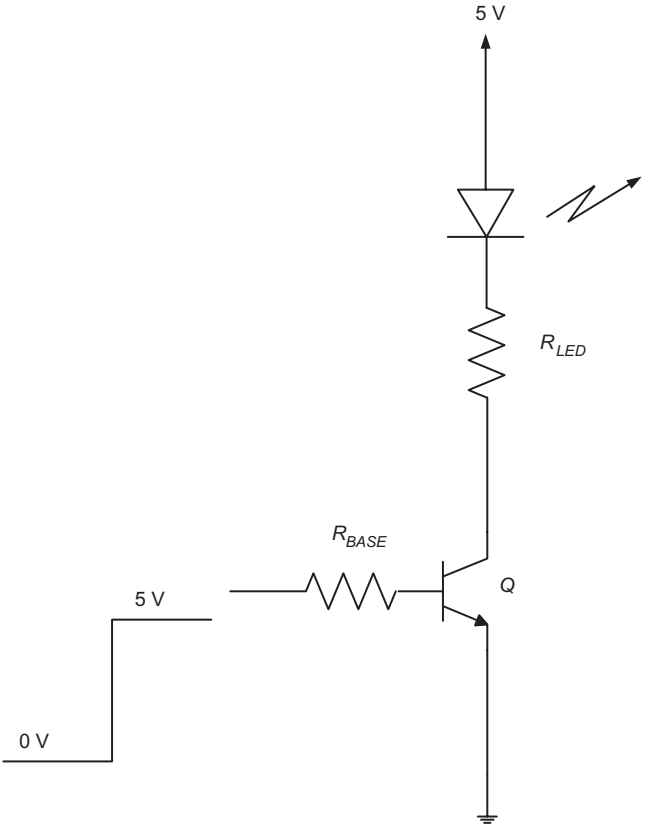

Figure 6.68 Circuit for Problem 6.14.

region of the MOSFET. Assume the MOSFET has $V_{TH} = 2$ V, $\mu_n C_{ox} = 100\ \mu A/V^2$, $W/L = 50$ and $\lambda = 0$.

6.16 For the circuit of Figure 6.70, calculate the appropriate values for R_D and R_S to keep the transistor *at* $I_D = 1$ mA and $V_D = 2$ V. Assume the following MOSFET parameter:

$$V_{TH} = 2 \text{ V}.$$

6.17 For the circuit of Problem 6.16 determine the DC gate current.

6.18 For the MOSFETs of Figure 6.71 determine the transistor region of operation. Assume that: $V_{TH} = 1.5$ V.

6.19 For the MOSFETs of Figure 6.72 determine the transistor region of operation. Assume that: (a) $\mu_p C_{ox}(W/L) = 100\ \mu A/V^2$, (b) $V_{TH} = -0.4$ V, and (c) $\lambda = 0$.

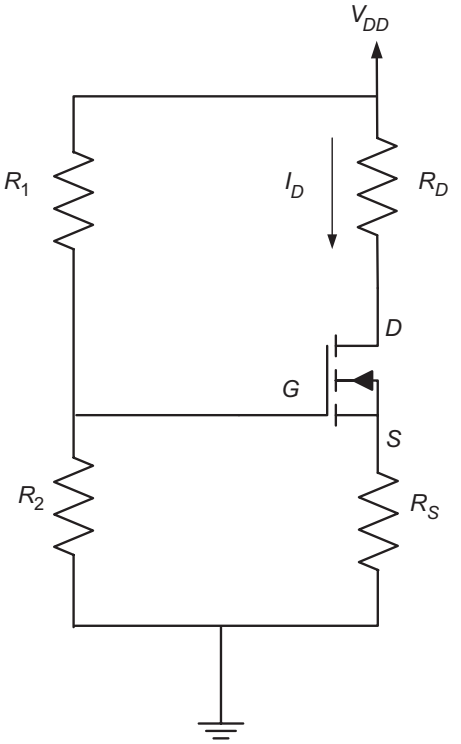

Figure 6.69 Circuit for Problem 6.15.

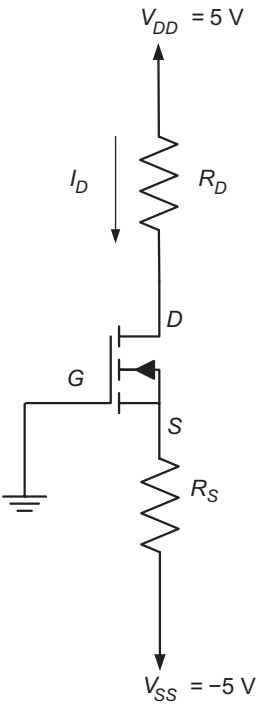

Figure 6.70 Circuit for Problem 6.16.

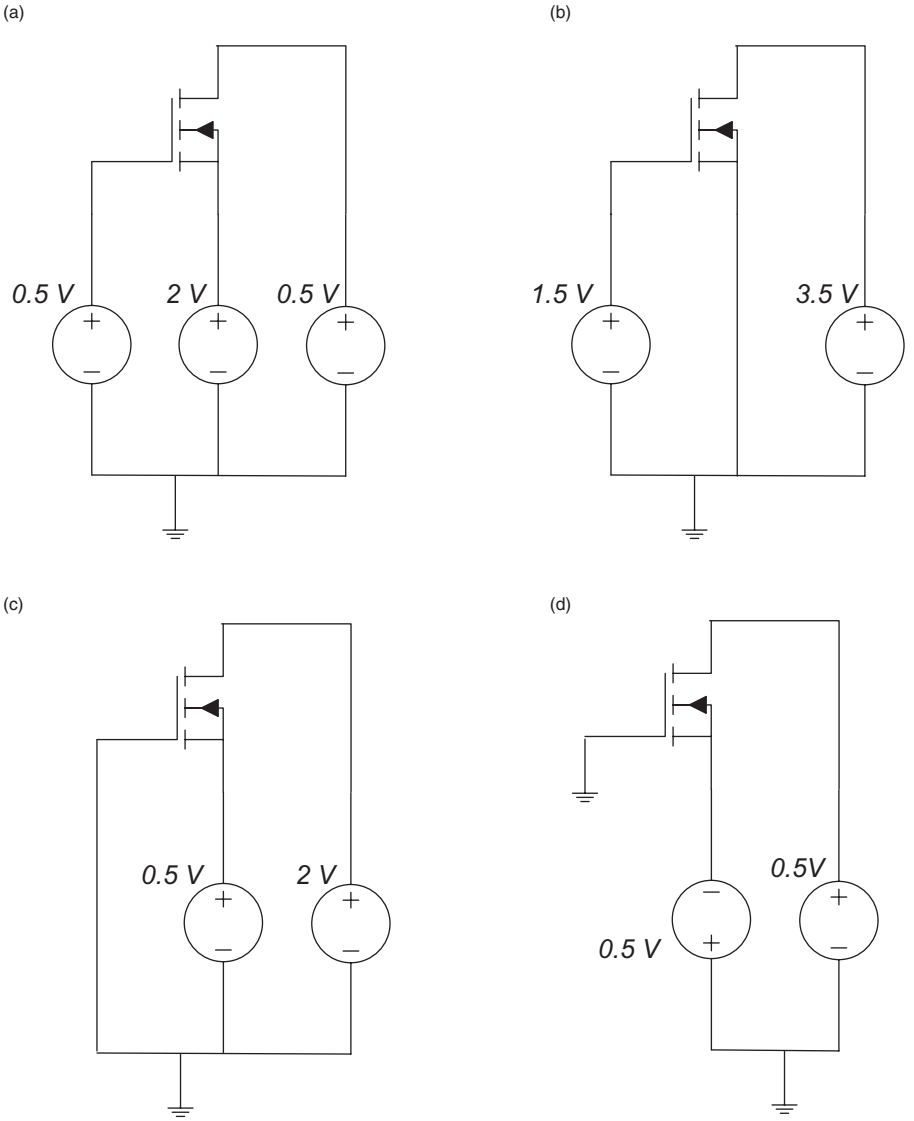

Figure 6.71 Circuits for Problem 6.18.

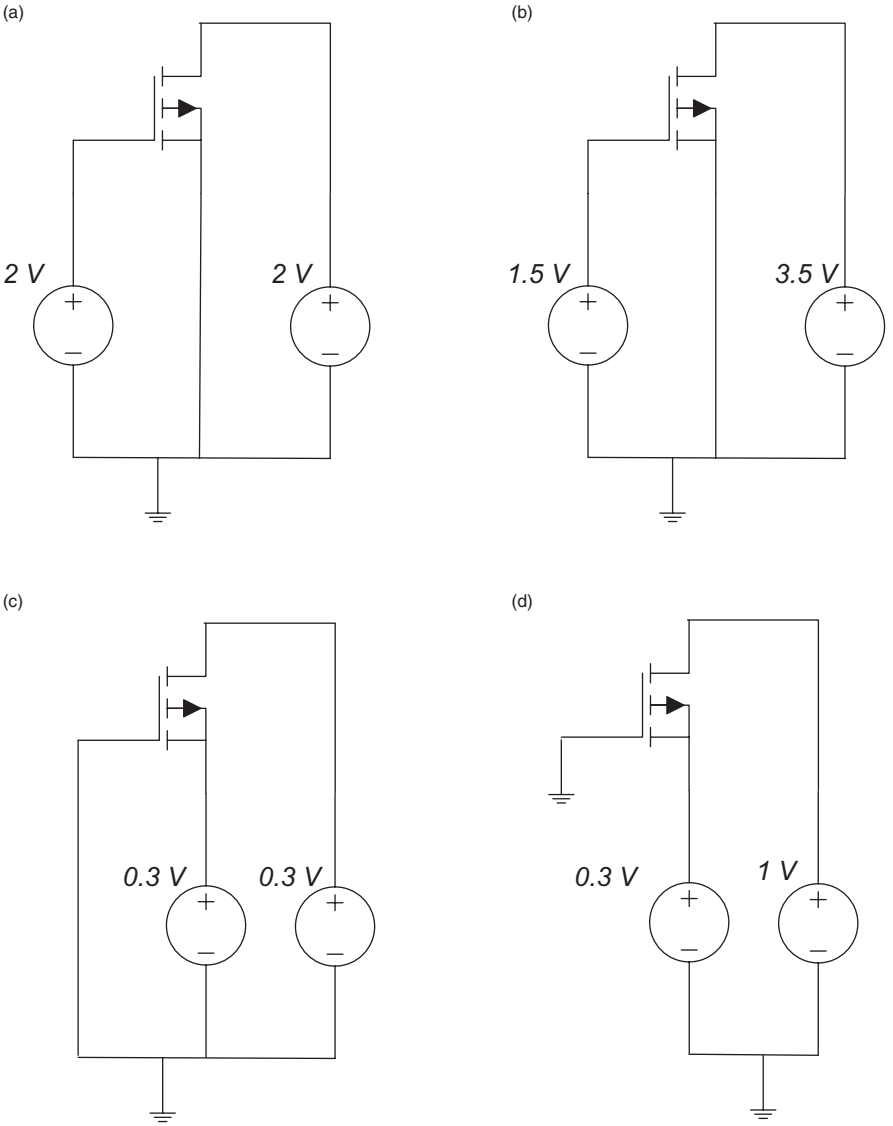

Figure 6.72 Circuits for Problem 6.19.