# 8
# Semiconductor Templates for the Fabrication of Nano-Objects

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## 8.1
## Introduction

Owing to the continuing miniaturization in nanotechnology applications requested by the semiconductor roadmap, important works are undertaken to develop novel and complementary ways of creating semiconductor templates allowing the growth of objects on the nanometer scale. Basically, two conceptually different approaches have so far emerged as fabrication methods. Both can achieve reproducible and well-controlled fabrication of arrays consisting of well-defined nanostructures on various semiconducting substrates. The first approach is called *top-down* or *descending* and the second one, which is more recent, is called *bottom-up* or *ascending*. *Top-down* nanofabrication techniques were inherited from microelectronic development through lithography and etching to meet the expectations related to the constant miniaturization of optoelectronic devices. *Bottom-up* methods allow nanofabrication and nanopatterning through the spontaneous reorganization of the substrate atoms induced by the intrinsic properties of the material. Subsequent controlled deposition of atoms and molecules then leads to the formation of self-organized assemblies of various materials. The third approach combines these two methods by adding a pattern of artificial perturbations, such as holes or stressors, via a top-down process onto a substrate with defined intrinsic properties.

In this chapter, some basic ideas concerning the growth of highly ordered arrays of well-defined and identical nano-objects on a substrate with extended dimensions will be described. Growth can be controlled by choosing the respective adsorbate and substrate materials and strain can be used to drive the adsorption of the deposited atoms or molecules at specific sites. Some of the most frequently used semiconductor templates and several deposited systems and architectures will be presented in this chapter.

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## 8.2
## Semiconductor Template Fabrication

Many strategies have been developed to pattern semiconductor surfaces for their uses in nanosciences [1, 2]. Emphasis will be placed in this section on techniques that use mechanical strain, specifically for nanostructuring surfaces. The usual morphological patterning that may induce local strain will be first briefly reminded. Then, we will point out elastic stress engineering using buried stressors either on flat surface or through lithography followed by etching. Finally, the use of intrinsic properties of the surface such as surface reconstructions and step edges on vicinal surfaces will be stressed. The combination of both approaches, artificial and natural patterning, can be also employed, but will not be presented in this section for the sake of simplicity.

### 8.2.1
### Artificially Prepatterned Substrates

#### 8.2.1.1 Morphological Patterning

Etching techniques are commonly used to transfer the hole patterns of a mask into the surface of the sample with individual dimensions that may be less than 50 nm. Three etching methods are commonly employed in the laboratories and the microelectronics industry (Figure 8.1): physical etching, chemical etching, and reactive ion etching (RIE). Physical etching consists of bombarding the sample with high-energy ions (few keV). This method may produce anisotropic patterns due to the particle momentum transfer and the mask may suffer from some damages. Chemical etching is performed by immersing the sample in a chemically active bath. This method can be isotropic, highly chemically selective, and sometimes strain sensitive. Finally, RIE tries to combine the advantages of the last methods by using chemically reactive plasmas to obtain highly selective and anisotropic etching. The plasma, fitted to the materials under study (e.g., fluorine and chlorine based for Si and GaAs,

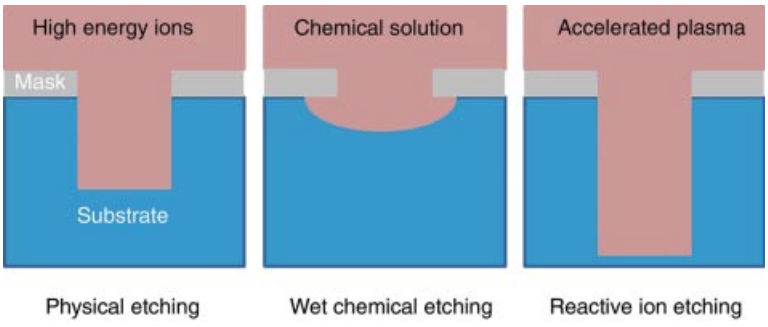


**Figure 8.1** Schematic illustration of the three etching methods using masks commonly employed in laboratories and microelectronics industry.

respectively), is generated by an electromagnetic field under low pressure. High-energy ions bombard the sample surface and react with the material.

Nanoimprint lithography is used to transfer nanometer-scale patterns with molds on resists. This technique is already included in the international technology roadmap for semiconductor for the 22 nm node.

It is also possible to apply maskless lithography techniques such as e-beam and interferometric and holographic lithography [3]. Interference lithography is a laboratory-scale patterning technique that uses the interference of coherent laser beams to write patterns over large areas. This technique can produce patterns with feature dimensions approaching 20 nm, but is limited to performing periodic patterns with micron to submicron periodicities only.

Pit- or groove-patterned semiconductor substrates are commonly used to grow ordered arrays of islands. Such topographic templates allow uniform shape, size, and periodicity control of the grown islands. The investigation of growth kinetics and postgrowth treatments is important and optimized annealing and etching can enable the tailoring of the island properties. The evolution of the morphology, chemical composition, homogeneity, size uniformity, and coarsening can thus be tuned. On nominally flat substrates, the nucleation of strained islands is mainly governed by the competition between surface energy and strain energy [2, 4, 5]. On a lithographically engineered, patterned surface, nucleation will be governed by the local surface curvature and local strains. The nucleation mechanisms will thus be modified compared to those on a flat surface [6].

#### 8.2.1.2 Silicon Etched Stripes: Example of the Use of Strain to Control Nanostructure Formation and Physical Properties

The advancement of silicon integrated circuits pushes lithography technology to the limits for making devices with smaller length scales. In the *top-down* approach, strain has been widely used to improve the carrier transport and the drive current of field effect transistor devices [7]. One solution among others consists of etching biaxially strained silicon on insulator layers obtained by wafer bonding [8]. For the stripe geometry (i.e., wires having a strain imposed by interfacial boundary conditions), the elastic relaxation with respect to the initial state depends not only on the width and thickness, which are now very thin in aggressive technologies (20 and 10 nm, respectively), but also on the technological steps necessary to integrate these active materials inside the transistor stacking (source–drain–gate materials). The measurement of the buried active layers (here strained silicon) has been performed to improve the physical understanding of the strain that drives the enhancement of the transport properties [9].

#### 8.2.1.3 Use of Buried Stressors

A localized strain on the surface can be provided by the propagation of buried strain fields that may result from specific nanostructure growth, for example, quantum dots (as explained later) or localized implantations [2]. It has also been proposed to control the lateral ordering of nanostructures at the wafer scale to use periodic dislocation networks obtained by wafer bonding [10]. Grain boundaries and dislocation networks

were known a long time ago in wafer bonding (see, for example, the early works dedicated to Au or Si), but recent improvements stand in the localization of the grain boundaries near the surface and in the control of their periodicity to tune finely the elastic fields [11, 12]. Network periodicity is controlled by the disorientation angle between the substrate and the bonded film, and the distance between the stressors and the surface adjusts the magnitude of the surface stress. This array is formed artificially by the dislocations appearing at the interface of two clean crystals bonded with a crystallographic disorientation. In general, the dislocation networks have to accommodate the lattice mismatch, the flexion and rotation angles of the two crystals. They also depend on the surface symmetry and on the interactions that may occur between different networks: for example, a high temperature annealing minimizes the total energy of interacting dislocations by changing the line arrangement [13]. For the hydrophobic bonding (without oxide layer) of identical silicon crystals, the interfacial structure has been studied by transmission electron microscopy (TEM) to determine the nature of dislocations and their interactions. For two (001) surfaces, twisted by 0.4° and having a negligible tilt, Figure 8.2a shows a square network of dissociated screw dislocations localized at the bonded interface. The dislocation network periodicity $\Lambda$ is related to the twist angle $\alpha$ and Burgers' vector modulus $b = a/2\langle 110\rangle$ by Frank's relation $\Lambda = b/[2\sin(\alpha/2)]$. A triangular network is obtained for the bonding of two Si(111) surfaces within similar conditions (see Figure 8.2c) [13]. The strain field of slightly buried dislocation networks is used to drive the nucleation of Ge dots on a nearly flat surface [14]. Another more efficient way to induce the positioning of semiconductors [11, 15] and metals [13] islands consists in transferring the symmetry of the dislocation lines to the surface by suitable wet etching [13]. In this case, significant trench depths are obtained (see the STM profiles in Figure 8.2b and d) and the positioning is also controlled by the local curvature.

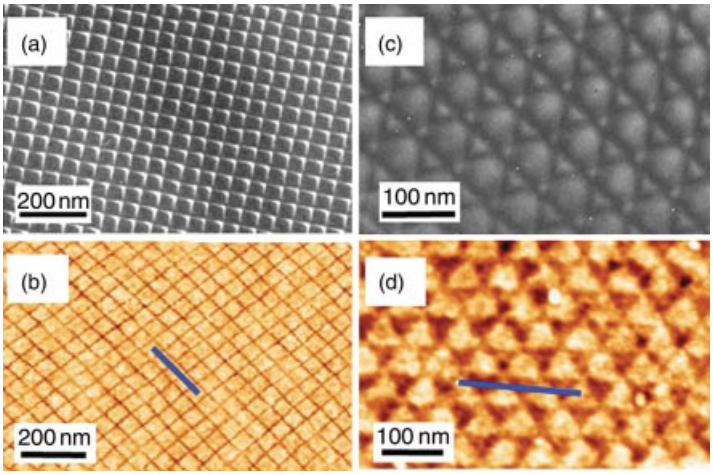


**Figure 8.2** Transmission electron microscopy images of pure 0.44° twist boundaries of two—(a) Si(001) and (c) Si(111)—surfaces [13]. (b) and (d) Scanning tunneling images of the same samples after chemical etchings (for details see Ref. [13]). The height variations along the blue line profiles are, respectively, 4 and 2.5 nm.

## 8.2.2 Patterning through Vicinal Surfaces

### 8.2.2.1 Generalities

A vicinal surface is obtained by cutting a crystal along a direction close to a high-symmetry direction with a disorientation angle between 0° and 15°. Annealing a vicinal surface leads to a rearrangement of matter and gives rise to a new surface consisting of a succession of steps separated by terraces. When fabricating a surface by cutting a crystal in a nominal direction or with a disorientation, the surface atoms adopt a different lattice parameter than the one in the bulk in order to minimize the free surface energy. Depending on the polar (tilt) and azimuthal (twist) miscut angles, surfaces can display different reconstructions and step–edge energies. The difference between the surface and the bulk lattice parameter induces an intrinsic stress in the surface layer that is directly related to the surface free energy. This stress is an important parameter to take into account when nanostructuring surfaces on a large scale. Steps are the most common defect in nominal crystalline surfaces, but vicinal surfaces can be intentionally offcut from a specific plane in a controlled manner to favor anisotropic growth of various nanostructures [16, 17]. The structural properties of the most frequently used semiconductor surfaces, Si(111) and Si(100), will be presented.

### 8.2.2.2 Vicinal Si(111)

Vicinal Si(111) surfaces transform under thermal treatment into two very distinct morphologies, depending on the azimuthal miscut direction. A vicinal Si(111) surface disoriented toward the $[11\bar{2}]$ azimuthal direction reorganizes into a series of terraces and steps. In this case, terraces with dimensions of several tens of nanometers are separated by step bunches [18]. When vicinals are cut toward the opposite azimuthal direction $[\bar{1}\bar{1}2]$, they rearrange into a pattern of smaller terraces separated by steps that are mono- or triple-layer high. An example of these two vicinal Si(111) surfaces is given in Figure 8.3. Step arrays with spacings of only a few nanometers can be made by using higher tilt angles such as on Si(557) $3 \times 1$ [19]. Here, the regularity of the step arrays is controlled by the step–step interactions, facet energies, and lateral extension of the $7 \times 7$ reconstruction. The periodicity is directly related to the Si lattice constant. By carefully choosing the thermal treatment, surfaces with both miscut directions can be prepared in a controlled manner and highly regular arrays can be achieved. These can subsequently be used as templates to grow various arrays of nano-objects. In Section 8.3, the use of a vicinal Si(111) surface as a template for the ordered growth of Au–Co nanoparticle array will be presented.

### 8.2.2.3 Vicinal Si(100)

Owing to the atomic configuration of Si(100), the vicinal surfaces of this orientation show very distinct reconstructions. The Si(100) surface displays a square symmetry with a surface lattice parameter of 0.384 nm. The surface is unstable because

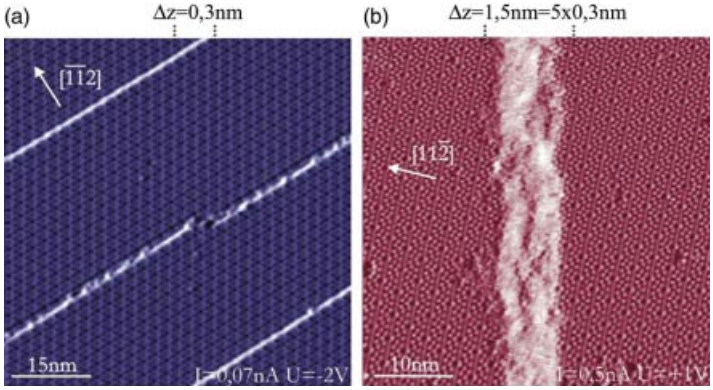


**Figure 8.3** Scanning tunneling microscopy images of Si(111) vicinals: (a) miscut in the $[\bar{1}\bar{1}2]$ direction showing an array of single steps separated by $(7 \times 7)$ reconstructed terraces and (b) miscut in the $[11\bar{2}]$ direction showing a step bunch.

each atom of the surface has two dangling bonds. The surface bonds dimerize in a $(2 \times 1)$ reconstruction resulting in $(2 \times 1)$ and $(1 \times 2)$ domains or for some conditions in $c(4 \times 2)$ and $p(2 \times 2)$ reconstructions. We conventionally define two kinds of steps: $S_a$ and $S_b$, where the upper terrace dimerization direction is perpendicular or parallel to the edge, respectively [20]. On vicinal surfaces with misorientation angles lower than 1.5°, the step heights are monoatomic and both kind of steps $S_a$ and $S_b$ alternate. As the misorientation angle is increased, the surface steps merge into double-height steps $D_b$ so that for angles higher than 8°, the whole surface consists of biatomic steps $D_b$. There is a chemical equilibrium between two phases $S_a + S_b$ and $D_b$ while the misorientation angle is increased, leading to a transition $S_a + S_b \rightarrow D_b$. This step-height transition has been extensively studied theoretically [21] and experimentally [22–24]. Changing the azimuthal misorientation gives rise to an even more complex surface reconstruction as shown in Figure 8.4a and b.

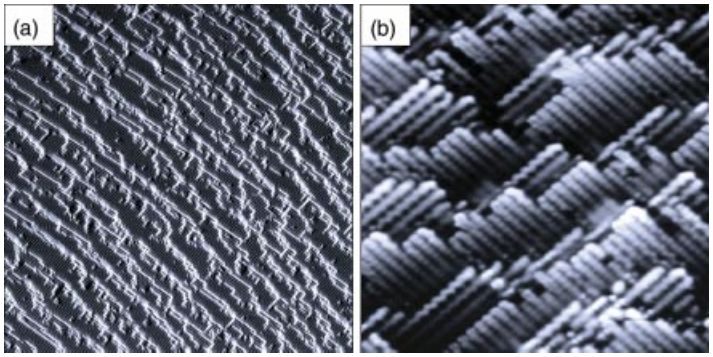


**Figure 8.4** Scanning tunneling microscopy images of a Si(100) surface tilted by 2.7° (a) with azimuthal misorientation varying from the left to the right side of the image by 10°; (b) shows an enlarged view of (a). The scanning directions are [010] and [001] and the scanned areas are, respectively, $120 \times 120$ and $12 \times 12\ nm^2$.

## 8.3
## Ordered Growth of Nano-Objects

### 8.3.1
### Growth Modes and Self-Organization

When depositing an adsorbate on a substrate, the balance of their free energies ($\delta_{\text{adsorbate}}$, $\delta_{\text{substrate}}$) and their interface free energy $\delta_{\text{interface}}$ determines their growth mode. Three main growth modes are distinguished as follows:

- $\delta_{\text{substrate}} < \delta_{\text{adsorbate}} + \delta_{\text{interface}}$
  In this case, the adsorbate will form three-dimensional islands on the substrate. This mode is called the Volmer–Weber mode (Figure 8.5). It is commonly observed if a reactive material is deposited on an inert substrate, for example, a transition metal on a noble metal or an oxide.
- $\delta_{\text{substrate}} > \delta_{\text{adsorbate}} + \delta_{\text{interface}}$
  In this situation, the first layer of the adsorbate will wet completely the substrate. For subsequent growth, two situations are possible. The atoms arriving at the surface will form further layers and the growth is then called the Frank–van der Merwe mode (layer by layer), or the free energy of the substrate is reduced enough (and the energy due to the parametric mismatch between the elements and the energy of dislocation formation comes into play) and the growth continues in the form of three-dimensional dots on the first wetting layer. This mode is called the Stranski–Krastanov (SK) mode (see Figure 8.5). This mode is widely used in

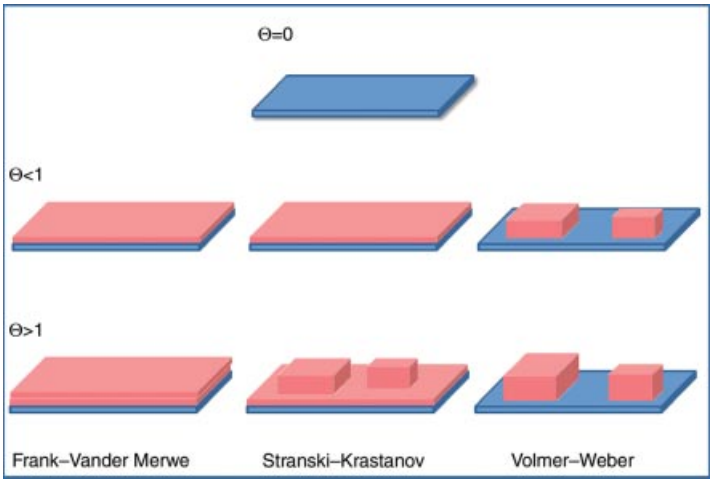


**Figure 8.5** Three major growth modes for the heteroepitaxy of 0, 1, and 2 equivalent monolayers.

the case of semiconductors and is essential when performing spontaneous self-organization of quantum boxes.

From the standpoint of the lattice parameter mismatch, we distinguish three situations linked to the presence of dislocations: coherent growth of the adsorbate on the substrate (pseudomorphic growth), totally relaxed growth of the adsorbate, and partially relaxed growth.

### 8.3.2 Quantum Dots and Nanoparticles Self-Organization with Control in Size and Position

The spontaneous self-organization is an efficient way to fabricate nanostructures such as quantum dots. Two routes can be distinguished to produce these nanostructures. First, spontaneously patterned surfaces can be used for self-organized growth. It proceeds by the preferential nucleation of species on regularly spaced surface traps [25] and occurs in a range of temperature where the diffusion length of adsorbed species is sufficient to be able to reach the preferential nucleation sites. The second way to grow the dots proceeds by strain-induced self-organization, which is also very efficient to produce ordered arrays of nanostructures [26]. In that case, the energy minimization with its strain component will drive the morphological evolution of the system. An alternative route is to combine the strain-induced self-organization on naturally or artificially prepatterned substrates. In all these direct *bottom-up* approaches, a high density of periodic nanostructures with a remarkably uniform size distribution can be obtained at large scale with a single growth step. They provide very promising ways to integrate nanodevices in the semiconductor technology process.

#### 8.3.2.1 Stranski–Krastanov Growth Mode

As previously discussed, the SK growth mode is one the three modes generally used to classify heteroepitaxial growth using thermodynamics arguments. Also known as "layer-by-layer plus island growth," this growth mode occurs for a system with small interface energy but large lattice misfit between the substrate and the grown film. In the early stages of growth, the film grows with the lattice parameter of the substrate and a layer-by-layer strained wetting film growth is observed. As the elastic energy increases with film thickness, the film may become unstable at a critical thickness after the growth of a certain number of smooth layers. The accumulated strain can be relieved by the formation of tridimensional (3D) islands [27]. The increase in the surface energy associated with the formation of clusters can be compensated by a decrease in the energy strain due to misfit dislocation nucleation underneath the islands. Islands that may be fully relaxed at the top, that is, with the bulk lattice parameter of the film material, are then formed. In some cases, strain relief occurs through the formation of nanoscale dislocation-free islands, also called coherent strained islands [28]. The relaxation of islands toward their bulk lattice parameter arises from local deformation of near-surface layers in the substrate. These defect-free islands are of great interest in nanoscale semiconductor technology to access to quantum properties. They are also used in the superlattice geometry [29], where

the vertical correlation between islands in successive layers may improve the island size and spacing uniformities. This self-organization phenomenon takes advantage of the elastic coupling in between the dots [30, 31] through the spacing layer.

Two examples will be discussed to illustrate the SK growth mode.

#### 8.3.2.2 **Au/Si(111) System**

Gold grows on Si(111) substrate via the SK mechanism to form individual Au-silicide islands on an intermediate two-dimensional layer. This wetting layer corresponds to a Si-rich Au silicide. In a recent work [32], a detailed study of the structure of the nanoparticles at the atomic scale has been performed by a combined scanning tunneling microscopy (STM) and TEM analysis. Au was deposited by means of molecular beam epitaxy in an ultrahigh vacuum chamber. Depending on the deposition temperature and the Au coverage, islands with facets or hemispherical shape can grow on the substrate. The characterization of the bulk structure by TEM and the surface structure by STM reveals that islands present several crystalline structures that were all identified as metal-rich Au silicides. We point out that the entire islands exhibit the silicide structure and no dislocations have been observed. An example of the atomic structure characterization of Au–Si islands is given in Figures 8.6 and 8.7.

By controlling the growth parameters, Rota *et al.* [33] have shown that arrays of high-density Au-rich silicide islands can be obtained on vicinal Si(111) substrates. Under thermal treatment in ultrahigh vacuum, vicinal Si(111) surfaces, misoriented by 1.5° toward the $[11\bar{2}]$ direction, form a regular array of bunches of several steps separated by terraces of 70–100 nm width. This self-organized step-bunched

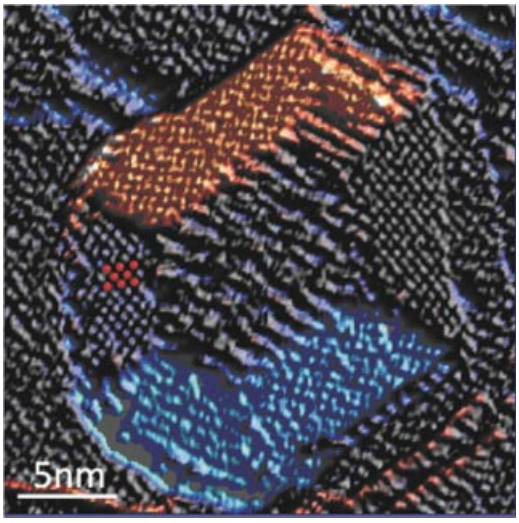


**Figure 8.6** Scanning tunneling microscopy image in the derivative mode of a faceted Au–Si nanoisland on Si(111), 3.5 nm in height. Added red balls on the facet correspond to the surface mesh.

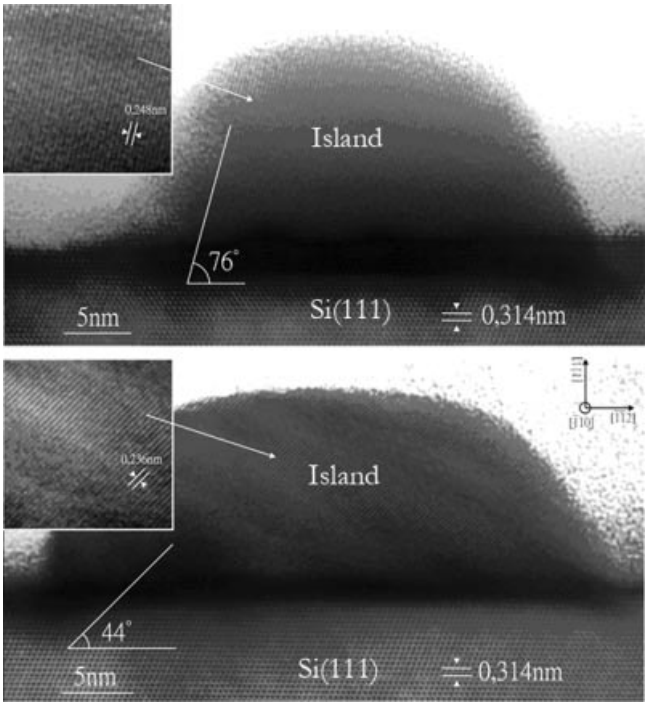


**Figure 8.7** High-resolution transmission electron microscopy image of two different hemispherical Au–Si nanoislands on Si(111). Cross-sectional views (insets) in which atomic planes are visible.

Si(111) surface can be used as a template for the self-organized growth of Au-silicide islands aligned in a 1D lattice, taking advantage of a preferred nucleation at step edges. Figure 8.8 shows the dependence of the island distribution on the surface with the growth temperature for a gold coverage of 3.5 ML (1 ML corresponds to $7.84 \times 10^{14}$ atoms/cm$^2$). At 340 °C and above, the gold atoms can reach the step bunches due to the adatom diffusion length value and all islands nucleate at step edges. Remarkably, a high density ($4 \times 10^{10}$ cm$^{-2}$) of nanoislands of about 20 nm in diameter is well aligned along step bunches for the 340 °C temperature. As expected in self-organized epitaxial growth, the islands have a narrower size distribution compared to "classical" epitaxial growth on homogeneous surfaces.

As the metal-rich Au-silicide nanoislands are supported on a Si-rich Au-silicide layer, a chemical patterning of the substrate is thus obtained through the deposition of Au. Subsequent deposition of Co leads to a magnetic patterning of the surface. The 2D and 3D gold silicides formed on the substrate react in a different way with Co: a nonmagnetic silicide is formed on terraces, while the 3D nanoparticles covered with Co exhibit magnetic properties at room temperature. These magnetic properties have been characterized by magneto-optical Kerr effect and alternating gradient force magnetometry [32, 34]. This magnetic functionalization of the surface can find applications in high-density magnetic data storage.

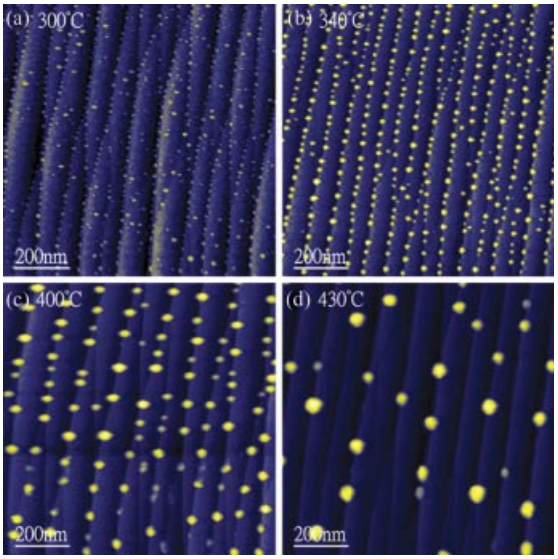


**Figure 8.8** Scanning tunneling microscopy images (1000 $nm^2$) of a vicinal Si(111) surface after the deposition of 3.5 equiv Au monolayers at (a) 300 °C, (b) 340 °C, (c) 400 °C, and (d) 430 °C. The Au–Si nanoislands are shown in yellow.

#### 8.3.2.3 **Ge/Si(001) System**

The self-organization of Ge quantum dots on Si(001) has been extensively studied in the literature [35]. The nanostructures can be first fabricated by elastic strain relaxation without applying any patterning technique. Misfit lattice strain of SiGe materials deposited on Si substrates can relax by bunching of atomic surface steps with SiGe agglomeration at the step edges or by nucleation of Ge-rich islands in the SK growth mode. Their formation mechanisms have been studied in detail [36], as well as the self-alignment and coarsening of quantum dots embedded in silicon [37]. SiGe islands may also be grown on pit-patterned Si(001) substrates, which pins the island position and suppresses lateral motion [38]. The size distribution of the objects can be advantageously decreased by stacking (and ordering) along the vertical direction arrays of SiGe/Si(001) islands [39].

### 8.3.3
### Wires: Catalytic and Catalyst-Free Growths with Control in Size and Position

Wires, rods, and pillars[1)] constitute a new type of materials to control the positioning of nanostructures. They provide new opportunities to get original heterostructures with low-dimensionality and quantum effects. The properties of homogeneous wires

1) The *nano* prefix is usually used to stress a small diameter (<100 nm), whereas the term *wire* refers to a large length/diameter ratio (>10). Rods and pillars often refer to intermediate situations. For the sake of simplicity, the generic objects will be called wires in this chapter.

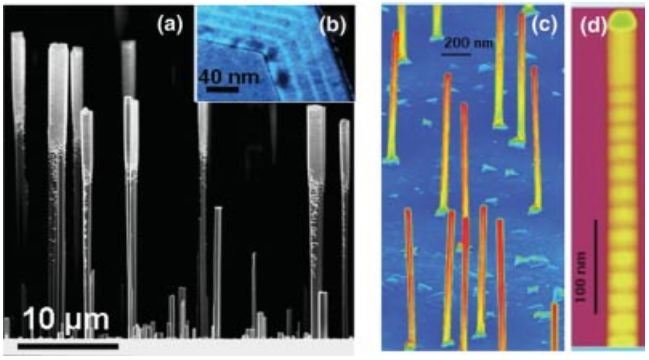


**Figure 8.9** (a) Radial InGaN/GaN multiple quantum wells at the top of GaN wire templates. (b) The wire cross section with five periods [48]. (c) Longitudinal InAs/InP superlattices inserted in InAs wires. (d) A magnification of the structure [66].

have been studied intensively for both individual objects and assemblies at random or selected positions, and they can also be used as templates for heterostructure growth, making possible longitudinal or radial stackings at the top or on the edges of the wires by a careful engineering of growth conditions [40]. This has been mainly evidenced in semiconductor systems and two examples exhibiting wires grown by metal organic chemical vapor deposition with radial GaN/InGaN and longitudinal InAs/InP superlattice insertions are shown in Figure 8.9. This geometry largely facilitates the integration of objects in devices [41] and also allows fabricating 3D wire networks with controlled diameters/arrangements and effective interwire connectivity. Their specific strain tensor—directly related to the free surface and interface relaxations—plays a key role in tuning the physical properties [42] and strain engineering has been used in a large number of applications. The most striking examples come again from the semiconductor field where an impressive number of wire-based demonstrations have been achieved in electronics (transistors, capacitors, etc.), optics (emitters, detectors), thermal (thermoelectricity), mechanical (NEMS), and chemical devices (sensors) [43, 44]. Many recent advances in synthesis have been achieved using several methods: chemistry, laser ablation, molecular beam epitaxy, and chemical vapor deposition, each of them involving very different growth mechanisms (see, for example, Ref. [45] for the molecular beam epitaxy growth). In most cases, the wire growth process utilizes a metal catalyst (usually gold) defining directly the wire diameter and the so-called vapor–liquid–solid (VLS) method, which was applied for the first time more than four decades ago by Wagner and Ellis [46]. In this mechanism, a catalytic liquid alloy phase can rapidly adsorb a vapor to saturation levels and crystal growth occurs from seeds nucleated at the liquid–solid interface [47]. Depending on materials and applications, the catalyst incorporation may harm the intrinsic electrical, optical, or chemical properties of the wires. These drawbacks have motivated the catalyst-free growth of semiconductor wires, which have been demonstrated, for example, in GaN [48–50] and ZnO [51] wires. Self-organized processes requiring no *ex situ* surface preparation before growth have been used; they generally need the deposition of a very thin mask or

additive layers that may be spontaneously thinned or rearranged locally to allow the epitaxial growth of wires (see some examples in Refs [48, 52, 53]). Thicker masks are also very effective in localizing the growth of semiconductor nanostructures. They are obtained by various techniques, such as interferometric lithography for regular arrays, nanoimprint, and e-beam lithography. For GaN materials (Figure 8.10), the use of thick patterned mask has been essentially developed in metal organic vapor phase epitaxy (MOVPE) with dielectrics ($SiO_2$ or $Si_3N_4$) to control the position and size of nanostructures as stripes, pyramids [54], and wires [55–57] and more recently in molecular beam epitaxy using Ti patterned masks [58].

#### 8.3.3.1 Strain in Bottom-Up Wire Heterostructures: Longitudinal and Radial Heterostructures

Like in conventional planar heterostructures, the structural quality of the wire surface is a critical feature necessary to produce epitaxial or fully coherent layers without defects. The strain energy can be relieved in planar films, for instance, by bending thin substrates, by introducing misfit dislocations at the interface, by forming new crystalline phases and interdiffusion, by surface instability and roughness, or by a transition from 2D film growth to 3D island growth (i.e., Stranski–Krastanov mechanism). These ingredients may also be present in wire heterostructures, but for this geometry and especially for small enough diameter, the main relaxation phenomenon can occur from a strong elastic relaxation coming from the surface and interfaces. The partitioning of the strain energy is therefore strongly modified, which allows accessing to new material combinations that overcome the usual 2D limitations in terms of critical film thickness [59].

In wire heterostructures, analytical models have extended the critical thickness approach of Matthews that explains equilibrium and coherency limits in planar heterostructures to take into account the lateral relaxations occurring at the boundaries [60, 61]. For radial heterostructures (so-called core/shell wires, see Figure 8.9a and b), assuming that the system exhibits radial symmetry and no displacement in the tangential direction, the application of continuum elasticity theory to misfit-strained core/shell structures gives very simple expressions of the displacement fields for coherently strained materials [60–62]: $u_n(r) = A_n r + B_n/r$, $u_n(z) = C_n z + D_n$, where $z(r)$ is along the length (radius) of the wire and $A_n$, $B_n$, $C_n$, $D_n$ ($n = c$, s for the core and shell, respectively) are eight coefficients expressed as a function of $R_n$ radii and elastic coefficients. The corresponding strain energy—deduced from the displacement fields—is generally lower than an analogous planar heterostructure. The critical values giving the limit of coherently strained structures can be calculated for a given type of defect that is assumed to nucleate first (single dislocation, dislocation loop, etc.). The stability diagrams as a function of the $R_n$ radii have been evaluated for several core/shell systems, for instance, cubic Si/Ge [60] and hexagonal GaN/InGaN and GaN/AlGaN [62]. The validity of these models has not been tested extensively by experiments due to the difficulty of fabricating homogeneous assemblies of core/shell heterostructures, but strain has been measured in single objects by electron microscopy to confirm the expansion of the coherent stability domain and study the nature of the interfacial defects [63–65]. X-ray diffraction techniques are beginning to be applied

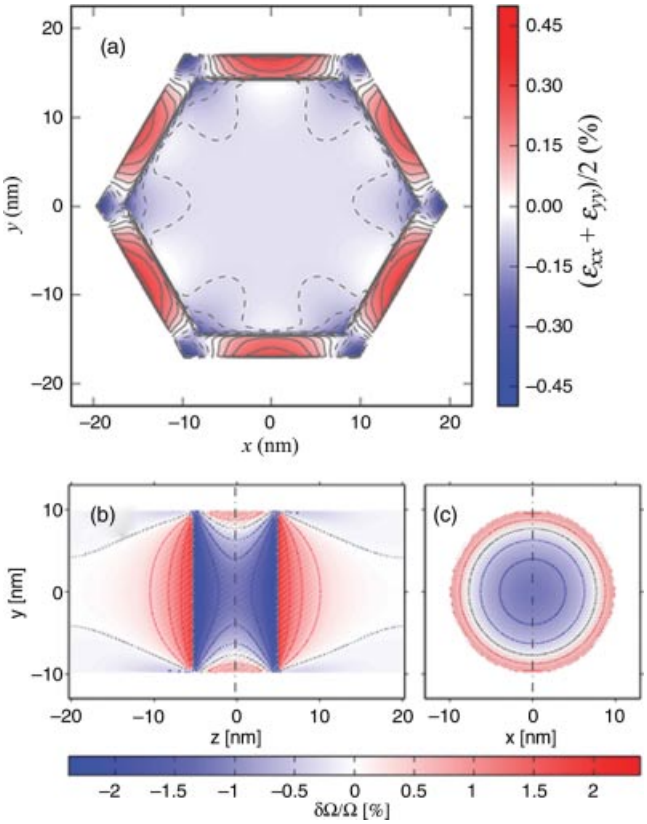


**Figure 8.10** Atomistic valence force field simulations of nanowire heterostructures [66, 69]. (a) In-plane deformation for a 30 nm GaN core/3 nm AlN shell wire. Hydrostatic strain for a longitudinal heterostructure 10 nm InAs/20 nm InP: (b) axial and (c) radial views.

to gain the strain tensor of wire assemblies [66, 67] and more recently on single objects [68]. These strain mapping measurements can be directly compared to finite element calculations and atomistic calculations. For compound semiconductors, semi-empirical potentials have been used [69, 70]. Figure 8.10a shows the strain profile of a hexagonal GaN/AlN core/shell heterostructure denoting a high strain relaxation at the edges with a change of sign. This last method also gives the atomic positions of anions and cations necessary to calculate electronic or transport properties in wires: this point is illustrated in Ref. [69] through electronic and optical properties of quantum dots and tunnel barriers of InAs/InP nanowire heterostructures.

The number of possible coherent structures for a given pair of materials can also be increased by using longitudinal wire heterostructures. Figure 8.9c and d shows a InAs/InP longitudinal wire growth and corresponding calculated elastic relaxations with atomistic potentials are shown in Figure 8.10b. For diameter in the nanometer range, longitudinal heterostructures allow controlling quantum dot formation with electronic confinement in the three directions [71]. This geometry

enables a straightforward coupling of the quantum dots along the growth axis to tune their properties [72]. A new approach also consists of controlling the change of structures (e.g., to switch between cubic zinc-blende and hexagonal wurtzite structures [73]) or nucleating twins in chemically homogeneous wires to get original electronic band structures [74]. As in core/shell structure, the calculations of insertions or superlattices of mismatched materials along wires have been studied with strain-partitioning arguments [69, 75–78]. Such calculations predict the existence of a critical radius below which the heterostructure is expected to remain coherent for any thickness of axial epilayer, depending on the magnitude of the Burger's vector $b$ of the dislocation that forms (see numerical applications for several systems in Ref. [75] for $b$ in the 0.1–0.3 nm range). In each case, experimental observations have been shown to be in agreement with the models [76] although the observation of single dislocation nucleation remains a difficult task.

#### 8.3.3.2 Wires as a Position Controlled Template

*Bottom-up* growth coupled with conventional technology process [79] is often used to get a collective or homogeneous behavior of the wire assembly (see Figure 8.11 for the example of GaN wires), for example, in photonic crystals and plasmonic devices. But the wire itself with well-chosen orientations of the surface facets can be also considered as a template. It allows growing quantum dots and multiple quantum wells on defect-free crystals that are sometimes difficult to get with other techniques. For example, in GaN wurtzite wires oriented along the $\langle 11\bar{2}0\rangle$ direction, the growth of *n*-GaN/InGaN/GaN/p-AlGaN/p-GaN multicolor light emission devices has been demonstrated on the $\{1\bar{1}00\}$ and $\{0001\}$ surfaces [80] and similar structures are under development on the $\{10\bar{1}0\}$ plane edge facets of *c*-axis wires. These studies are motivated by the bandgap engineering of optoelectronic devices that must take into account internal and piezoelectric fields imposed by the crystallographic structures [81]: semipolar and nonpolar surface orientations may favor the quantum efficiency of the emission process, that is, the radiative recombination of electrons and holes. The integration of such devices is obtained preferentially by direct growth of vertical wire arrays to benefit from parallel integration. For sensor applications [82], where it is better to use the whole surface, a bridging method between two electrodes can also be applied. So far, horizontally aligned wires have been mostly used for research purpose by contacting them individually to inject the current or to control the tension. However, many new improvements may benefit to future device mass

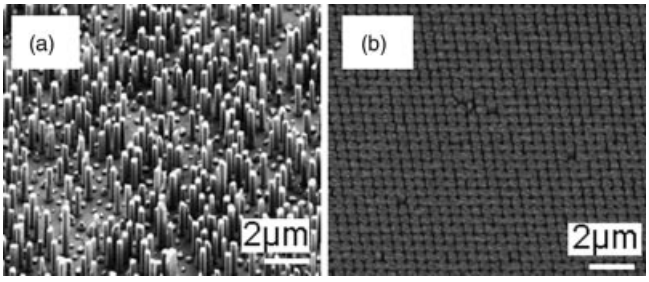


**Figure 8.11** GaN wires (oriented along the *c*-axis) grown on patterned *c*-sapphire substrates. Selective growth is obtained with a $Si_3N_4$ mask. (a) Partial filing of the sites and (b) complete filing.

production in this horizontal geometry [83]. Indeed, it has been shown that wires can be transferred by alignment techniques with fluid flow in microchannel, by interactions with chemically patterned surfaces, by Langmuir–Blodgett technique, by electric and magnetic fields assisted orientation, and so on.

## 8.4 Conclusions

This chapter has illustrated the large variety of avenues to fabricate semiconductor templates for the growth of nano-objects. The realization of artificially prepatterned surfaces is very versatile and takes advantage of the continuous improvement in many lithography and etching techniques. These approaches have been enriched by the use of strained materials and buried stressors and by the spontaneous patterning of vicinal surfaces.

The broad area of solutions with top-down, bottom-up, and mixed approaches provides solutions to build new materials for nanosciences and applications. The challenge remains to get a better control of size and positions of the nano-objects to define more accurately their electronic and optical properties. Quantum dots and nanoparticles have taken advantage of the patterning of planar surfaces. A tridimensional patterning is being developed using wires as templates. But up to now no one method has a monopoly, and suitable solutions are continuously proposed.

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